119-Bump BGA
Commercial Temp
Industrial Temp

512K x 18, 256K x 36 ByteSafe™ 8Mb S/DCD Sync Burst SRAMs

100 MHz–66 MHz
3.3 V V_{DD}
3.3 V and 2.5 V I/O

Features

- $\overline{FT}$ pin for user-configurable flow through or pipeline operation
- Single/Dual Cycle Deselect Selectable
- IEEE 1149.1 JTAG Compatible Boundary Scan
- On-chip write parity checking; even or odd selectable
- ZQ mode pin for user-selectable high/low output drive strength
- x16/x32 mode with on-chip parity encoding and error detection
- 3.3 V +10%/–5% core power supply
- 2.5 V or 3.3 V I/O supply
- $\overline{LBO}$ pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to SCD x18/x36 Interleaved Pipelined mode
- Byte Write ($\overline{BW}$) and/or Global Write ($\overline{GW}$) operation
- Common data inputs and data outputs
- Clock Control, registered, address, data, and control
- Internal self-timed write cycle
- Automatic power-down for portable applications
- 119-bump BGA package

		-11	-11.5	-100	-80	-66
Pipeline 3-1-1-1	tCycle	10 ns	10 ns	10 ns	12.5 ns	15 ns
	t_{KQ}	4.0 ns	4.0 ns	4.0 ns	4.5 ns	5 ns
	I_{DD}	225 mA	225 mA	225 mA	200 mA	185 mA
Flow Through 2-1-1-1	t_{KQ}	11 ns	11.5 ns	12 ns	14 ns	18 ns
	tCycle	15 ns	15 ns	15 ns	15 ns	20 ns
	I_{DD}	180 mA	180 mA	180 mA	175 mA	165 mA

Functional Description

Applications

The GS88218/36B is a 9,437,184-bit high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications, ranging from DSP main store to networking chip set support.

Controls

Addresses, data I/Os, chip enables ($\overline{E1}$ and E2), address burst control inputs ($\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$), and write control inputs ($\overline{Bx}$, $\overline{BW}$, $\overline{GW}$) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable ($\overline{G}$) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by $\overline{ADV}$. The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order ($\overline{LBO}$) input. The Burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Flow Through/Pipeline Reads

The function of the Data Output Register can be controlled by the user via the $\overline{FT}$ mode bump (Bump 5R). Holding the $\overline{FT}$ mode pin low places the RAM in Flow Through mode, causing output data to bypass the Data Output Register. Holding $\overline{FT}$ high places the RAM in Pipeline mode, activating the rising-edge-triggered Data Output Register.

SCD and DCD Pipelined Reads

The GS88218/36B is a SCD (Single Cycle Deselect) and DCD (Dual Cycle Deselect) pipelined synchronous SRAM. DCD SRAMs pipeline disable commands to the same degree as read commands. SCD SRAMs pipeline deselect commands one stage less than read commands. SCD RAMs begin turning off their outputs immediately after the deselect command has been captured in the input registers. DCD RAMs hold the deselect command for one full cycle and then begin turning off their outputs just after the second rising edge of clock. The user may configure this SRAM for either mode of operation using the SCD mode input on Bump 4L.

Byte Write and Global Write

Byte write operation is performed by using Byte Write enable ($\overline{BW}$) input combined with one or more individual byte write signals ($\overline{Bx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

ByteSafe™ Parity Functions

The GS88218/36B features ByteSafe data security functions. See **"ByteSafe™ Parity Functions" on page 8** for further information.

FLXDrive™

The ZQ pin allows selection between high drive strength (ZQ low) for multi-drop bus applications and normal drive strength (ZQ floating or high) point-to-point applications. See the **Output Driver Characteristics chart on page 38** for details.

Sleep Mode

Low power (Sleep mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

Core and Interface Voltages

The GS88218/36B operates on a 3.3 V power supply and all inputs/outputs are 3.3 V- and 2.5 V-compatible. Separate output power (V_{DDQ}) pins are used to decouple output noise from the internal circuit.

GS88236 Pad Out

119-Bump BGA—Top View

	1	2	3	4	5	6	7
A	V_{DDQ}	A_6	A_7	$\overline{ADSP}$	A_8	A_9	V_{DDQ}
B	NC	E_2	A_4	$\overline{ADSC}$	A_{15}	A_{17}	NC
C	NC	A_5	A_3	V_{DD}	A_{14}	A_{16}	NC
D	DQ_{C4}	DQ_{C9}	V_{SS}	ZQ	V_{SS}	DQ_{B9}	DQ_{B4}
E	DQ_{C3}	DQ_{C8}	V_{SS}	$\overline{E}_1$	V_{SS}	DQ_{B8}	DQ_{B3}
F	V_{DDQ}	DQ_{C7}	V_{SS}	$\overline{G}$	V_{SS}	DQ_{B7}	V_{DDQ}
G	DQ_{C2}	DQ_{C6}	$\overline{B}_C$	$\overline{ADV}$	$\overline{B}_B$	DQ_{B6}	DQ_{B2}
H	DQ_{C1}	DQ_{C5}	V_{SS}	$\overline{GW}$	V_{SS}	DQ_{B5}	DQ_{B1}
J	V_{DDQ}	V_{DD}	DP	V_{DD}	$\overline{QE}$	V_{DD}	V_{DDQ}
K	DQ_{D1}	DQ_{D5}	V_{SS}	CK	V_{SS}	DQ_{A5}	DQ_{A1}
L	DQ_{D2}	DQ_{D6}	$\overline{B}_D$	SCD	$\overline{B}_A$	DQ_{A6}	DQ_{A2}
M	V_{DDQ}	DQ_{D78}	V_{SS}	$\overline{BW}$	V_{SS}	DQ_{A7}	V_{DDQ}
N	DQ_{D3}	DQ_{D8}	V_{SS}	A_1	V_{SS}	DQ_{A8}	DQ_{A3}
P	DQ_{D4}	DQ_{D9}	V_{SS}	A_0	V_{SS}	DQ_{A9}	DQ_{A4}
R	NC	A_2	$\overline{LBO}$	V_{DD}	$\overline{FT}$	A_{13}	$\overline{PE}$
T	NC	NC	A_{10}	A_{11}	A_{12}	NC	ZZ
U	$V_{DDQ}Q$	TMS	TDI	TCK	TDO	NC	V_{DDQ}

GS88218 Pad Out

119-Bump BGA—Top View

	1	2	3	4	5	6	7
A	V_{DDQ}	A6	A7	$\overline{ADSP}$	A8	A9	V_{DDQ}
B	NC	E2	A4	$\overline{ADSC}$	A15	A17	NC
C	NC	A5	A3	V_{DD}	A14	A16	NC
D	DQ_{B1}	NC	V_{SS}	ZQ	V_{SS}	DQ_{A9}	NC
E	NC	DQ_{B2}	V_{SS}	$\overline{E}_1$	V_{SS}	NC	DQ_{A8}
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQ_{A7}	V_{DDQ}
G	NC	DQ_{B3}	$\overline{B}_B$	$\overline{ADV}$	NC	NC	DQ_{A6}
H	DQ_{B4}	NC	V_{SS}	$\overline{GW}$	V_{SS}	DQ_{A5}	NC
J	V_{DDQ}	V_{DD}	DP	V_{DD}	$\overline{QE}$	V_{DD}	V_{DDQ}
K	NC	DQ_{B5}	V_{SS}	CK	V_{SS}	NC	DQ_{A4}
L	DQ_{B6}	NC	NC	SCD	$\overline{B}_A$	DQ_{A3}	NC
M	V_{DDQ}	DQ_{B7}	V_{SS}	$\overline{BW}$	V_{SS}	NC	V_{DDQ}
N	DQ_{B8}	NC	V_{SS}	A1	V_{SS}	DQ_{A2}	NC
P	NC	DQ_{B9}	V_{SS}	A0	V_{SS}	NC	DQ_{A1}
R	NC	A2	$\overline{LBO}$	V_{DD}	$\overline{FT}$	A13	$\overline{PE}$
T	NC	A10	A11	NC	A12	A18	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

GS88218/36 BGA Pin Description

Pin Location	Symbol	Type	Description
P4, N4	A_0, A_1	I	Address field LSBs and Address Counter Preset Inputs
A2, A3, A5, A6, B3, B5, B6, C2, C3, C5, C6, R2, R6, T3, T5	An	I	Address Inputs
T4	An	I	Address Inputs (x36 Version)
T2, T6	NC	—	No Connect (x36 Version)
T2, T6	An	I	Address Inputs (x18 Version)
K7, K6, L7, L6, M6, N7, N6, P7, P6 H7, H6, G7, G6, F6, E7, E6, D7, D6 H1, H2, G1, G2, F2, E1, E2, D1, D2 K1, K2, L1, L2, M2, N1, N2, P1, P2	DQ_{A1}–DQ_{A9} DQ_{B1}–DQ_{B9} DQ_{C1}–DQ_{C9} DQ_{D1}–DQ_{D9}	I/O	Data Input and Output pins (x36 Version)
L5, G5, G3, L3	$\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$	I	Byte Write Enable for DQ_A, DQ_B, DQ_C, DQ_D I/Os; active low (x36 Version)
P7, N6, L6, K7, H6, G7, F6, E7, D6 D1, E2, G2, H1, K2, L1, M2, N1, P2	DQ_{A1}–DQ_{A9} DQ_{B1}–DQ_{B9}	I/O	Data Input and Output pins (x18 Version)
L5, G3	$\overline{B}_A$, $\overline{B}_B$	I	Byte Write Enable for DQ_A, DQ_B Data I/Os; active low (x18 Version)
P6, N7, M6, L7, K6, H7, G6, E6, D7, D2, E1, F2, G1, H2, K1, L2, N2, P1, G5, L3, T4	NC	—	No Connect (x18 Version)
K4	CK	I	Clock Input Signal; active high
M4	$\overline{BW}$	I	Byte Write—Writes all enabled bytes; active low
H4	$\overline{GW}$	I	Global Write Enable—Writes all bytes; active low
E4	$\overline{E}_1$	I	Chip Enable; active low
B2	E_2	I	Chip Enable; active high
F4	$\overline{G}$	I	Output Enable; active low
G4	$\overline{ADV}$	I	Burst address counter advance enable; active low
A4, B4	$\overline{ADSP}$, $\overline{ADSC}$	I	Address Strobe (Processor, Cache Controller); active low
T7	ZZ	I	Sleep Mode control; active high
R5	$\overline{FT}$	I	Flow Through or Pipeline mode; active low
R3	$\overline{LBO}$	I	Linear Burst Order mode; active low
L4	SCD	I	Single Cycle Deselect/Dual Cycle Deselect Mode Control
R7	$\overline{PE}$	I	Parity Bit Enable; active low (High = x16/32 Mode, Low = x18/36 Mode)
J3	DP	I	Data Parity Mode Input; 1 = Even, 0 = Odd
J5	$\overline{QE}$	O	Parity Error Out; Open Drain Output
D4	ZQ	I	FLXDrive Output Impedance Control (Low = Low Impedance [High Drive], High = High Impedance [Low Drive])
B1, C1, R1, T1, B7, C7, U6	NC	—	No Connect

GS88218/36 BGA Pin Description

Pin Location	Symbol	Type	Description
U2	TMS	I	Scan Test Mode Select
U3	TDI	I	Scan Test Data In
U5	TDO	O	Scan Test Data Out
U4	TCK	I	Scan Test Clock
J2, C4, J4, R4, J6	V_{DD}	I	Core power supply
D3, E3, F3, H3, K3, M3, N3, P3, D5, E5, F5, H5, K5, M5, N5, P5	V_{SS}	I	I/O and Core Ground
A1, F1, J1, M1, U1, A7, F7, J7, M7, U7	V_{DDQ}	I	Output driver power supply

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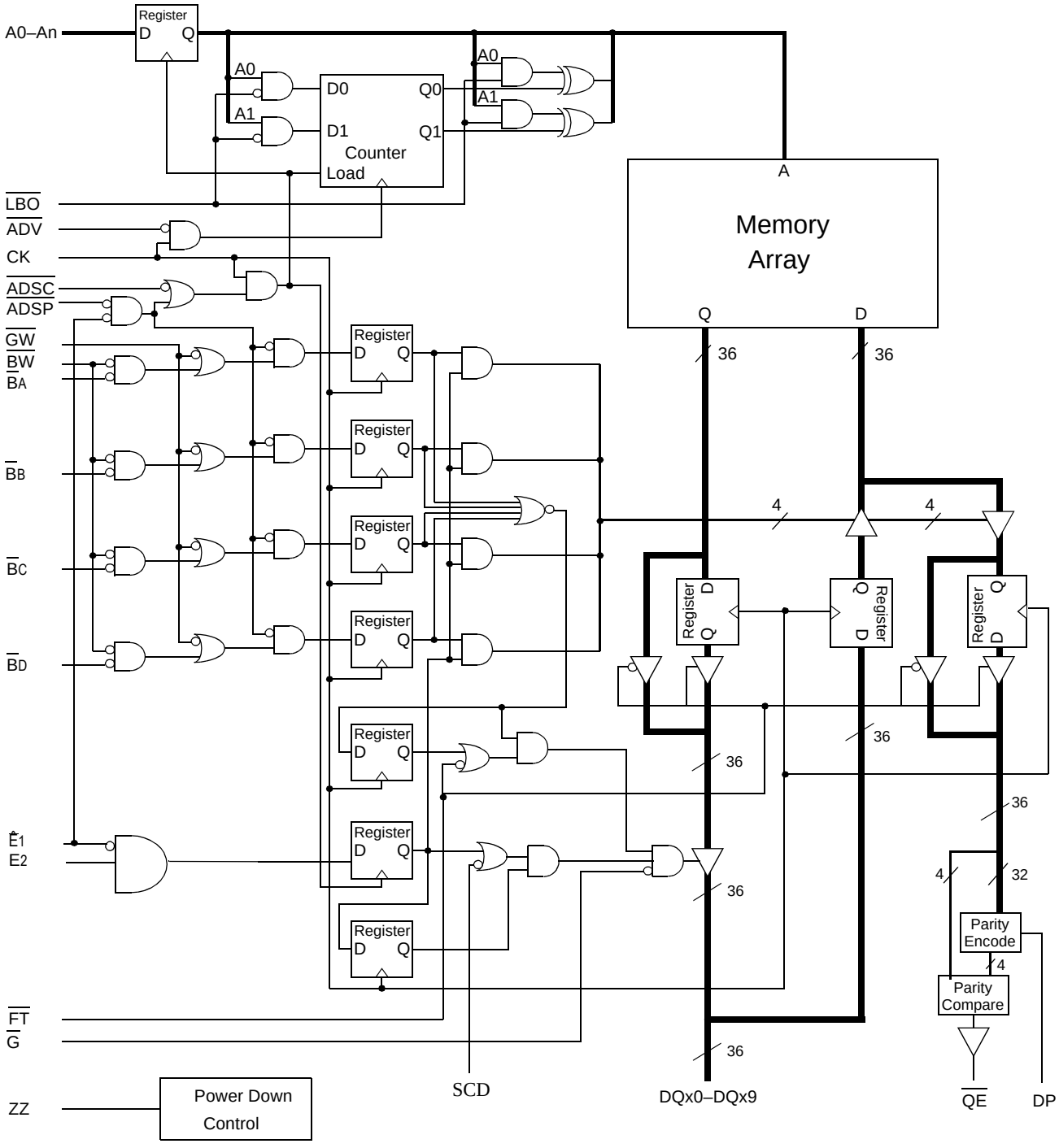
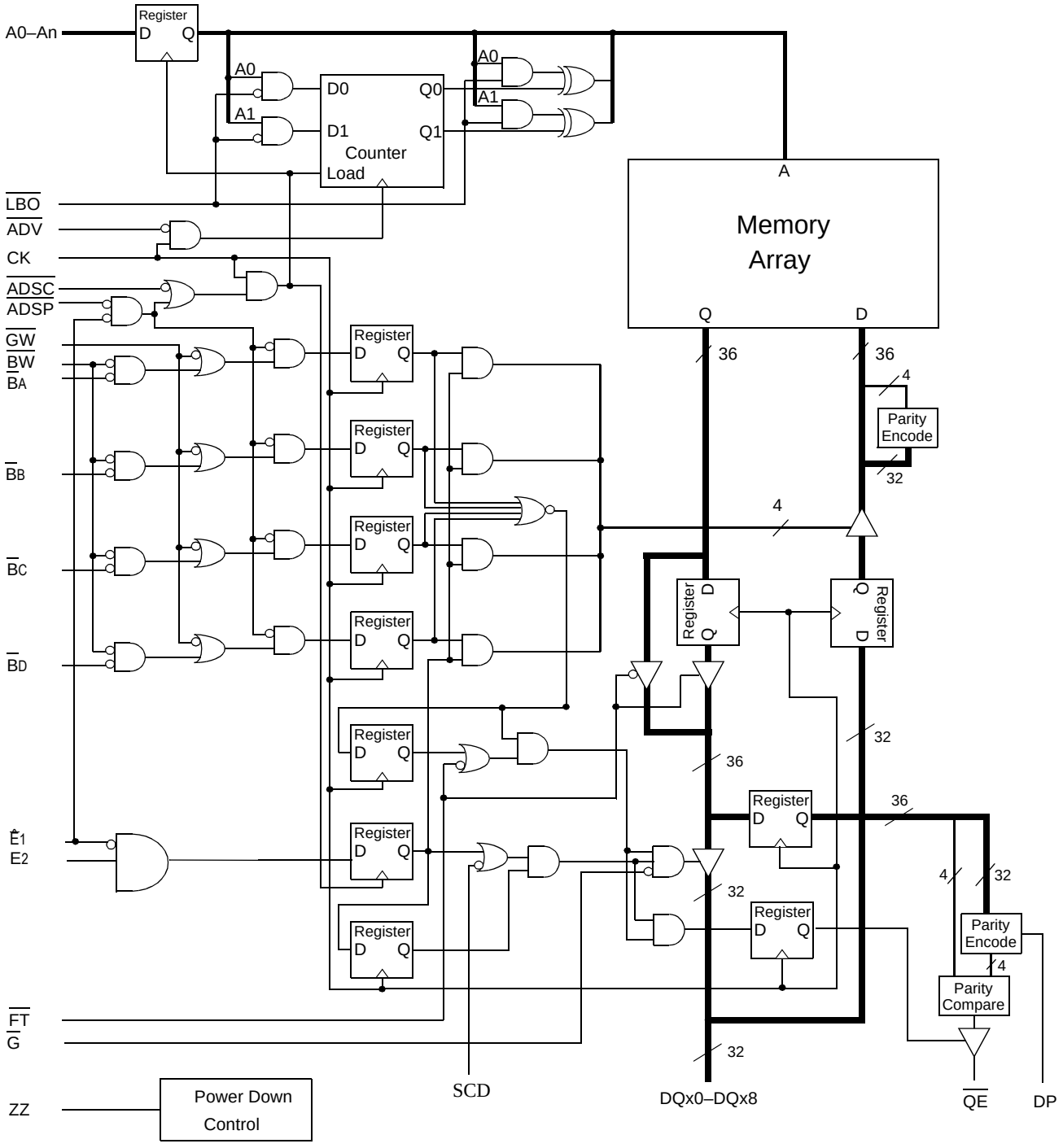
GS88218/36 ($\overline{PE}$ = 0) Block Diagram



Note: Only x36 version shown for simplicity.

GS88218/36 ($\overline{PE}$ = 1) X16x32 Mode Block Diagram



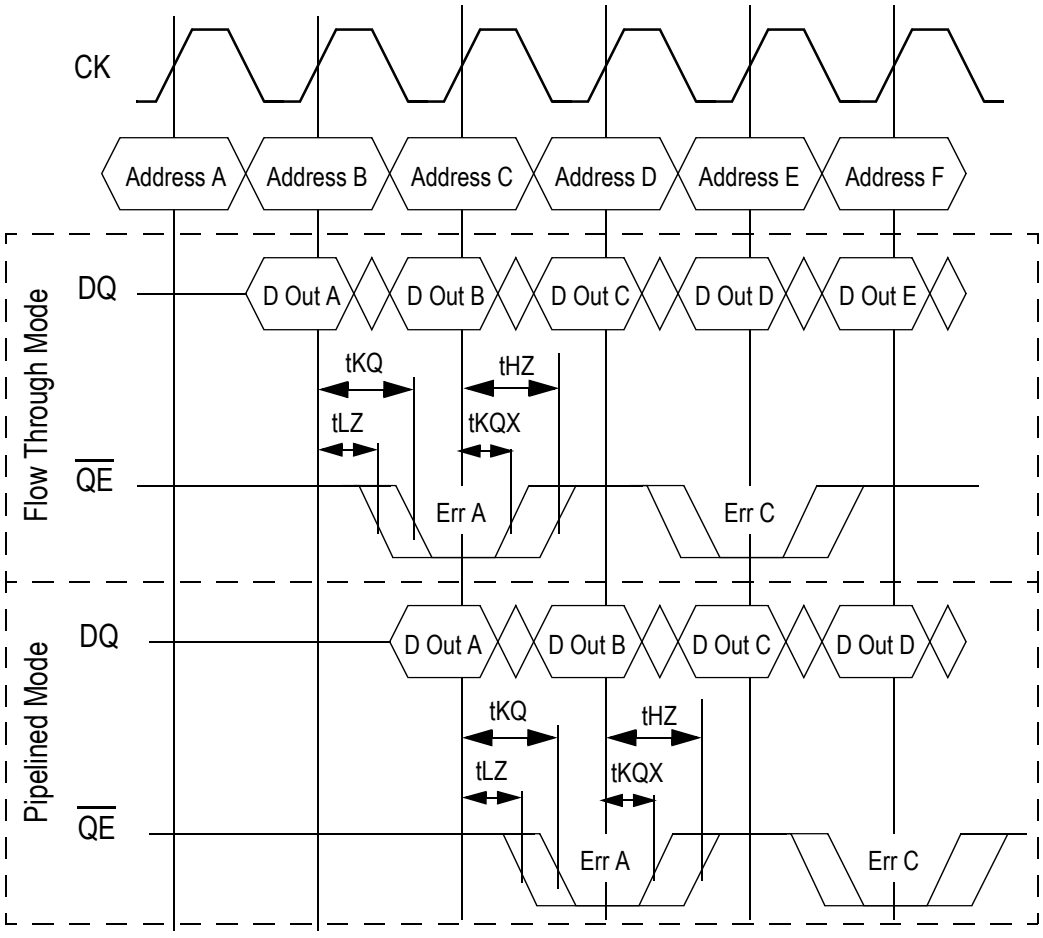
Note: Only x36 version shown for simplicity.

ByteSafe™ Parity Functions

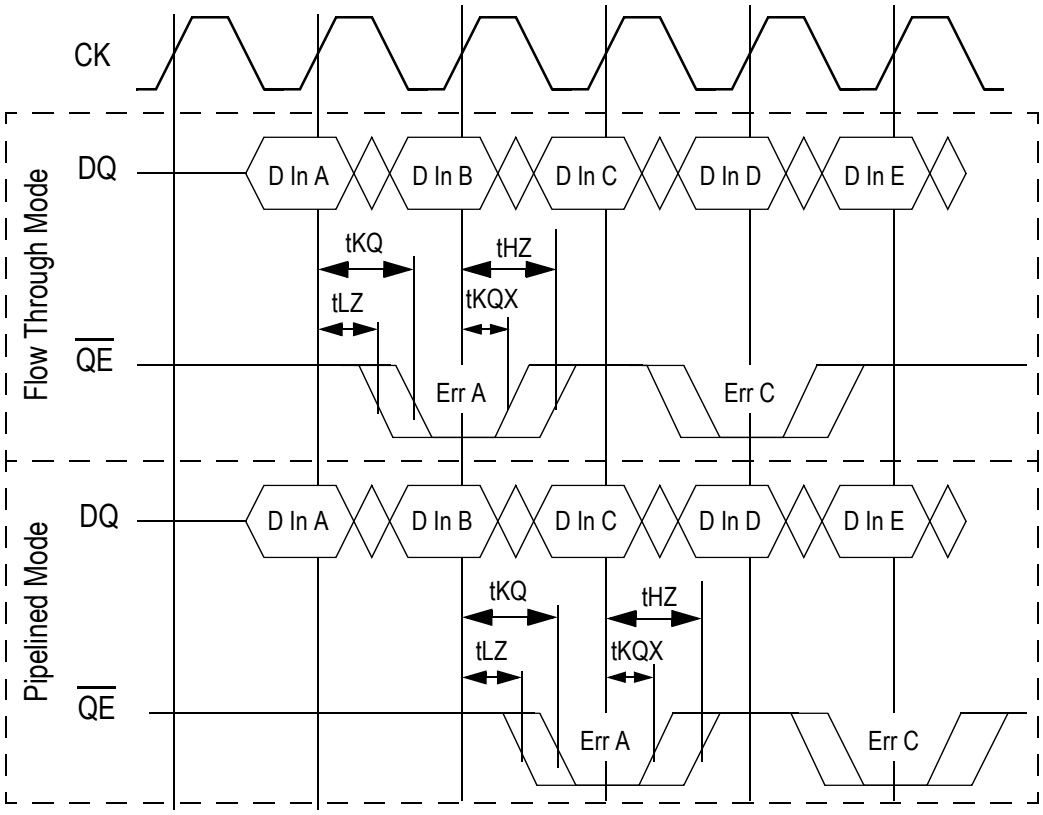
In x32/x16 mode this RAM features a parity encoding and checking function. It is assumed that the RAM is being used in x32/x16 mode because there is no source for parity bits from the system. So, in x32/x16 mode, the device generates parity and stores it along with written data. It is also assumed that there is no facility for parity checking, so the RAM checks read parity and reports an error in the cycle following parity check.
In x32/x16 mode the device does not drive the 9th data output, even though the internal ByteSafe parity encoding has been activated. A ByteSafe SRAM, used in x32/x16 mode, allows parity protection of data in applications where parity encoding or checking are not otherwise available. As in any system that checks read parity, reads of un-written memory locations may well produce parity errors. Initialization of the memory should be implemented to avoid this issue.

In x18/x36 mode this SRAM includes a write data parity check that checks the validity of data coming into the RAM on write cycles. In Flow Through mode, write data errors are reported in the cycle following the data input cycle. In Pipeline mode, write data errors are reported one clock cycle later. (See timing diagram below.) The Data Parity Mode (DP) pin must be tied high to set the RAM to check for even parity or low to check for odd parity. Read data parity is not checked by the RAM as data validity is best established at the data's destination. The Parity Error Output is an open drain output and drives low to indicate a parity error. Multiple Parity Error Output pins may share a common pull-up resistor.

x32 Mode ($\overline{PE}$ = 1) Read Parity Error Output Timing Diagram



x18/x36 Mode ($\overline{PE}$ = 0) Write Parity Error Output Timing Diagram



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Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{\text{LBO}}$	L	Linear Burst
		H or NC	Interleaved Burst
Output Register Control	$\overline{\text{FT}}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$
Single / Dual Cycle Deselect Control	SCD	L	Dual Cycle Deselect
		H or NC	Single Cycle Deselect
ByteSafe Data Parity Control	DP	L	Check for Odd Parity
		H or NC	Check for Even Parity
Parity Enable	$\overline{\text{PE}}$	L or NC	Activate 9th I/Os (x18/36 Mode)
		H	Deactivate 9th I/Os (x16/32 Mode)
FLXDrive Output Impedance Control	ZQ	L	High Drive (Low Impedance)
		H or NC	Low Drive (High Impedance)

Note:
There are pull-up devices on the $\overline{\text{LBO}}$, ZQ, SCD, DP and $\overline{\text{FT}}$ pins and a pull down device on the $\overline{\text{PE}}$ and ZZ pins, so those input pins can be unconnected and the chip will operate in the default states as specified in the above table.

Enable / Disable Parity I/O Pins

This SRAM allows the user to configure the device to operate in Parity I/O active (x18 or x36) or in Parity I/O inactive (x16 or x32) mode. Holding the $\overline{\text{PE}}$ bump low or letting it float will activate the 9th I/O on each byte of the RAM. Tying $\overline{\text{PE}}$ high deactivates the 9th I/O of each byte, although the bit in each byte of the memory array remains active to store and recall parity bits generated and read into the ByteSafe parity circuits.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note: The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note: The burst counter wraps to initial state on the 5th clock.

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Byte Write Truth Table

Function	$\overline{GW}$	$\overline{BW}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$	Notes
Read	H	H	X	X	X	X	1
Read	H	L	H	H	H	H	1
Write byte a	H	L	L	H	H	H	2, 3
Write byte b	H	L	H	L	H	H	2, 3
Write byte c	H	L	H	H	L	H	2, 3, 4
Write byte d	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

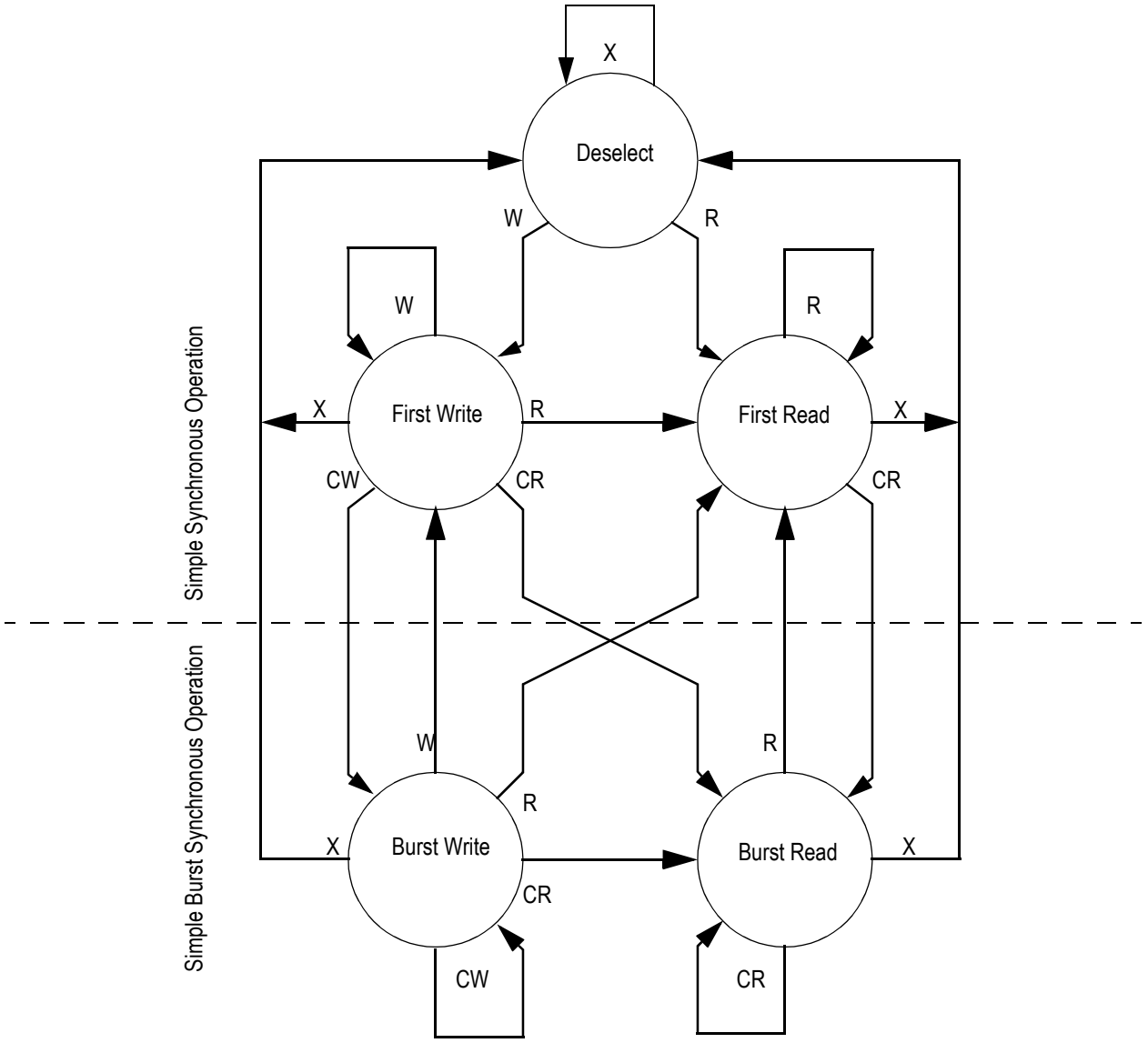
Notes:
1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs.
2. Byte Write Enable inputs $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, and/or $\overline{B}_D$ may be used in any combination with $\overline{BW}$ to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "C" and "D" are only available on the x36 version.

Synchronous Truth Table

Operation	Address Used	State Diagram Key[5]	E[2]	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	W[3]	DQ[4]
Deselect Cycle, Power Down	**None**	**X**	**X**	**X**	**L**	**X**	**X**	**High-Z**
Deselect Cycle, Power Down	None	X	F	L	X	X	X	High-Z
Deselect Cycle, Power Down	**None**	**X**	**F**	**H**	**L**	**X**	**X**	**High-Z**
Read Cycle, Begin Burst	External	R	T	L	X	X	X	Q
Read Cycle, Begin Burst	**External**	**R**	**T**	**H**	**L**	**X**	**F**	**Q**
Write Cycle, Begin Burst	**External**	**W**	**T**	**H**	**L**	**X**	**T**	**D**
Read Cycle, Continue Burst	*Next*	*CR*	*X*	*H*	*H*	*L*	*F*	*Q*
Read Cycle, Continue Burst	Next	CR	X	X	H	L	F	Q
Write Cycle, Continue Burst	*Next*	*CW*	*X*	*H*	*H*	*L*	*T*	*D*
Write Cycle, Continue Burst	Next	CW	X	X	H	L	T	D
Read Cycle, Suspend Burst	Current		X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current		X	X	H	H	F	Q
Write Cycle, Suspend Burst	Current		X	H	H	H	T	D
Write Cycle, Suspend Burst	Current		X	X	H	H	T	D

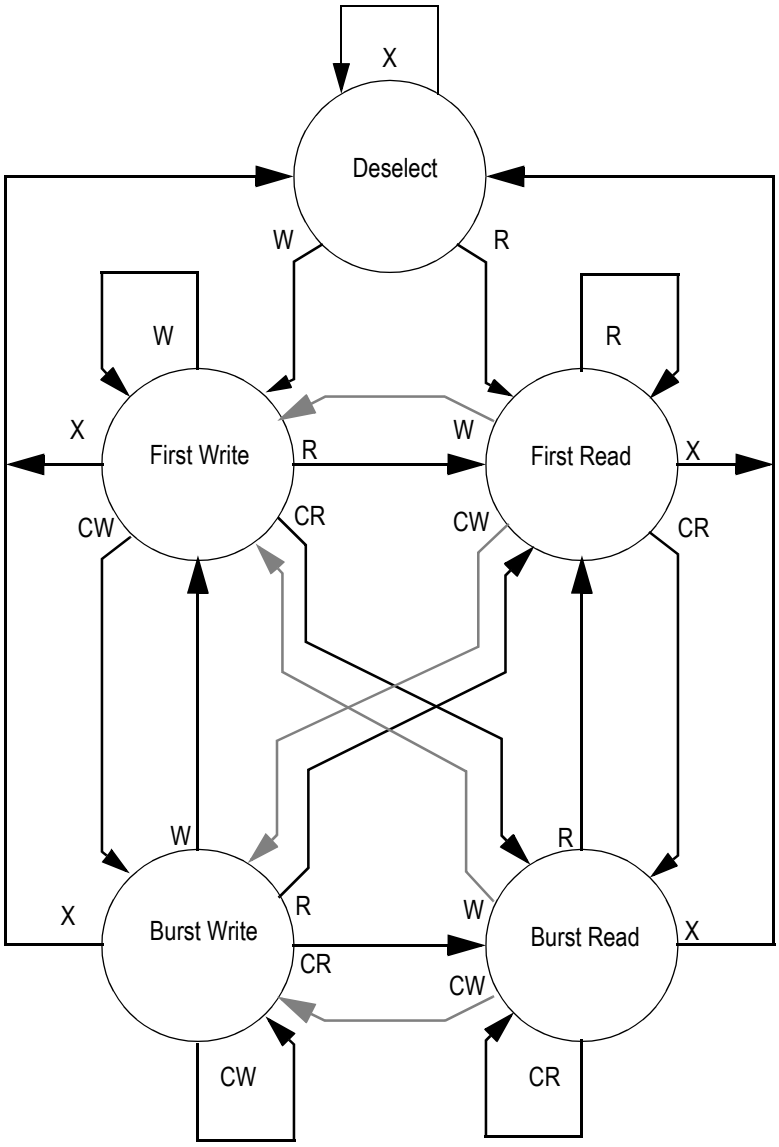
Notes:
1. X = Don't Care, H = High, L = Low
2. E = T (True) if E2 = 1; E = F (False) if E2 = 0
3. $\overline{W}$ = T (True) and F (False) is defined in the Byte Write Truth Table preceding.
4. $\overline{G}$ is an asynchronous input. $\overline{G}$ can be driven high at any time to disable active output drivers. $\overline{G}$ low can only enable active drivers (shown as "Q" in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying $\overline{ADSP}$ high and $\overline{ADSC}$ low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying $\overline{ADSP}$ high and $\overline{ADV}$ low while using $\overline{ADSC}$ to load new addresses allows simple burst operations. See *ITALIC* items above.

Simplified State Diagram



Notes:
1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes $\overline{G}$ is tied low.
2. The upper portion of the diagram assumes active use of only the Enable (E1and E2) and Write ($\overline{B_A}$, $\overline{B_B}$, $\overline{B_C}$, $\overline{B_D}$, $\overline{BW}$, and $\overline{GW}$) control inputs, and that $\overline{ADSP}$ is tied high and $\overline{ADSC}$ is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write, and $\overline{ADSC}$ control inputs, and assumes $\overline{ADSP}$ is tied high and $\overline{ADV}$ is tied low.

Simplified State Diagram with $\overline{G}$



Notes:
1. The diagram shows supported (tested) synchronous state transitions, plus supported transitions that depend upon the use of $\overline{G}$.
2. Use of "Dummy Reads" (Read Cycles with $\overline{G}$ High) may be used to make the transition from Read cycles to Write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal Read cycles.
3. Transitions shown in gray tone assume $\overline{G}$ has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to V_{DD}	V
V_{CK}	Voltage on Clock Input Pin	–0.5 to 6	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–55 to 125	°C
T_{BIAS}	Temperature Under Bias	–55 to 125	°C

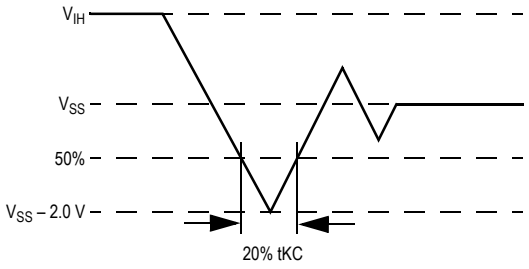
Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

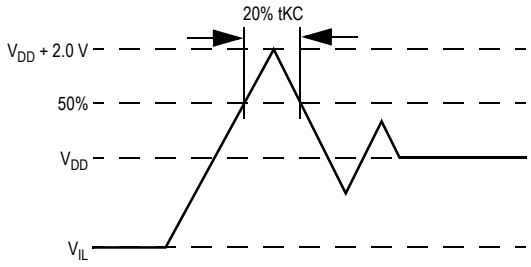
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	V_{DD}	3.135	3.3	3.6	V	
I/O Supply Voltage	V_{DDQ}	2.375	2.5	V_{DD}	V	1
Input High Voltage	V_{IH}	1.7	—	V_{DD} +0.3	V	2
Input Low Voltage	V_{IL}	–0.3	—	0.8	V	2
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	3
Ambient Temperature (Industrial Range Versions)	T_A	–40	25	85	°C	3

Notes:
1. Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both 2.75 V ≤ V_{DDQ} ≤ 2.375 V (i.e., 2.5 V I/O) and 3.6 V ≤ V_{DDQ} ≤ 3.135 V (i.e., 3.3 V I/O), and quoted at whichever condition is worst case.
2. This device features input buffers compatible with both 3.3 V and 2.5 V I/O drivers.
3. Most speed grades and configurations of this device are offered in both Commercial and Industrial Temperature ranges. The part number of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
4. Input Under/overshoot voltage must be –2 V > Vi < V_{DD} +2 V with a pulse width not to exceed 20% tKC.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 3.3 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0 V	6	7	pF

Note: These parameters are sample tested.

Package Thermal Characteristics

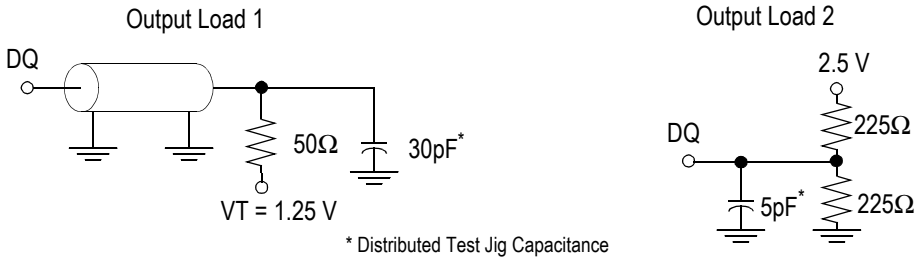
Rating	Layer Board	Symbol	Max	Unit	Notes
Junction to Ambient (at 200 lfm)	single	$R_{\Theta JA}$	40	°C/W	1,2
Junction to Ambient (at 200 lfm)	four	$R_{\Theta JA}$	24	°C/W	1,2
Junction to Case (TOP)	—	$R_{\Theta JC}$	9	°C/W	3

Notes:
1. Junction temperature is a function of SRAM power dissipation, package thermal resistance, mounting board temperature, ambient. Temperature air flow, board density, and PCB thermal resistance.
2. SCMI G-38-87
3. Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1

AC Test Conditions

Parameter	Conditions
Input high level	2.3 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	1.25 V
Output reference level	1.25 V
Output load	**Fig. 1& 2**

Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output Load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}
4. Device is deselected as defined by the Truth Table.



DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
ZZ Input Current	I_{INZZ}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0\ V \leq V_{IN} \leq V_{IH}$	–1 uA –1 uA	1 uA 300 uA
Mode Pin Input Current	I_{INM}	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0\ V \leq V_{IN} \leq V_{IL}$	–300 uA –1 uA	1 uA 1 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH}	I_{OH} = –8 mA, V_{DDQ} = 2.375 V	1.7 V	—
Output High Voltage	V_{OH}	I_{OH} = –8 mA, V_{DDQ} = 3.135 V	2.4 V	—
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	0.4 V

Operating Currents

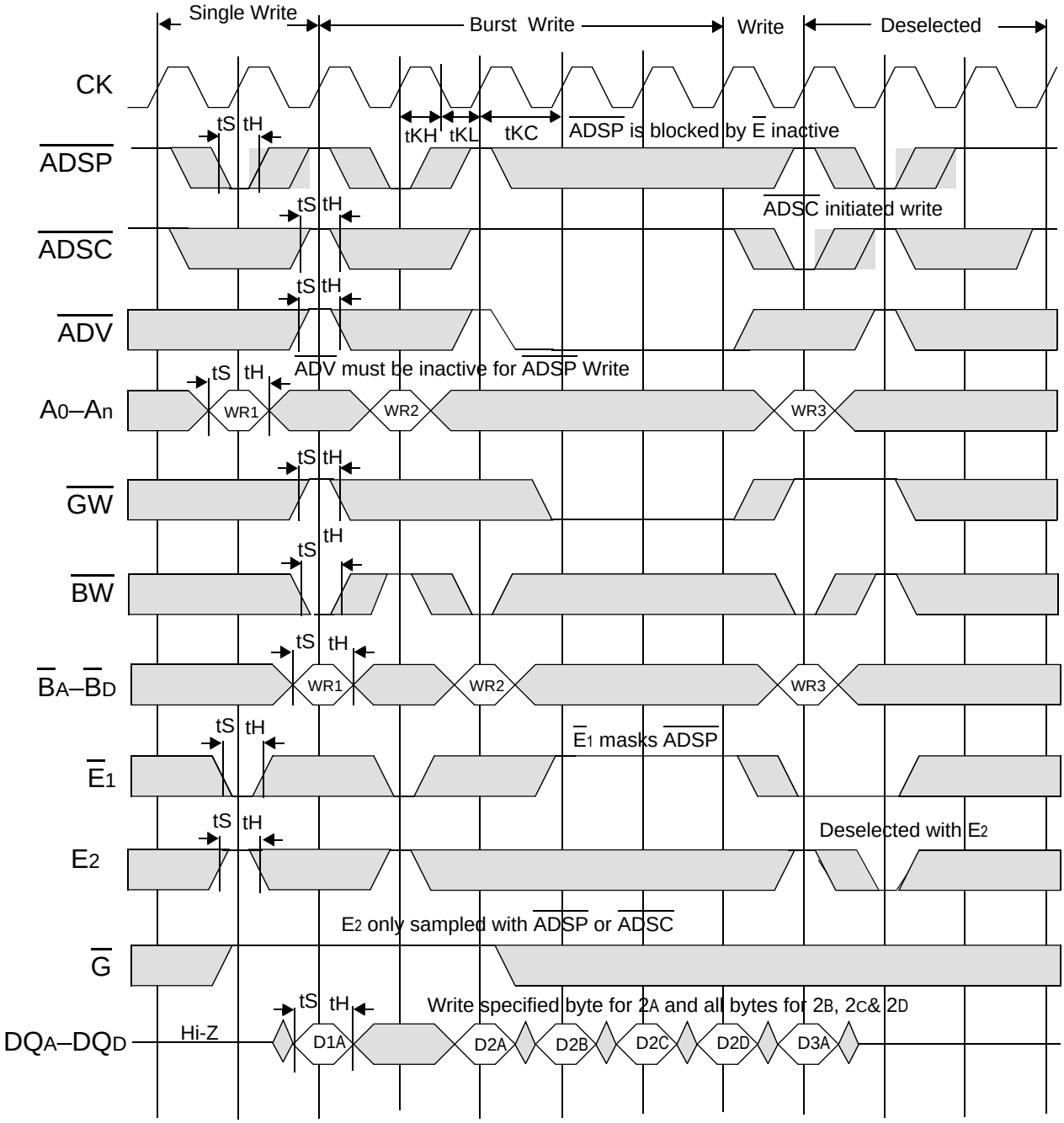
Parameter	Test Conditions	Symbol	-11		-11.5		-100		-80		-66		Unit
			0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	
Operating Current	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	I_{DD} Pipeline	225	235	225	235	225	235	200	210	185	195	mA
		I_{DD} Flow-Thru	180	190	180	190	180	190	175	185	165	175	mA
Standby Current	$ZZ \geq V_{DD}$ - 0.2V	I_{SB} Pipeline	30	40	30	40	30	40	30	40	30	40	mA
		I_{SB} Flow-Thru	30	40	30	40	30	40	30	40	30	40	mA
Deselect Current	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	I_{DD} Pipeline	80	90	80	90	80	90	70	80	60	70	mA
		I_{DD} Flow-Thru	65	75	65	75	65	75	55	65	50	60	mA

AC Electrical Characteristics

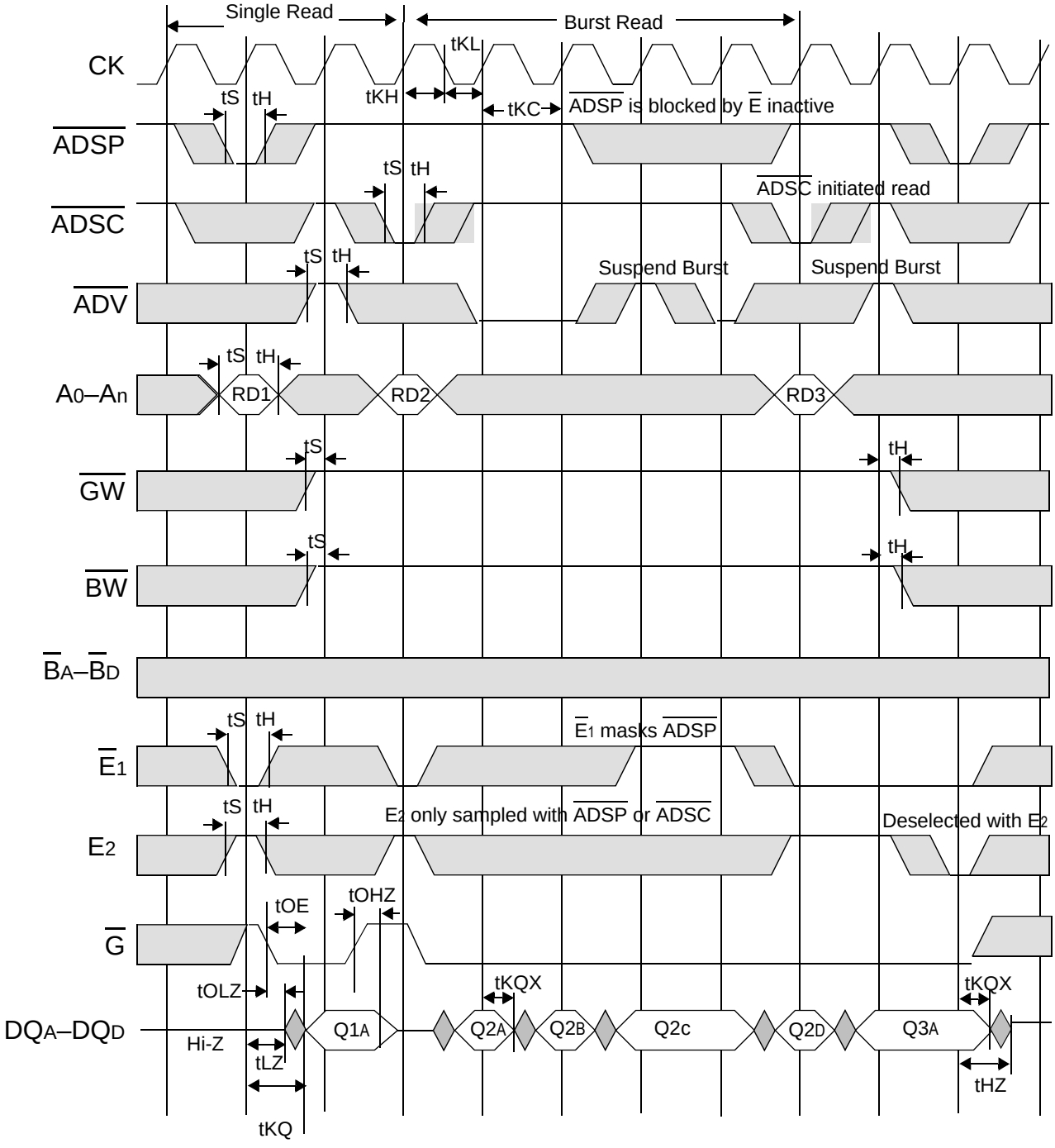
	Parameter	Symbol	-11		-11.5		-100		-80		-66		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	tKC	10	—	10	—	10	—	12.5	—	15	—	ns
	Clock to Output Valid	tKQ	—	4.0	—	4.0	—	4.0	—	4.5	—	5.0	ns
	Clock to Output Invalid	tKQX	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	tLZ[1]	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
Flow-Thru	Clock Cycle Time	tKC	15.0	—	15.0	—	15.0	—	15.0	—	20.0	—	ns
	Clock to Output Valid	tKQ	—	11.0	—	11.5	—	12.0	—	14.0	—	18.0	ns
	Clock to Output Invalid	tKQX	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock HIGH Time	tKH	1.7	—	1.7	—	2	—	2	—	2.3	—	ns
	Clock LOW Time	tKL	2	—	2	—	2.2	—	2.2	—	2.5	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	4.0	1.5	4.2	1.5	4.5	1.5	4.5	1.5	4.8	ns
	$\overline{G}$ to Output Valid	tOE	—	4.0	—	4.2	—	4.5	—	4.5	—	4.8	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	0	—	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	4.0	—	4.2	—	4.5	—	4.5	—	4.8	ns
	Setup time	tS	1.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
	Hold time	tH	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
	ZZ setup time	tZZS[2]	5	—	5	—	5	—	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	1	—	1	—	1	—	ns
	ZZ recovery	tZZR	20	—	20	—	20	—	20	—	20	—	ns

Notes:
1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

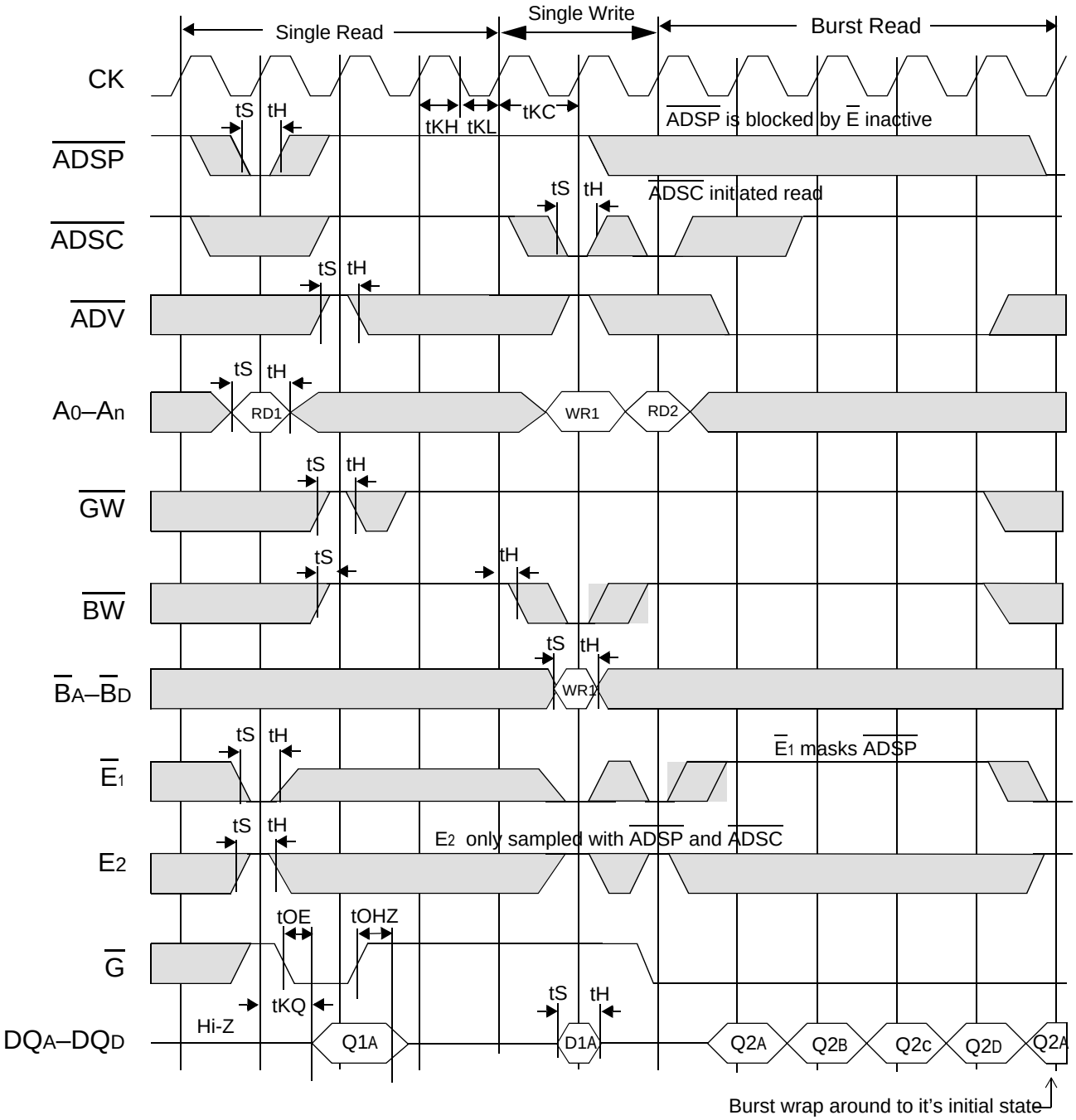
Write Cycle Timing



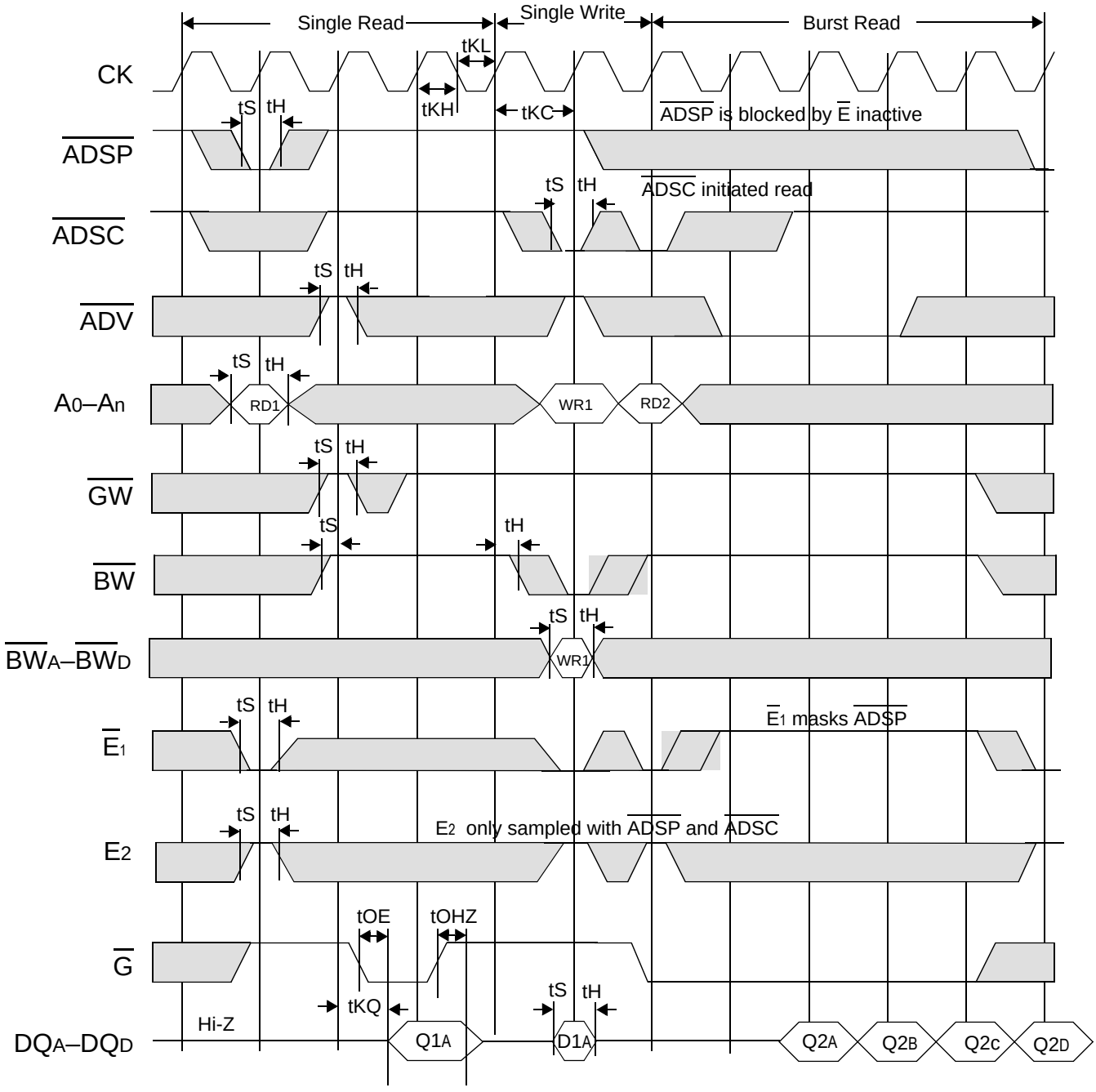
Flow Through Read Cycle Timing



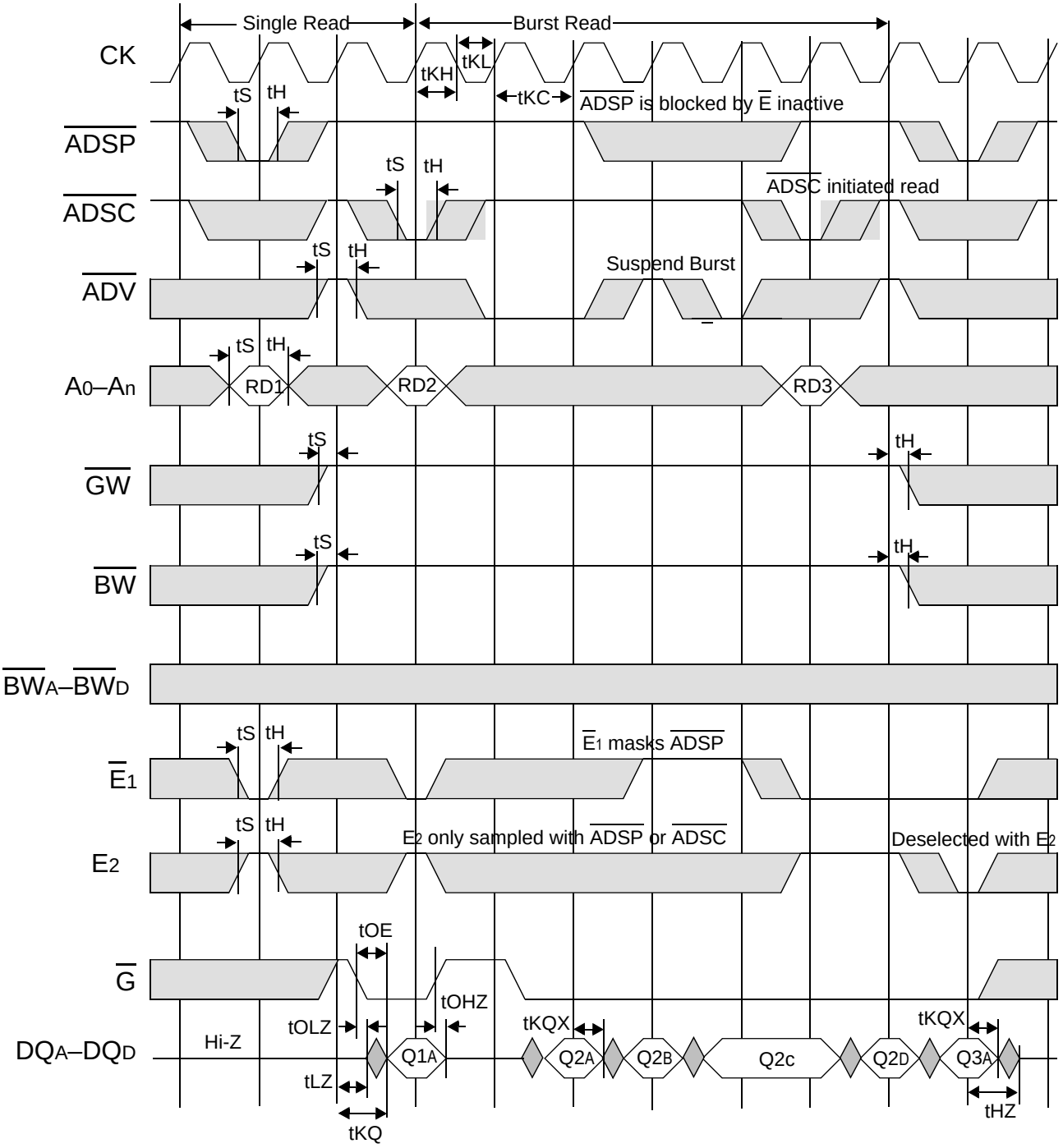
Flow Through Read-Write Cycle Timing



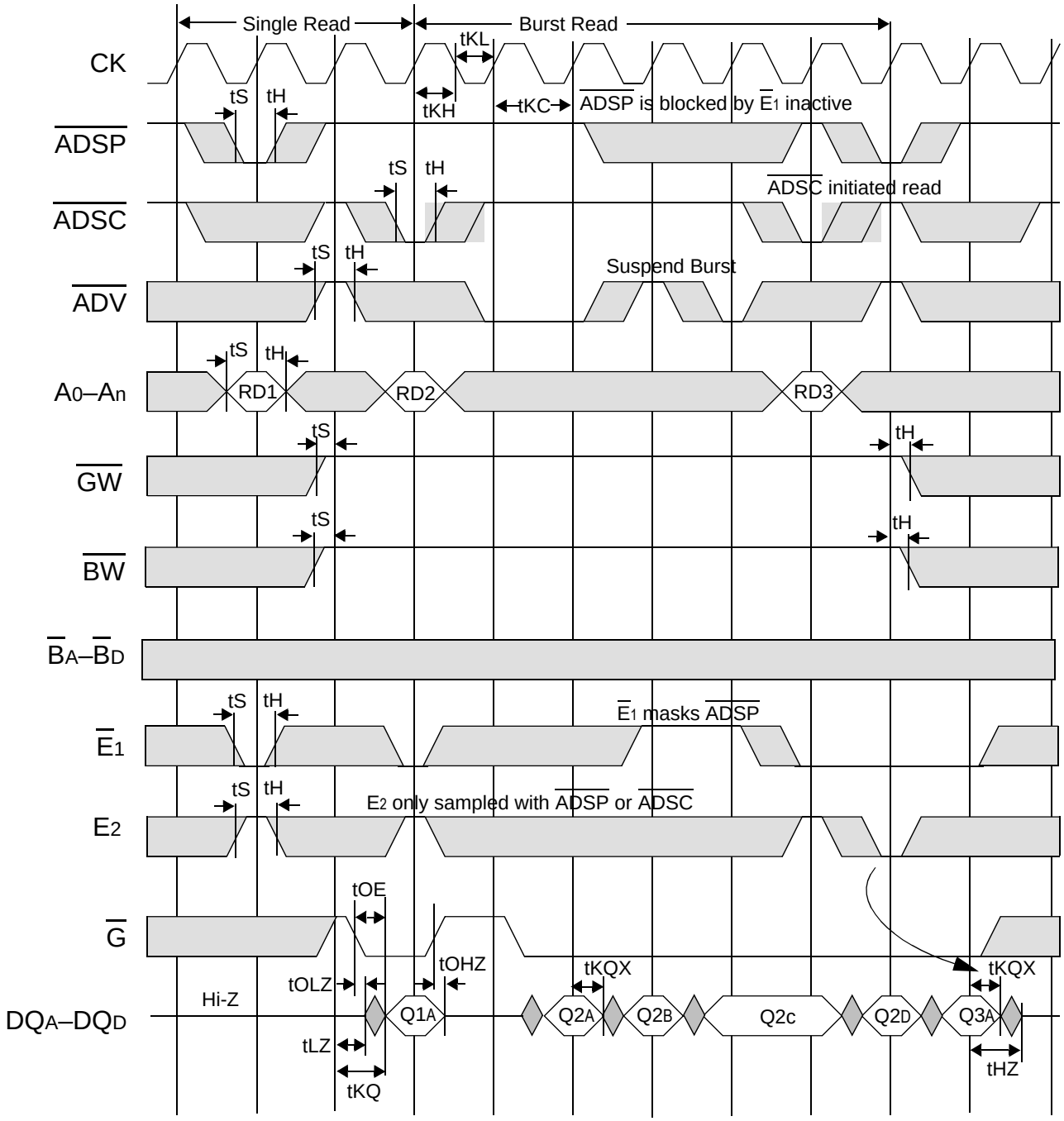
Pipelined SCD Read - Write Cycle Timing



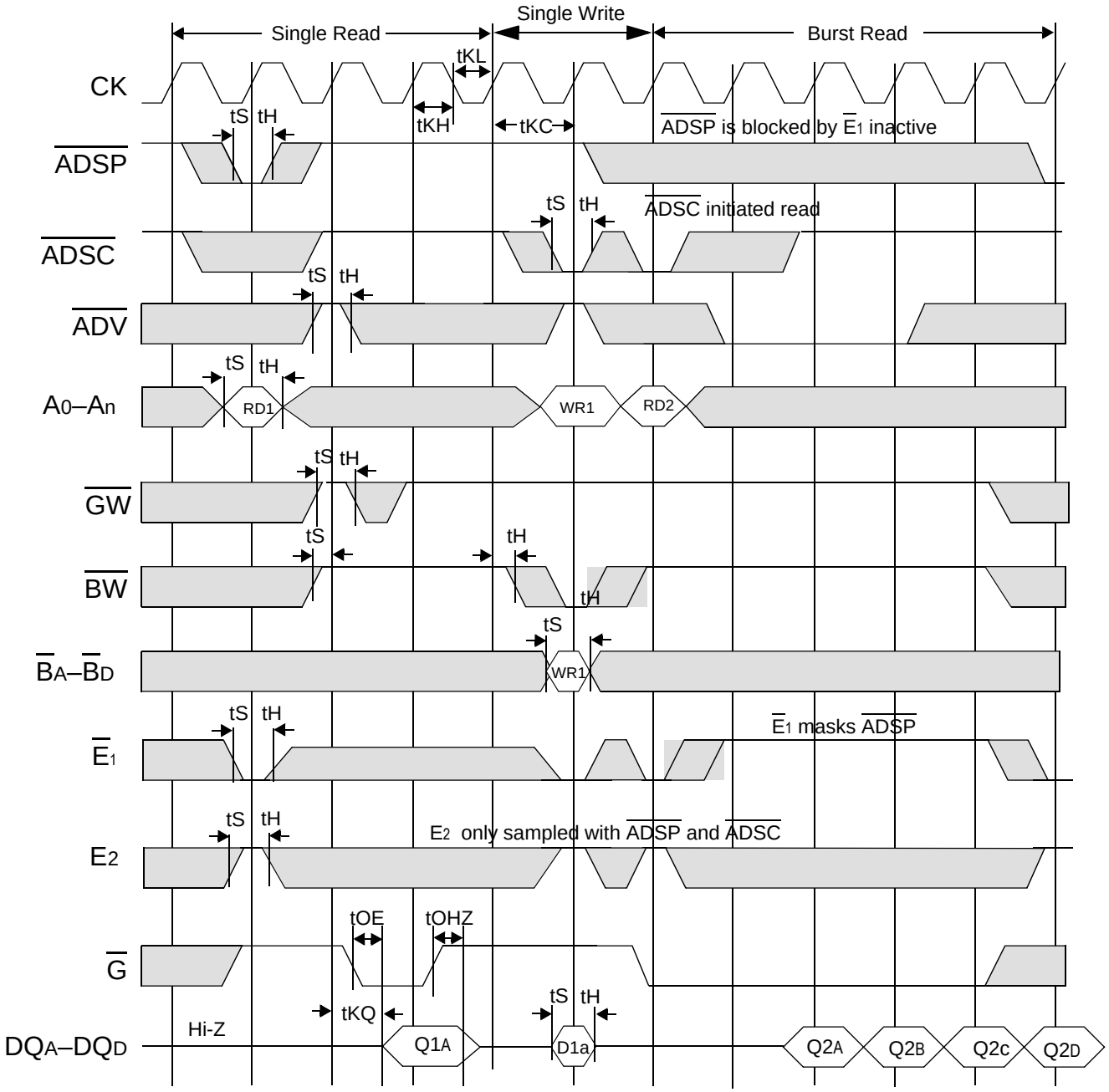
Pipelined SCD Read Cycle Timing



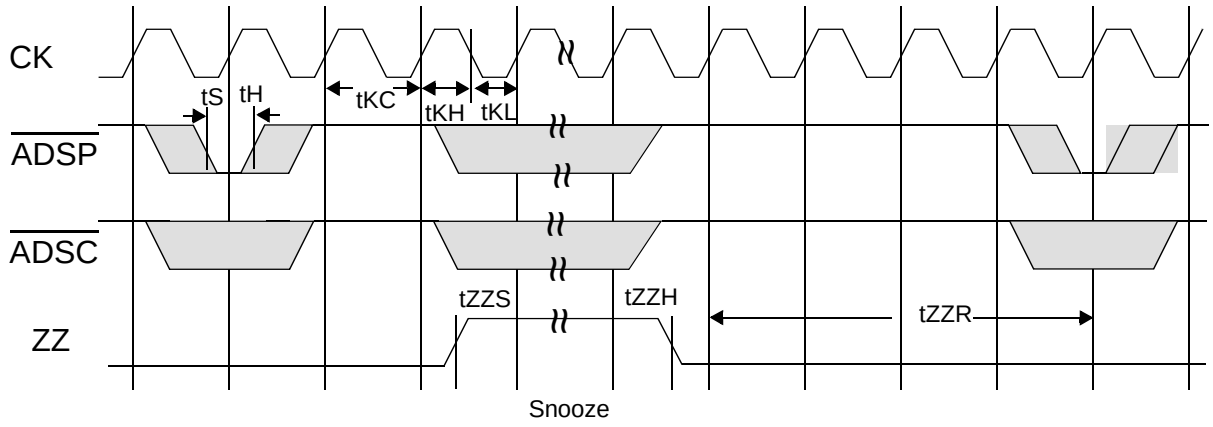
Pipelined DCD Read Cycle Timing



Pipelined DCD Read-Write Cycle Timing



Sleep Mode Timing Diagram



Application Tips

Single and Dual Cycle Deselect

SCD devices force the use of "dummy read cycles" (read cycles that are launched normally, but that are ended with the output drivers inactive) in a fully synchronous environment. Dummy read cycles waste performance, but their use usually assures there will be no bus contention in transitions from reads to writes or between banks of RAMs. DCD SRAMs do not waste bandwidth on dummy cycles and are logically simpler to manage in a multiple bank application (wait states need not be inserted at bank address boundary crossings), but greater care must be exercised to avoid excessive bus contention.

JTAG Port Operation

Overview

The JTAG Port on this RAM operates in a manner consistent with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Some functions have been modified or eliminated because they can slow the RAM. Nevertheless, the RAM supports 1149.1-1990 TAP (Test Access Port) Controller architecture, and can be expected to function in a manner that does not conflict with the operation of Standard 1149.1 compliant devices. The JTAG Port interfaces with conventional TTL / CMOS logic level signaling.

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits. To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either V_{DD} or V_{SS}. TDO should be left unconnected.

JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:
This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automaticly at power-up.

JTAG Port Registers

Overview

The various JTAG registers, refered to as TAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on the next falling edge of TCK. When a register is selected it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

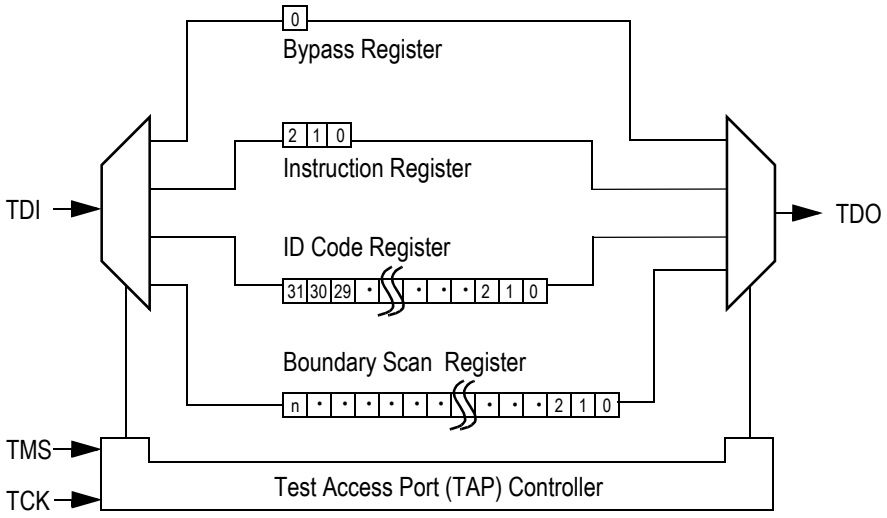
Bypass Register

The Bypass Register is a single-bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. Two TAP instructions can be used to activate the Boundary Scan Register.

JTAG TAP Block Diagram



Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Contents

	Die Revision Code				Not Used												I/O Configuration				GSI Technology JEDEC Vendor ID Code											Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x36	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	1	1	0	0	1	1
x32	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	1	1	0	0	1	1
x18	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	1	1	0	0	1	1
x16	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	0	1	1	0	0	1	1

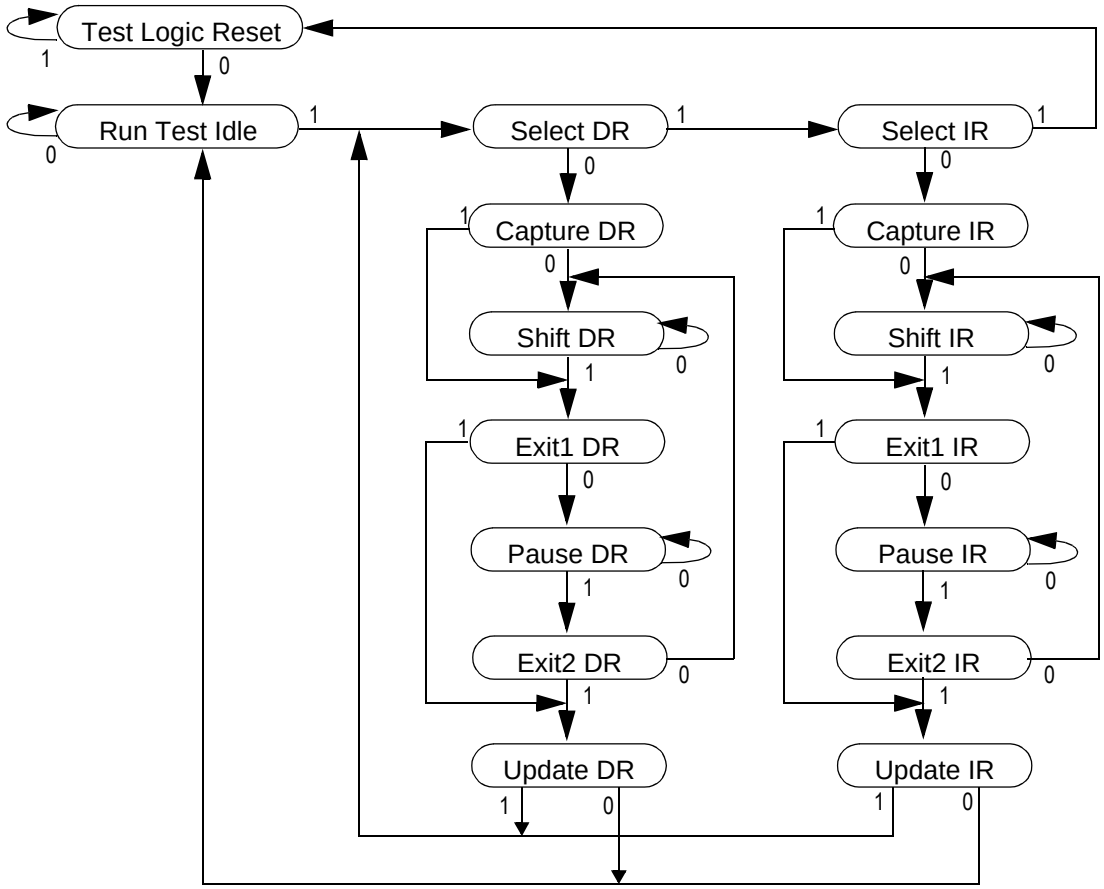
Tap Controller Instruction Set

Overview

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions, are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1-compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers.This device will not perform EXTEST, INTEST or the SAMPLE/PRELOAD command.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

JTAG Tap Controller State Diagram



Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE/PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time (tTS plus tTH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the

TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the Update-DR state with the SAMPLE / PRELOAD instruction loaded in the Instruction Register has the same effect as the Pause-DR command. This functionality is not Standard 1149.1-compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore, this device is not 1149.1-compliant. Nevertheless, this RAM's TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the BYPASS instruction described above.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

RFU

These instructions are Reserved for Future Use. In this device they replicate the BYPASS instruction.

JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST	000	Replicates BYPASS instruction. Places Bypass Register between TDI and TDO. This RAM does not implement 1149.1 EXTEST function. *Not 1149.1 Compliant *	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.	1
RFU	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. This RAM does not implement 1149.1 PRELOAD function. *Not 1149.1 Compliant *	1
GSI	101	GSI private instruction.	1
RFU	110	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

Notes:
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

JTAG Port Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
Test Port Input High Voltage	V_{IHT}	1.7	V_{DD} +0.3	V	1, 2
Test Port Input Low Voltage	V_{ILT}	–0.3	0.8	V	1, 2
TMS, TCK and TDI Input Leakage Current	I_{INTH}	–300	1	uA	3
TMS, TCK and TDI Input Leakage Current	I_{INTL}	–1	1	uA	4
TDO Output Leakage Current	I_{OLT}	–1	1	uA	5
Test Port Output High Voltage	V_{OHT}	2.4	—	V	6, 7
Test Port Output Low Voltage	V_{OLT}	—	0.4	V	6, 8

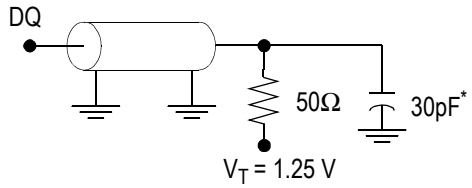
Notes:
1. This device features input buffers compatible with both 3.3 V and 2.5 V I/O drivers.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DD} +2 V with a pulse width not to exceed 20% tTKC.
3. $V_{DD} \geq V_{IN} \geq V_{IL}$
4. $0 V \leq V_{IN} \leq V_{IL}$
5. Output Disable, V_{OUT} = 0 to V_{DD}
6. The TDO output driver is served by the V_{DD} supply.
7. I_{OH} = –4 mA
8. I_{OL} = +4 mA

JTAG Port AC Test Conditions

Parameter	Conditions
Input high level	2.3 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	1.25 V
Output reference level	1.25 V

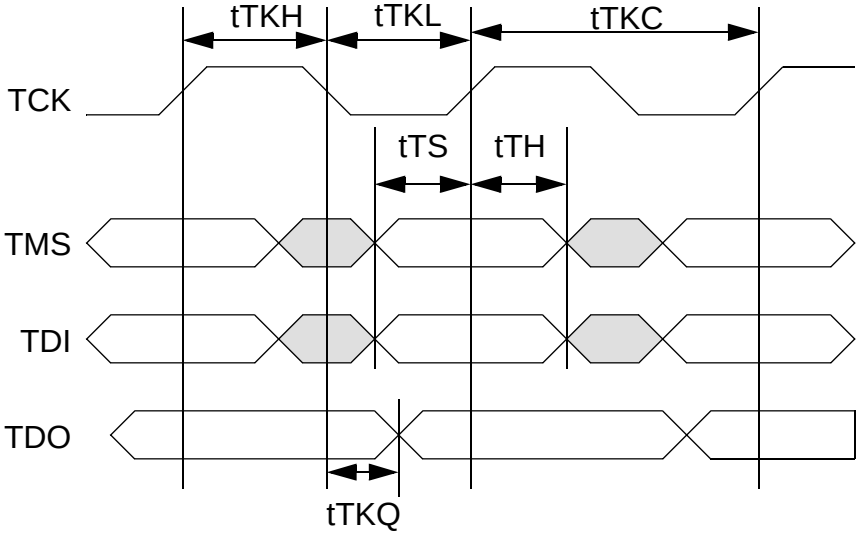
Notes:
1. Include scope and jig capacitance.

JTAG Port AC Test Load



* Distributed Test Jig Capacitance

JTAG Port Timing Diagram



JTAG Port AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	tTKC	20	—	ns
TCK Low to TDO Valid	tTKQ	—	10	ns
TCK High Pulse Width	tTKH	10	—	ns
TCK Low Pulse Width	tTKL	10	—	ns
TDI & TMS Set Up Time	tTS	5	—	ns
TDI & TMS Hold Time	tTH	5	—	ns

GS88218/36B BGA Boundary Scan Register

Order	x36	x18	Bump x36	Bump x18
1	$\overline{PE}$		7R	
2	PH = 0		n/a	
3	A_{10}		3T	2T
4	A_{11}		4T	3T
5	A_{12}		5T	
6	A_{13}		6R	
7	A_{14}		5C	
8	A_{15}		5B	
9	A_{16}		6C	
10	x36 = DQ_{A9} x32 = NA = 0	NC = 1	6P	
11	DQ_{A8}	NC = 1	7N	
12	DQ_{A4}	NC = 1	6M	
13	DQ_{A3}	NC = 1	7L	
14	DQ_{A7}	NC = 1	6K	
15	DQ_{A6}	DQ_{A1}	7P	
16	DQ_{A5}	DQ_{A2}	6N	
17	DQ_{A2}	DQ_{A3}	6L	
18	DQ_{A1}	DQ_{A4}	7K	
19	$\overline{ZZ}$		7T	
20	$\overline{QE}$		5J	
21	DQ_{B5}	DQ_{A5}	6H	
22	DQ_{B1}	DQ_{A6}	7G	
23	DQ_{B2}	DQ_{A7}	6F	
24	DQ_{B6}	DQ_{A8}	7E	
25	DQ_{B3}	x18 = DQ_{A9} x16 = NA = 0	7H	6D
26	DQ_{B4}	NC = 1	6G	
27	DQ_{B7}	NC = 1	6E	
28	DQ_{B8}	NC = 1	7D	
29	x36 = DQ_{B9} x32 = NA = 0	A_{18}	6D	6T

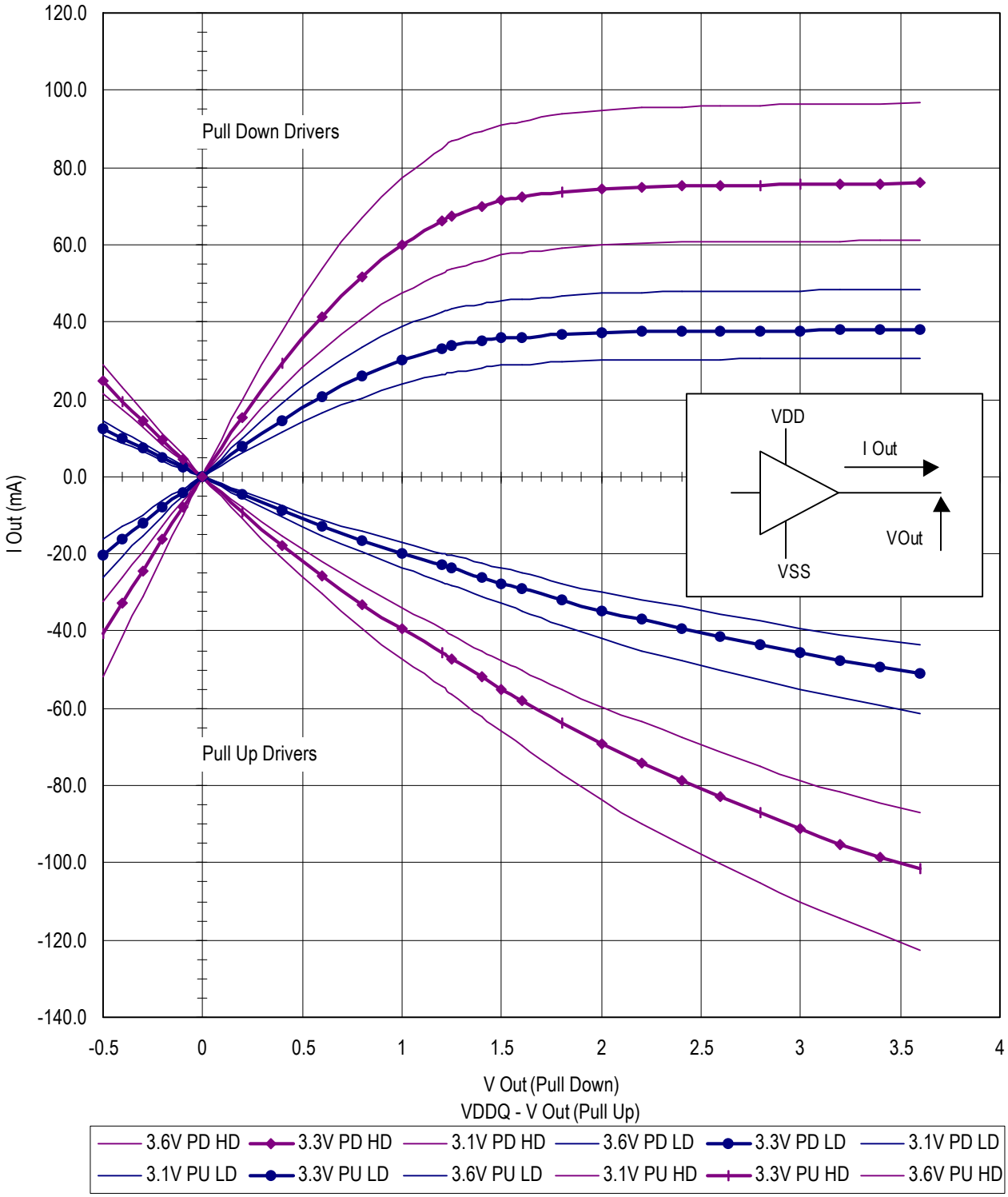
Order	x36	x18	Bump x36	Bump x18
30	A_9		6A	
31	A_8		5A	
32	$\overline{ADV}$		4G	
33	$\overline{ADSP}$		4A	
34	$\overline{ADSC}$		4B	
35	$\overline{G}$		4F	
36	$\overline{BW}$		4M	
37	$\overline{GW}$		4H	
38	CK		4K	
39	PH = 0		n/a	
40	PH = 0		n/a	
41	A_{17}		6B	
42	$\overline{B_A}$		5L	
43	$\overline{B_B}$	$\overline{B_B}$	5G	3G
44	$\overline{B_C}$	NC = 1	3G	5G
45	$\overline{B_D}$	NC = 1	3L	
46	CE_2		2B	
47	$\overline{CE_1}$		4E	
48	A_7		3A	
49	A_6		2A	
50	x36 = DQ_{C9} x32 = NA = 0	NC = 1	2D	
51	DQ_{C8}	NC = 1	1E	
52	DQ_{C4}	NC = 1	2F	
53	DQ_{C3}	NC = 1	1G	
54	DQ_{C7}	NC = 1	2H	
55	DQ_{C6}	DQ_{B1}	1D	
56	DQ_{C5}	DQ_{B2}	2E	
57	DQ_{C2}	DQ_{B3}	2G	
58	DQ_{C1}	DQ_{B4}	1H	
59	$\overline{FT}$		5R	

Order	x36	x18	Bump x36	Bump x18
60	DP		3J	
61	SCD		4L	
62	DQ_{D1}	DQ_{B5}	2K	
63	DQ_{D2}	DQ_{B6}	1L	
64	DQ_{D5}	DQ_{B7}	2M	
65	DQ_{D6}	DQ_{B8}	1N	
66	DQ_{D3}	x18 = DQ_{B9} x16 = NA = 0	1K	2P
67	DQ_{D4}	NC = 1	2L	
68	DQ_{D7}	NC = 1	2N	
69	DQ_{D8}	NC = 1	1P	
70	x36 = DQ_{D9} x32 = NA = 0	NC = 1	2P	1K
71	$\overline{LBO}$		3R	
72	A_5		2C	
73	A_4		3B	
74	A_3		3C	
75	A_2		2R	
76	A_1		4N	
77	A_0		4P	
78	ZQ		4D	

BPR 1999.08.11

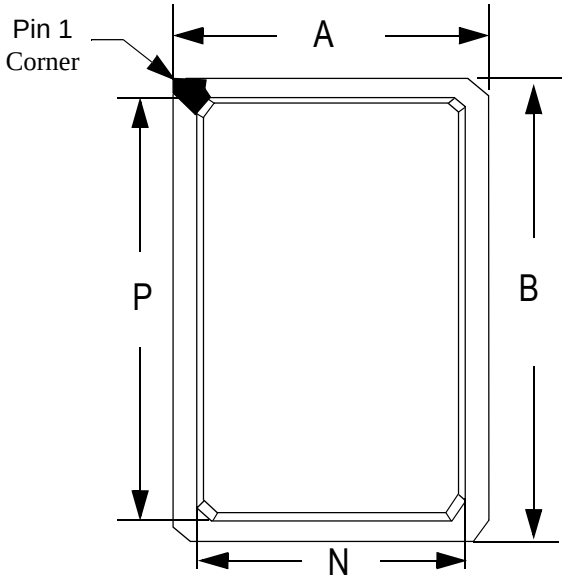
Note:
1. The Boundary Scan Register contains a number of registers that are not connected to any pin. They default to the value shown at reset.
2. Registers are listed in exit order (i.e., Location 1 is the first out of the TDO pin).
3. NC = No Connect, NA = Not Active

FLXDrive Output Driver Characteristics

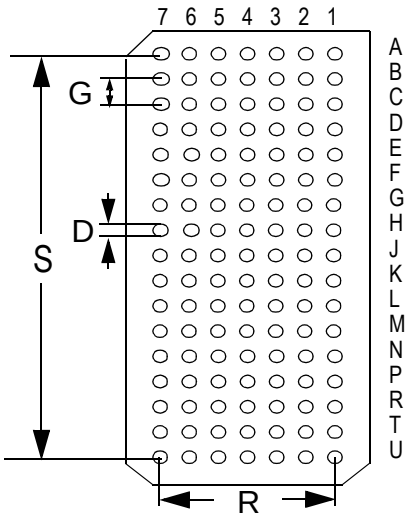


BPR 2000.02.14

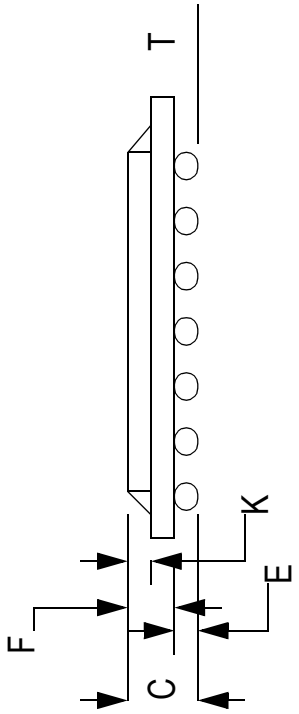
Package Dimensions—119 Pin BGA



Top View



Bottom View



Side View

Package Dimensions—119-Pin BGA

Symbol	Description	Min	Nom	Max
A	Width	13.8	14.0	14.2
B	Length	21.8	22.0	22.2
C	Package Height (including ball)	—	—	2.40
D	Ball Size	0.60	0.75	0.90
E	Ball Height	0.50	0.60	0.70
F	Package Height (excluding balls)	—	1.46	1.70
G	Width between Balls	—	1.27	—
K	Package Height above board	0.80	0.90	1.00
N	Cut-out Package Width	—	12.00	—
P	Foot Length	—	19.50	—
R	Width of package between balls	—	7.62	—
S	Length of package between balls	—	20.32	—
T	Variance of Ball Height	—	0.15	—

Unit: mm

BPR 1999.05.18

Ordering Information for GSI Synchronous Burst RAMs

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A[3]	Status
514K x 18	GS88218B-11	ByteSafe S/DCD Pipeline/Flow Through	BGA	100/11	C	
514K x 18	GS88218B-11.5	ByteSafe S/DCD Pipeline/Flow Through	BGA	100/11.5	C	
514K x 18	GS88218B-100	ByteSafe S/DCD Pipeline/Flow Through	BGA	100/12	C	
514K x 18	GS88218B-80	ByteSafe S/DCD Pipeline/Flow Through	BGA	80/14	C	
514K x 18	GS88218B-66	ByteSafe S/DCD Pipeline/Flow Through	BGA	66/18	C	
256K x 36	GS88236B-11	ByteSafe S/DCD Pipeline/Flow Through	BGA	100/11	C	
256K x 36	GS88236B-11.5	ByteSafe S/DCD Pipeline/Flow Through	BGA	100/11.5	C	
256K x 36	GS88236B-100	ByteSafe S/DCD Pipeline/Flow Through	BGA	100/12	C	
256K x 36	GS88236B-80	ByteSafe S/DCD Pipeline/Flow Through	BGA	80/14	C	
256K x 36	GS88236B-66	ByteSafe S/DCD Pipeline/Flow Through	BGA	66/18	C	
514K x 18	GS88218B-11I	ByteSafe S/DCD Pipeline/Flow Through	BGA	100/11	I	
514K x 18	GS88218B-11.5I	ByteSafe S/DCD Pipeline/Flow Through	BGA	100/11.5	I	
514K x 18	GS88218B-100I	ByteSafe S/DCD Pipeline/Flow Through	BGA	100/12	I	
514K x 18	GS88218B-80I	ByteSafe S/DCD Pipeline/Flow Through	BGA	80/14	I	
514K x 18	GS88218B-66I	ByteSafe S/DCD Pipeline/Flow Through	BGA	66/18	I	
256K x 36	GS88236B-11I	ByteSafe S/DCD Pipeline/Flow Through	BGA	100/11	I	
256K x 36	GS88236B-11.5I	ByteSafe S/DCD Pipeline/Flow Through	BGA	100/11.5	I	
256K x 36	GS88236B-100I	ByteSafe S/DCD Pipeline/Flow Through	BGA	100/12	I	
256K x 36	GS88236B-80I	ByteSafe S/DCD Pipeline/Flow Through	BGA	80/14	I	
256K x 36	GS88236B-66I	ByteSafe S/DCD Pipeline/Flow Through	BGA	66/18	I	

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS88218BT.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
3. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings.

8M Synchronous Datasheet Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
GS88218/36B Rev1.04h 5/ 1999; 1.05 9/1999I	Format/Typos	• Last Page/Fixed “GSGS..” in Ordering Information Note. • Fromatted Pin Outs and Pin Description to new small caps. • Formatted Block diagrams to new small caps. • Formatted Timing Diagrams to new small caps. • Changed “Flow thru” to “Flow Through” in Timing Diagrams. • Boundary Scan Register/Formatted to new small caps.
	Content	• 5/Fixed pin description table to match pinouts. • Pin Description/Changed chip enables to match pins. • Pin Description/Took 4A out of NC x18 row. • Pin Description/Reversed 4P and 4N to be consistent with A0 and A1. • Pin Description?Changed 2H to 1H in x18 Data I/O’s. • Boundary Scan Register/Corrected sequence of Data I/O pins. • Boundary Scan Register?Minor corrections and comments invisible.
GS88218/36B1.05 9/ 1999I;1.06 11/1999J	Content	• Changed 4J to $\overline{VDD}$ in Pad out. • Changed 5J to $\overline{QE}$. • First Release of 880 F.
GS88218/36B1.06 11/ 1999J;1.07 11/1999K	content	• Changed Bump 3C to 4L on first page to correspond SCD pin in BGA pinout.
GS8821836 Rev 1.07 11/ 1999; GS8821836 Rev 1.08 3/2000	Content	• Changed speed bin to 150 - 80 $\overline{Mhz}$ • Correction on page 8. x32 Mode ($\overline{PE}$ = 0) Changed to ($\overline{PE}$ = 1) • Correction on page 9. x18/x36 Mode ($\overline{PE}$ = 1) Changed to ($\overline{PE}$ = 0)
GS88218/36B1.0 3/2000; GS88218/36B1.0 3/2000O;	Content	• Corrections to AC Electrical Characteristics Table -
GS88218/36B1.0 3/2000O; 88218_r1_10	Content	• Updated BSR table on page 37 (see order 39 & 60) • Updated ADSC, E1 and E2 on timing diagrams on pages 25, 26, & 29
88218_r1_10; 88218_r1_11	Content	• Updated diagrams on pages 8 & 9
88218_r1_11; 88218_r1_12	Content	• Updated BGA pin description to meet JEDEC standard

8M Synchronous Datasheet Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
88218_r1_12; 88218_r1_13	Content/Format	• Deleted 150 MHz references • Changed 133 MHz references to 11 ns • Changed 117 MHz references to 11.5 ns • Used 100 MHz Pipeline mode numbers for 11 ns and 11.5 ns • Added 66 MHz speed bin • Updated format to comply with Technical Publications standards
88218_r1_13; 88218_r1_14	Content	• Updated Capitance table—removed Input row and changed Output row to I/O
88218_r1_14; 88218_r1_15	Content	• Updated Synchronous Truth Table (deleted $\overline{E1}$ reference)

