Integrated Device Technology, Inc.

FAST CMOS OCTAL LATCHED TRANSCEIVER

IDT54/74FCT543/2543T/AT/CT/DT

FEATURES:

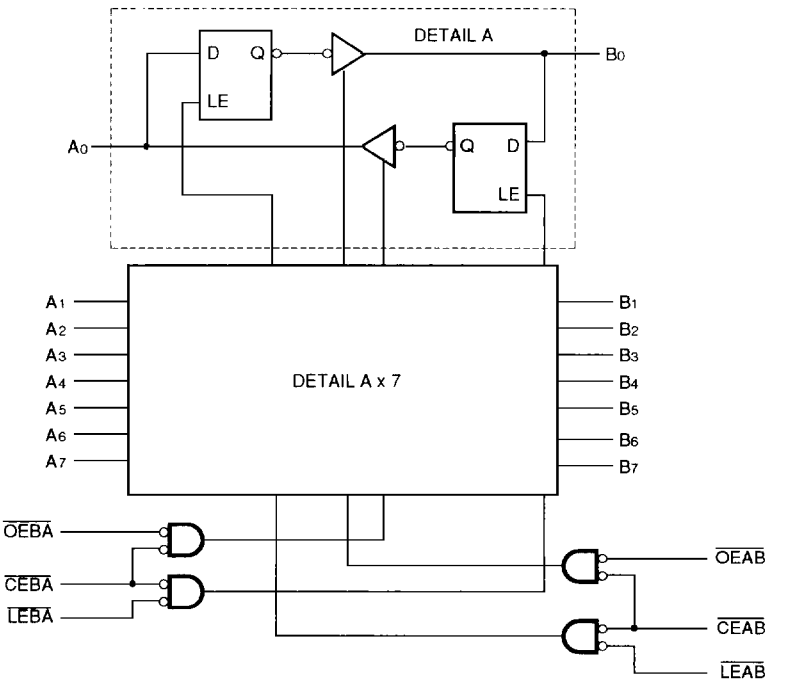
- **Common features:**
  - Std., A, C and D speed grades
  - Low input and output leakage ≤1μA (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - V_{OH} = 3.3V (typ.)
    - V_{OL} = 0.3V (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT543T/AT/CT/DT**
  - High drive outputs (-15mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
- **Features for FCT2543T/AT/CT/DT:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise

DESCRIPTION:

The IDT54/74FCT543T/AT/CT/DT are non-inverting octal transceivers built using an advanced dual metal CMOS technology. These devices contain two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0–A_7 or to take data from B_0–B_7, as indicated in the Function Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

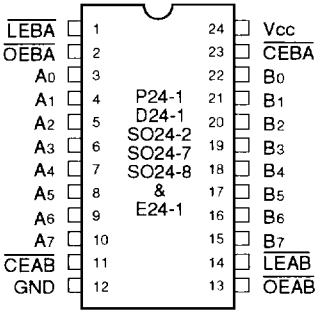
The IDT54/74FCT2543T/AT/CT/DT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. IDT54/74FCT2xxxT parts are plug-in replacements for IDT54/74FCTxxxT parts.

FUNCTIONAL BLOCK DIAGRAM



2613 drw 01

PIN CONFIGURATIONS



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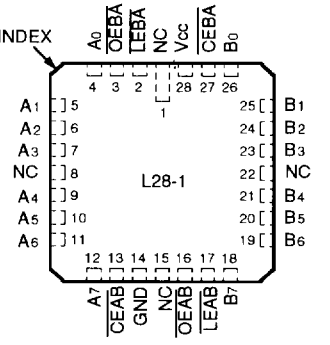
DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



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LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0–A_7	A-to-B Data Inputs or B-to-A 3-State Outputs
B_0–B_7	B-to-A Data Inputs or A-to-B 3-State Outputs

2613 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2613 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

FUNCTION TABLE(1, 2)

For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B_0–B_7
H	—	—	Storing	High Z
—	H	—	Storing	—
—	—	H	—	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

2613 tbl 02

NOTES:
1. * Before $\overline{LEAB}$ LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   — = Don't Care or Irrelevant
2. A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2613 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		−60	−120	−225	mA
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

2613 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR 543T/AT/CT/DT

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6mA MIL. I_{OH} = −8mA COM'L.	2.4	3.3	—	V
			I_{OH} = −12mA MIL. I_{OH} = −15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2613 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR 2543T/AT/CT/DT

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −16mA MIL. I_{OH} = −24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2613 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = −55°C.
5. This parameter is guaranteed but not tested.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	0.15	0.25	mA/ MHz
				FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	1.5	3.5	mA
				FCT2xxxT	—	0.6	2.2	
			V_{IN} = 3.4V V_{IN} = GND	FCTxxxT	—	2.0	5.5	
				FCT2xxxT	—	1.1	4.2	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	3.8	7.3[5]	
				FCT2xxxT	—	1.5	4.0[5]	
			V_{IN} = 3.4V V_{IN} = GND	FCTxxxT	—	6.0	16.3[5]	
				FCT2xxxT	—	3.8	13.0[5]	

2613 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT543T/ FCT2543T				FCT543AT/ FCT2543AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparant Mode An to Bn or Bn to An	CL = 50pF RL = 500Ω	1.5	8.5	1.5	10.0	1.5	6.5	1.5	7.5	ns
tPLH tPHL	Propagation Delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn		1.5	12.5	1.5	14.0	1.5	8.0	1.5	9.0	ns
tPZH tPZL	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		1.5	12.0	1.5	14.0	1.5	9.0	1.5	10.0	ns
tPHZ tPLZ	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		1.5	9.0	1.5	13.0	1.5	7.5	1.5	8.5	ns
tSU	Set-up Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		3.0	—	3.0	—	2.0	—	2.0	—	ns
tH	Hold Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW		5.0	—	5.0	—	5.0	—	5.0	—	ns

2513 tbl 09

Symbol	Parameter	Condition[1]	FCT543CT/ FCT2543CT				FCT543DT/ FCT2543DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparant Mode An to Bn or Bn to An	CL = 50pF RL = 500Ω	1.5	5.3	1.5	6.1	1.5	4.4	—	—	ns
tPLH tPHL	Propagation Delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn		1.5	7.0	1.5	8.0	1.5	5.0	—	—	ns
tPZH tPZL	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		1.5	8.0	1.5	9.0	1.5	5.4	—	—	ns
tPHZ tPLZ	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		1.5	6.5	1.5	7.5	1.5	4.3	—	—	ns
tSU	Set-up Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		2.0	—	2.0	—	1.5	—	—	—	ns
tH	Hold Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		2.0	—	2.0	—	1.5	—	—	—	ns
tW	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW		5.0	—	5.0	—	3.0[3]	—	—	—	ns

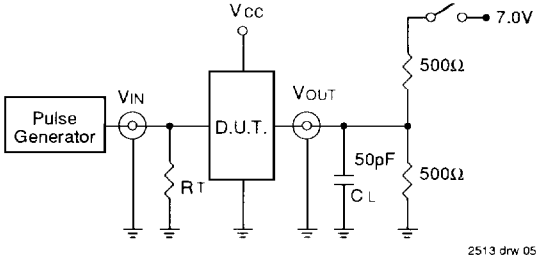
NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This limit is guaranteed but not tested.

2513 tbl 10

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2513 drw 05

SWITCH POSITION

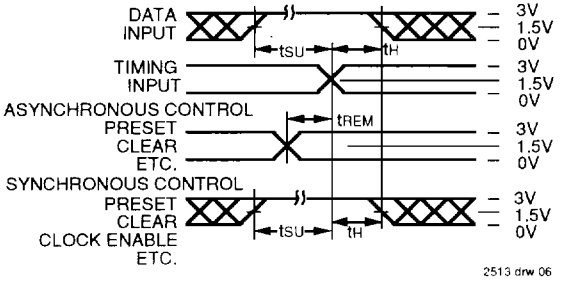
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2513 lnk 11

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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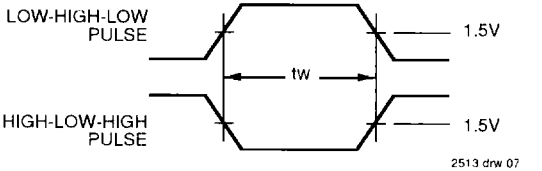
PULSE WIDTH



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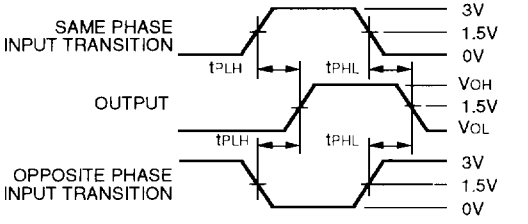
PROPAGATION DELAY



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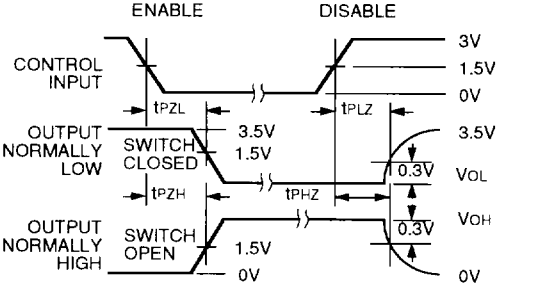
ENABLE AND DISABLE TIMES



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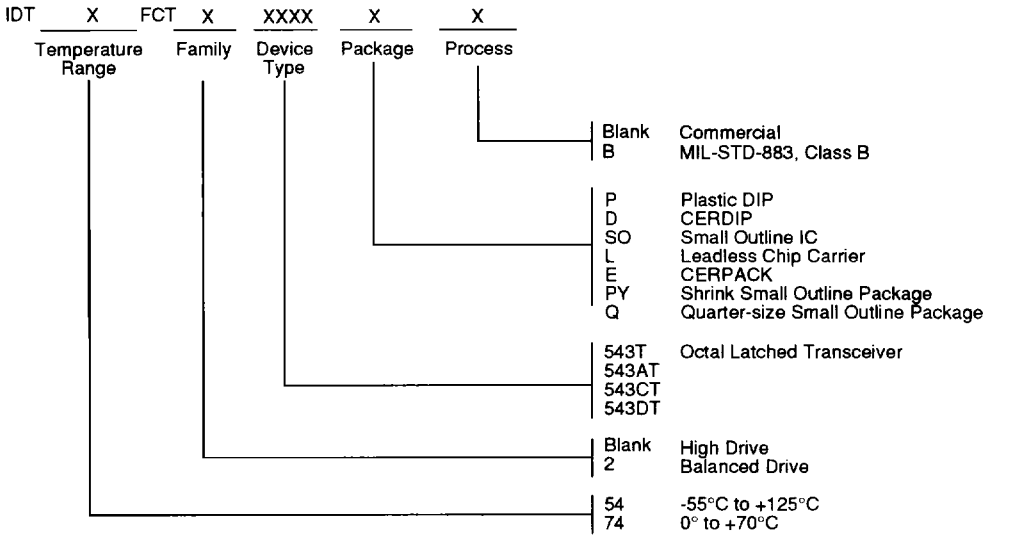
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2613 drw 10

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