FAST 74F550, 74F551

'F550 Octal Registered Transceiver With Status Flags, Non-Inverting
'F551 Octal Registered Transceiver With Status Flags, Inverting
Preliminary Specification

FAST Products

FEATURES

- **8-bit bidirectional I/O port with handshake**
- **Back-to-back registers for storage**
- **Register status flag flip-flops**
- **Separate edge-detecting clears for flags**
- **'F550 non-inverting 'F551 inverting**
- **B outputs sink 64mA**

DESCRIPTION

The 'F550 and 'F551 octal transceivers contain two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own Clock (CPA, CPB) and Clock Enable ($\overline{CEA}$, $\overline{CEB}$) inputs as well as a flag flip-flop that is set automatically as the register is loaded. Each flag flip-flop is provided with a clear input, and each register has a separate Output Enable ($\overline{OEA}$, $\overline{OEB}$) for its 3-State buffers. The separate Clocks, Flags and Enables provide considerable flexibility as I/O ports for demand-response data transfer. The 'F550 is non-inverting; the 'F551 inverts data in both directions.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F550	6.3ns	130mA
74F551	6.3ns	130mA

ORDERING INFORMATION

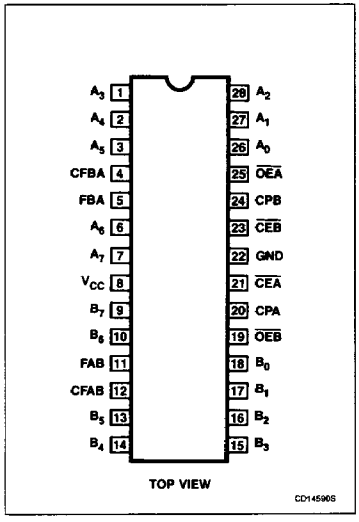
PACKAGE	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
28-Pin Plastic DIP	N74F550N, N74F551N
28-Pin Plastic SOL	N74F550D, N74F551D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

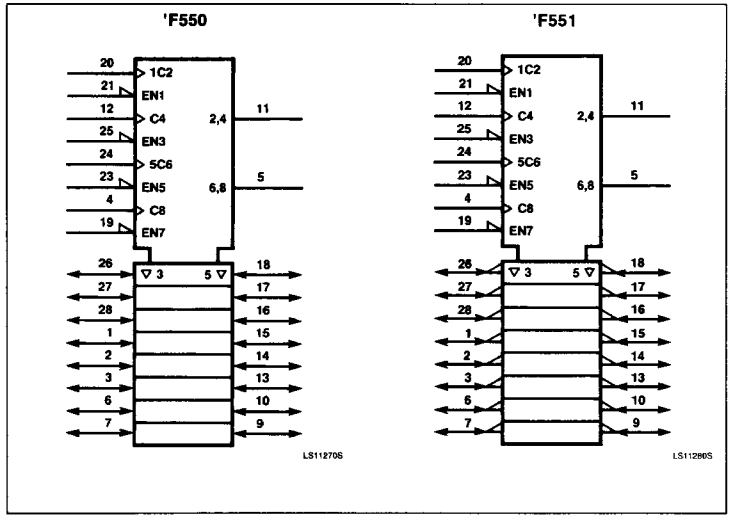
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	A-to-B Data inputs	3.5/1.0	70μA/0.6mA
$B_0 - B_7$	B-to-A Data inputs	3.5/1.0	70μA/0.6mA
CPA	A-to-B Clock input (active rising edge)	1.0/1.0	20μA/0.6mA
CPB	B-to-A Clock input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{CEA}$	A-to-B Clock Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{CEB}$	B-to-A Clock Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{OEA}$	A-to-B Output Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{OEB}$	B-to-A Output Enable input (active-Low)	1.0/1.0	20μA/0.6mA
CFAB	A-to-B Flag Clear input (active rising edge)	1.0/1.33	20μA/0.8mA
CFBA	B-to-A Flag Clear input (active rising edge)	1.0/1.33	20μA/0.8mA
$A_0 - A_7$	A-to-B Data outputs	150/40	3mA/24mA
$B_0 - B_7$	B-to-A Data outputs	150/40	3mA/24mA
FAB	A-to-B Status Flag output (active-High)	50/33.3	1mA/20mA
FBA	B-to-A Output Enable input (active-High)	50/33.3	1mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

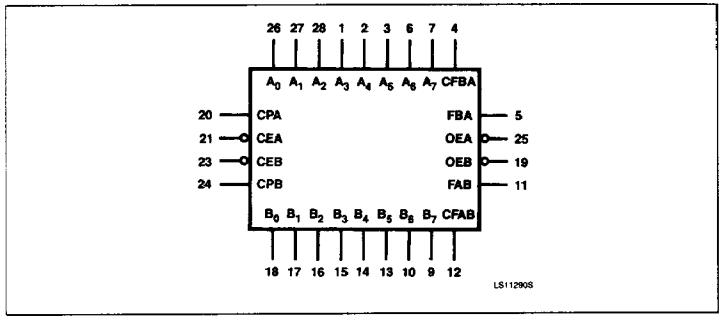
PIN CONFIGURATION



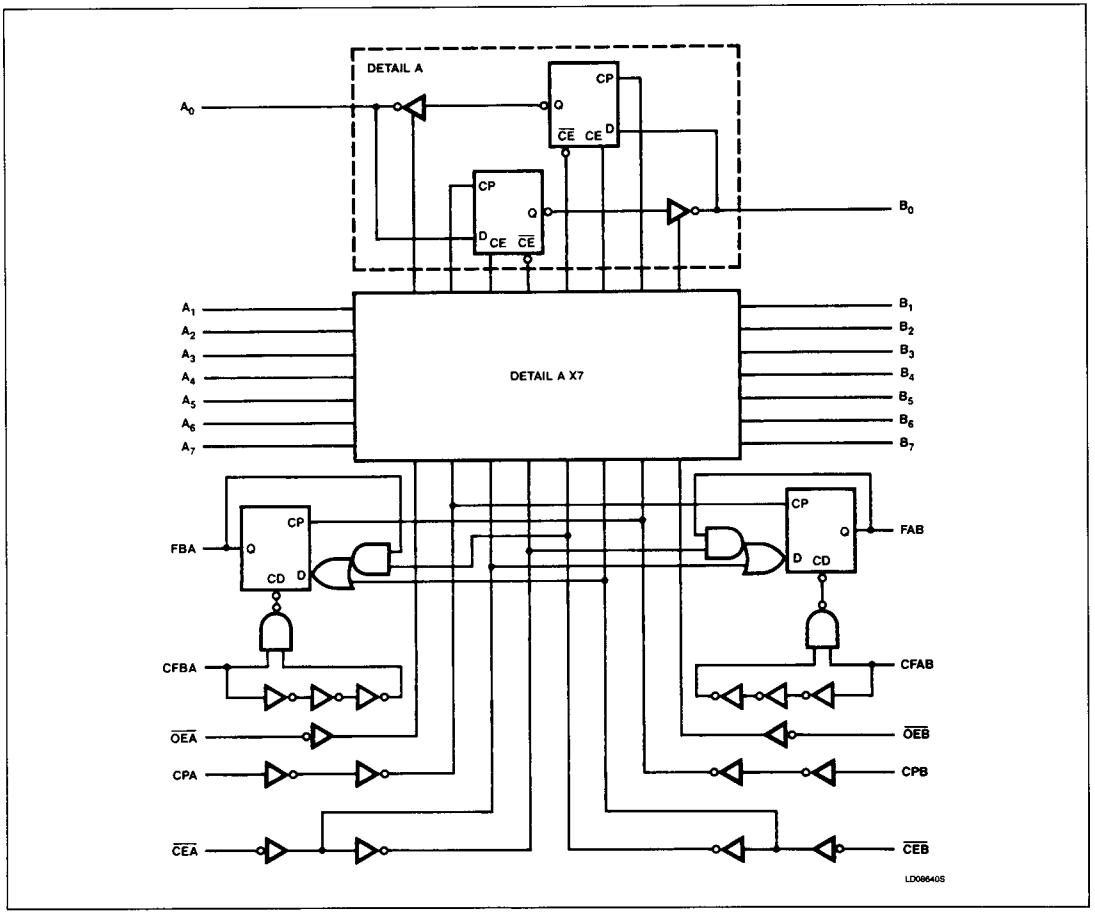
SYMBOL (IEEE/IEC)



LOGIC SYMBOL



LOGIC DIAGRAM for 'F550



FUNCTIONAL DESCRIPTION

Data applied to the A inputs are entered and stored on the rising edge of the A Clock (CPA), provided that the A Clock Enable ($\overline{CEA}$) is Low; simultaneously, the status flip-flop is set and the A-to-B Flag (FAB) output goes High. Data entered from the A inputs is present at the inputs to the B output buffers, but only appears on the B I/O pins when the B Output Enable ($\overline{OEB}$) signal is made Low. After the B output data is assimilated, the receiving system clears the A-to-B Flag flip-flop by applying a Low-to-High transition to the CFAB input. Optionally, the OEA and CFAB pins can be tied together and operated by one function from the receiving system.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. Inputs $\overline{CEB}$ and CPB enter the B input data and set the B-to-A Flag (FBA) output High. A Low signal on $\overline{OEA}$ enables the A output buffers and a Low-to-High transition on CFBA clears the FBA Flag.

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FUNCTION TABLE

OPERATING MODE	INPUTS			INTERNAL Q
	A or B	CP	$\overline{CE}$	
Hold data	X	X	H	No change
Load data	L H	↑ ↑	L L	L H

FLAG FUNCTION TABLE

OPERATING MODE	INPUTS			FLAG OUTPUT
	CF	CP	$\overline{CE}$	
Hold Flag	↕	X	H	No change
Clear Flag	↑	X	X	L
Set Flag	↕	↑	L	H

OUTPUT CONTROL TABLE

OPERATING MODE	$\overline{OE}$	INTERNAL Q	OUTPUT	
			'F550	'F551
Disable outputs	H	X	Z	Z
Enable outputs	L L	L H	L H	H L

H = High Voltage Level
L = Low Voltage Level
X = Don't care
Z = High-Impedance
↑ = Low-to-High Transition
↕ = Doesn't allow Low-to-High Transition

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	FAB, FBA	40	mA
		$A_0 - A_7$, $B_0 - B_7$	48	
T_A	Operating free-air temperature range		0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	V
I_{OH}	High-level output current	FAB, FBA			−1	mA
		$A_0 - A_7$, $B_0 - B_7$			−3	
I_{OL}	Low-level output current	FAB, FBA			20	mA
		$A_0 - A_7$, $B_0 - B_7$			24	
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F550, 74F551			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX I_{OH} = MAX, V_{IH} = MIN	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	Others	V_{CC} = MAX, V_I = 7.0V				100	µA
		$A_0 - A_7$, $B_0 - B_7$	V_{CC} = 5.5V, V_I = 5.5V				1.0	mA
I_{IH}	High-level input current	except $A_0 - A_7$, $B_0 - B_7$	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−600	µA
$I_{IH}+I_{OZH}$	High-level input current	$A_0 - A_7$, $B_0 - B_7$	V_{CC} = MAX, V_O = 2.7V				70	µA
$I_{IL}+I_{OZL}$	Low-level input current		V_{CC} = MAX, V_O = 0.5V				−600	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current		V_{CC} = MAX			130	190	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

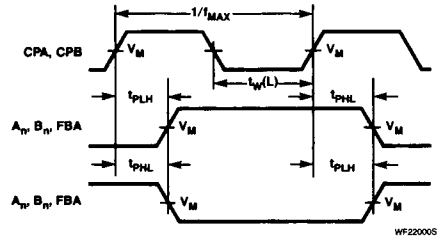
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F550, 74F551					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A=0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum operating frequency	Waveform 1	60	70		50		MHz
t_{PLH} t_{PHL}	Propagation delay CPA or CPB to B_n or A_n	Waveform 1	3.0 4.0	5.5 7.0	7.5 9.0	2.5 3.5	8.5 10.0	ns
t_{PLH}	Propagation delay CPA or CPB to FAB or FBA	Waveform 1	3.5	6.0	6.0	3.0	9.0	ns
t_{PHL}	Propagation delay CFAB or CFBA to FAB or FBA	Waveform 2	5.0	9.0	11.5	4.5	13.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	Waveform 4, 5	2.5 3.5	5.5 7.0	7.5 9.5	2.0 3.0	8.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	Waveform 4, 5	3.0 2.5	6.5 5.5	9.0 7.5	2.5 2.0	10.0 8.5	ns

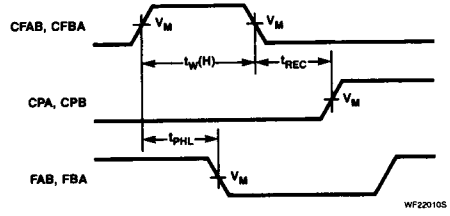
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F550, 74F551					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A=0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ CL = 50pF $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPA or CPB	Waveform 3	4.0 4.0			4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPA or CPB	Waveform 3	2.0 2.0			2.5 2.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	Waveform 3	4.0 4.0			4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	Waveform 3	2.0 2.0			2.5 2.5		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPA or CPB	Waveform 3	3.0 3.0			3.5 3.5		ns
$t_w(H)$	Pulse width, High CFAB or CFBA	Waveform 2	3.0			3.5		ns
t_{rec}	Recovery time CFAB or CFBA to CPA or CPB	Waveform 2	9.0			10.0		ns

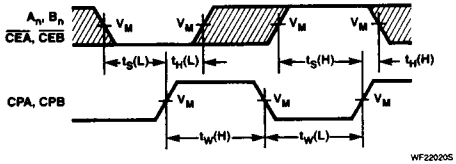
AC WAVEFORMS



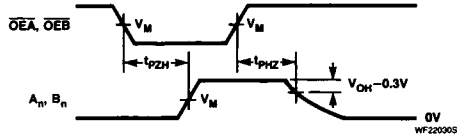
Waveform 1. Propagation Delay, Clock Input to Output



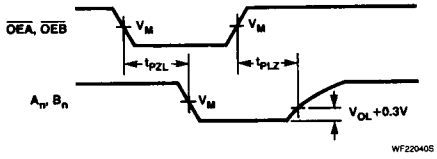
Waveform 2. Propagation Delay, Flag Clear Input to Status Flag Output, Recovery Time Flag Clear Input to Clock Output



Waveform 3. Data Setup Time and Hold Times, and Clock Pulse Widths



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: $V_M = 1.5V$.
The shaded area indicate when the input is permitted to change for predictable output performance.

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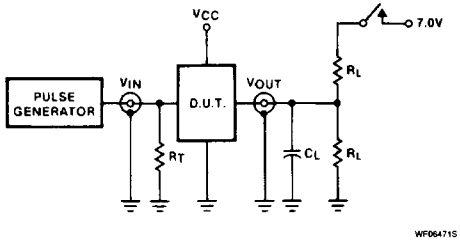
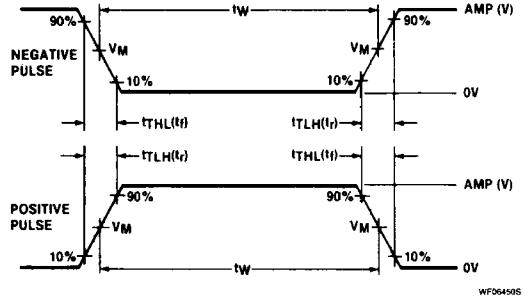
TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.