Signetics

Document No.	853-1097
ECN No.	97708
Date of issue	September 22, 1989
Status	Product Specification
FAST Products	

FAST 74F2952, 74F2953 Transceivers

74F2952 Registered Transceiver, Non-Inverting (3-State)
74F2953 Registered Transceiver, Inverting (3-State)

FEATURES

- **8-bit Registered Transceivers**
- **Two 8-bit , back-to-back registers store data moving in both directions between two bidirectional busses**
- **Separate Clock, Clock Enable and 3-state Enable provided for each register**
- **'F2952 Non-inverting 'F2953 Inverting**
- **AM2952/2953 functional equivalent**
- **A outputs sink 24mA and source 3mA**
- **B outputs sink 64mA and source 15mA**
- **300 mil wide 24-pin Slim DIP package**

DESCRIPTION

The 74F2952 and 74F2953 are 8-bit Registered Transceivers. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-state output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F2952	160MHz	105mA
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ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F2952N, N74F2953N
24-Pin Plastic SOL[1]	N74F2952D, N74F2953D
28-Pin Plastic PLCC	N74F2952A, N74F2953A

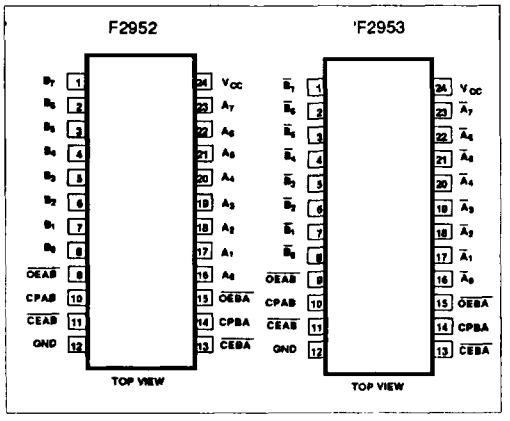
NOTE:
1.Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

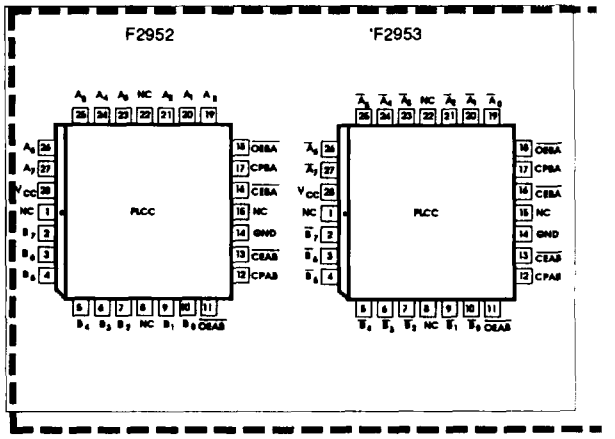
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	Port A, 3-state inputs	3.5/1.0	70µA/0.6mA
B_0 - B_7	Port B, 3-state inputs	3.5/1.0	70µA/0.6mA
CPAB,CPBA	Clock inputs	1.0/1.0	20µA/0.6mA
$\overline{CEAB}$,$\overline{CEBA}$	Clock Enable inputs	1.0/1.0	20µA/0.6mA
$\overline{OEAB}$,$\overline{OEBA}$	Output Enable inputs	1.0/1.0	20µA/0.6mA
A_0 - A_7	Port A, 3-state outputs	150/40	3.0mA/24mA
B_0 - B_7	Port B, 3-state outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

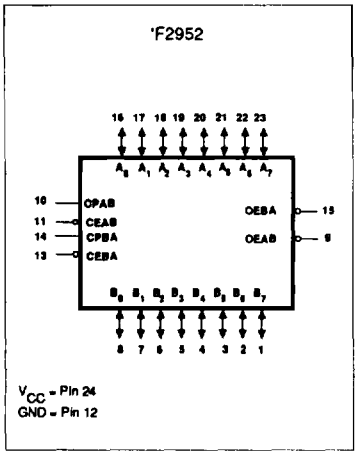
PIN CONFIGURATION DIP



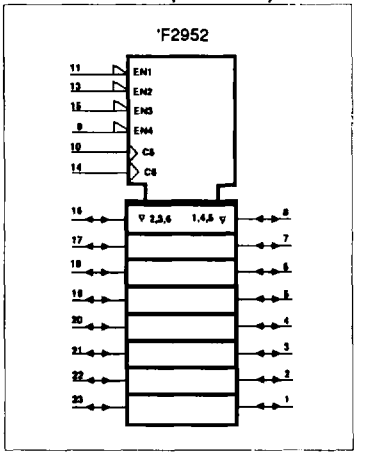
PIN CONFIGURATION PLCC



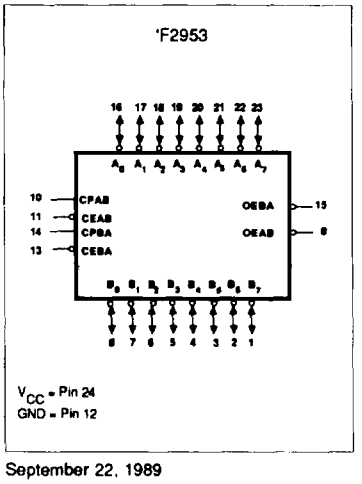
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)