

1M x 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	t _{TRAC}	t _{CAC}	t _{TRC}
KM416C1200A-6/A-L6/A-F6	60ns	15ns	110ns
KM416C1200A-7/A-L7/A-F7	70ns	20ns	130ns
KM416C1200A-8/A-L8/A-F8	80ns	20ns	150ns

- Fast Page Mode operation
- 2 CAS Byte/Word Read/Write operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Triple +5V ± 10% power supply
- Refresh Cycle
 - 1024 cycles/16ms (Normal)
 - 1024 cycles/128ms (L-version)
 - 1024 cycles/128ms (F-version)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages

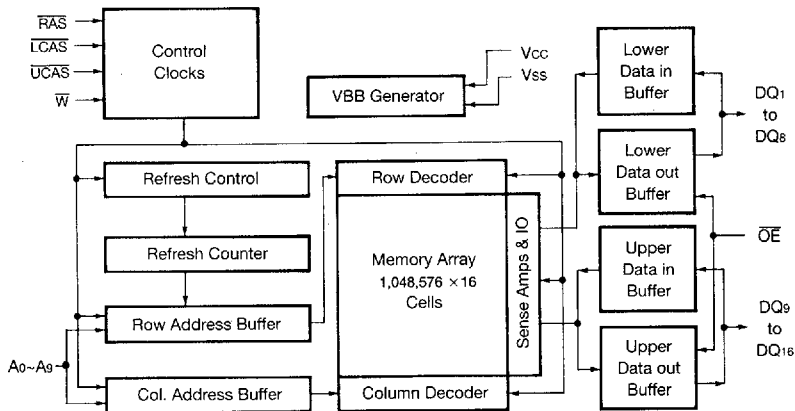
GENERAL DESCRIPTION

The Samsung KM416C1200A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

The KM416C1200A/A-L/A-F features Fast Page Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

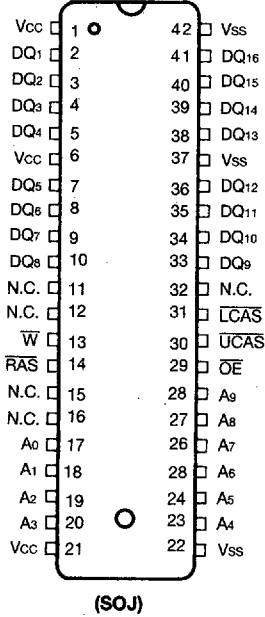
The KM416C1200A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

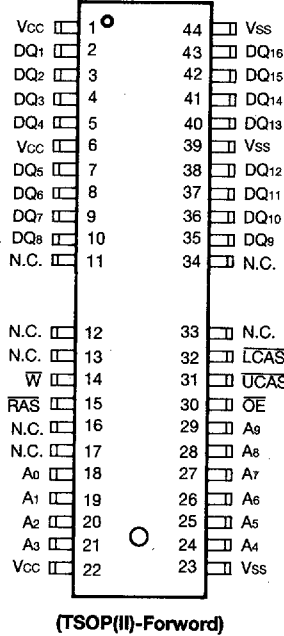


PIN CONFIGURATION (Top Views)

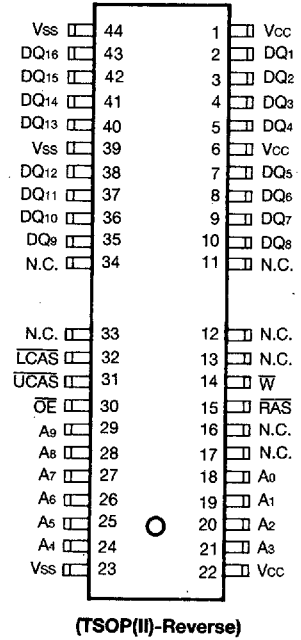
• KM416C1200AJ



• KM416C1200AT



• KM416C1200AR



Pin Name	Pin Function
A0-A9	Address Inputs
DQ1-16	Data In/Out
Vss	Ground
\overline{RAS}	Row Address Strobe
\overline{UCAS}	Upper Column Address Strobe
\overline{LCAS}	Lower Column Address Strobe
\overline{W}	Read/Write Input
\overline{OE}	Data Output Enable
Vcc	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 ~ + 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-1 ~ + 7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _d	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	Vcc + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS, UCAS or LCAS, Address Cycling @trc=min.)	KM416C1200A-6/A-L6/A-F6 KM416C1200A-7/A-L7/A-F7 KM416C1200A-8/A-L8/A-F8 Icc1	-	160 150 140	mA mA mA
Standby Current (RAS=UCAS=LCAS=W=V _{IH})	KM416C1200A KM416C1200A-L KM416C1200A-F Icc2	-	2 1 1	mA mA mA
RAS-Only Refresh Current* (UCAS=LCAS=V _{IH} , RAS, Address Cycling @trc=min.)	KM416C1200A-6/A-L6/A-F6 KM416C1200A-7/A-L7/A-F7 KM416C1200A-8/A-L8/A-F8 Icc3	-	160 150 140	mA mA mA
Fast Page Mode Current* (RAS=V _{IL} , UCAS or LCAS, Address Cycling @trc=min.)	KM416C1200A-6/A-L6/A-F6 KM416C1200A-7/A-L7/A-F7 KM416C1200A-8/A-L8/A-F8 Icc4	-	110 100 90	mA mA mA
Standby Current (RAS=UCAS=LCAS=W=Vcc-0.2V)	KM416C1200A KM416C1200A-L KM416C1200A-F Icc5	-	1 300 200	mA μA μA
CAS-Before-RAS Refresh Current* (RAS, UCAS or LCAS Cycling @trc=min.)	KM416C1200A-6/A-L6/A-F6 KM416C1200A-7/A-L7/A-F7 KM416C1200A-8/A-L8/A-F8 Icc6	-	160 150 140	mA mA mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V _{IH})=Vcc-0.2V, input Low Voltage(V _{IL})=0.2V UCAS, LCAS=0.2V DIN=Don't Care, trc=125μs (L-Version) tRAS=tRAS min-300ns	KM416C1200A-L Icc7	-	350	μA

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DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=UCAS=LCAS=0.2V W=OE=A0-A9=Vcc-0.2V or 0.2V DQ1-DQ16=Vcc-0.2V, 0.2V or Open	Iccs	-	250	μA
Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test=0V)	II(L)	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ VOUT ≤ Vcc)	IO(L)	-10	10	μA
Output High Voltage Level (IOH=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)	VOL	-	0.4	V

*NOTE: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, address can be changed maximum once while RAS=VIL. In Icc4, Address can be changed maximum once while page mode cycle time tpc.

CAPACITANCE (TA=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A9)	CIN1	-	5	pF
Input Capacitance (RAS, LCAS, UCAS, W, OE)	CIN2	-	7	pF
Output Capacitance (DQ1~DQ16)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, Vcc=5.0V ± 10%, See notes 1,2)

(Test condition : VIH/VIL=2.4V/0.8V, VOH/VOL=2.4V/0.4V, Output Loading CL=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	110		130		150		ns	
Read-modify-write cycle time	trwc	155		185		205		ns	
Access time from RAS	trac		60		70		80	ns	3,4,11
Access time from CAS	tcac		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
CAS to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	toff	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
RAS precharge time	trp	40		50		60		ns	
RAS pulse width	trAS	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	trSH	15		20		20		ns	
CAS hold time	tcSH	60		70		80		ns	
CAS pulse width	tcAS	15	10,000	20	10,000	20	10,000	ns	
RAS to CAS delay time	trCD	20	45	20	50	20	60	ns	4
RAS to column address delay time	trAD	15	30	15	35	15	40	ns	11



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
CAS to RAS precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to RAS	tAR	45		55		60		ns	6
Column address to RAS lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to CAS	tRCH	0		0		0		ns	9
Read command hold time referenced to RAS	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to RAS	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		15		20		ns	
Write command to CAS lead time	tCWL	15		15		20		ns	
Data-in set-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	10		15		15		ns	10
Data-in hold time referenced to RAS	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
CAS to W delay time	tCWD	40		50		50		ns	8
RAS to W delay time	tRWD	85		95		105		ns	8
Column address to W delay time	tAWD	55		60		65		ns	8
CAS precharge to W delay time	tCPWD	60		65		70		ns	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		ns	
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		10		ns	
RAS precharge to CAS hold time	tRPC	5		5		5		ns	
CAS precharge time (C-B-R counter test cycle)	tCPT	20		25		30		ns	
Access time from CAS precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		95		100		ns	
RAS pulse width (Fast page mode)	tRASP	60	200K	70	200K	80	200K	ns	
RAS hold time from CAS precharge	tRHCP	35		40		45		ns	
CAS precharge time (Fast page mode)	tCP	10		10		10		ns	
RAS hold time referenced to OE	tROH	15		20		20		ns	

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AC CHARACTERISTICS (Continued)

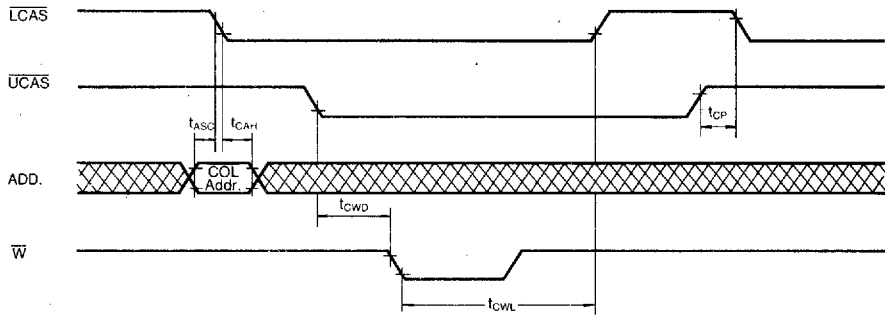
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
\overline{OE} access time	toEA		15		20		20	ns	
\overline{OE} to data delay	toED	15		20		20		ns	
Output buffer turn off delay time from \overline{OE}	toEZ	0	15	0	20	0	20	ns	
\overline{OE} command hold time	toEH	15		20		20		ns	
RAS pulse width (F-ver)	trASS	100		100		100		μ s	19
RAS precharge time (F-ver)	trPS	110		130		150		ns	19
CAS hold time (F-ver)	tCHS	-50		-50		-50		ns	19

KM416C1200A/A-L/A-F Truth Table

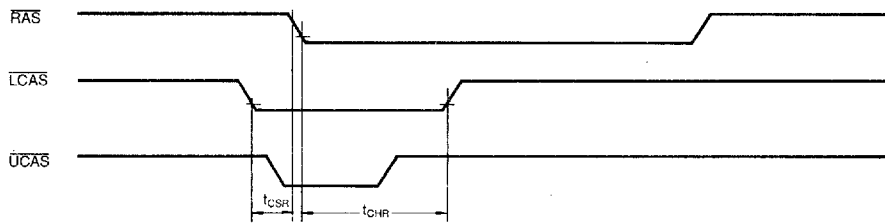
RAS	LCAS	UCAS	\overline{W}	\overline{OE}	DQ1-DQ8	DQ9-DQ16	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

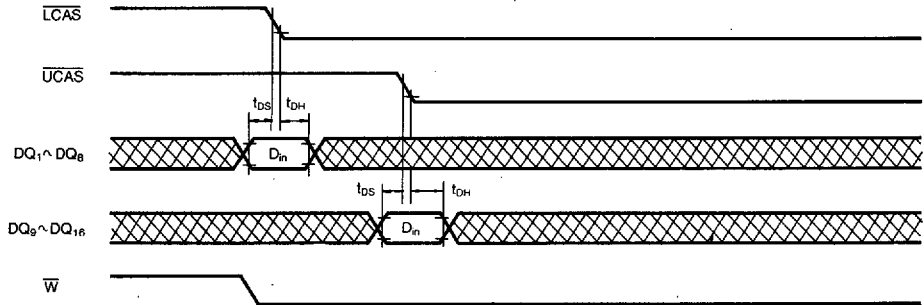
1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(\min)}$ and $V_{IL(\max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(\min)}$ and $V_{IL(\max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{\text{RCD}(\max)}$ limit insures that $t_{\text{RAC}(\max)}$ can be met. $t_{\text{RCD}(\max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}(\max)}$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}(\max)}$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{\text{RAD}(\max)}$.
7. $t_{\text{OFF}(\max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating aparameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}(\min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}(\min)}$, $t_{\text{RWD}} \geq t_{\text{RWD}(\min)}$, $t_{\text{AWD}} \geq t_{\text{AWD}(\min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the $t_{\text{RAD}(\max)}$ limit insures that $t_{\text{RAC}(\max)}$ can be met. $t_{\text{RAD}(\max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}(\max)}$ limit, then access time is controlled by t_{AA} .
12. t_{ASC} , t_{CAH} are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
13. t_{CP} is specified from the last $\overline{\text{CAS}}$ rising edge in the previous cycle to the first $\overline{\text{CAS}}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{\text{W}}$ falling edge to the earlier $\overline{\text{CAS}}$ rising edge.



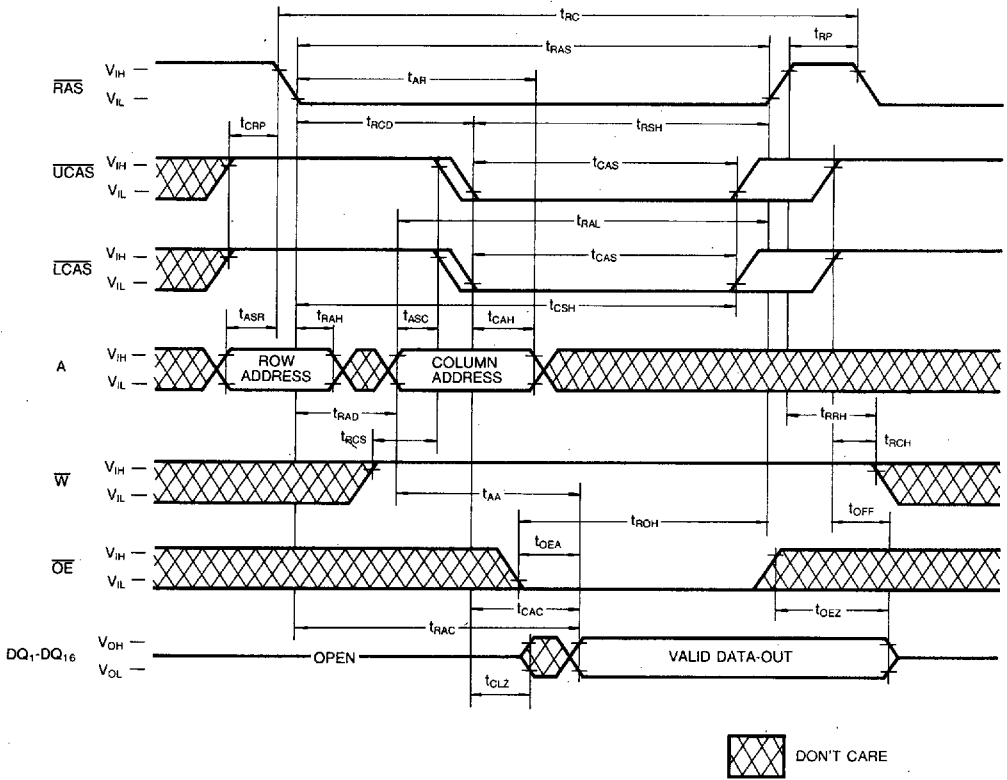
16. t_{CSR} is referenced to earlier $\overline{\text{CAS}}$ falling low before $\overline{\text{RAS}}$ transition low.
17. t_{CHR} is referenced to the later $\overline{\text{CAS}}$ rising high after $\overline{\text{RAS}}$ transition low.



18. t_{DS} , t_{DH} is independently specified for lower byte $D_{in(1\sim8)}$, upper byte $D_{in(9\sim16)}$

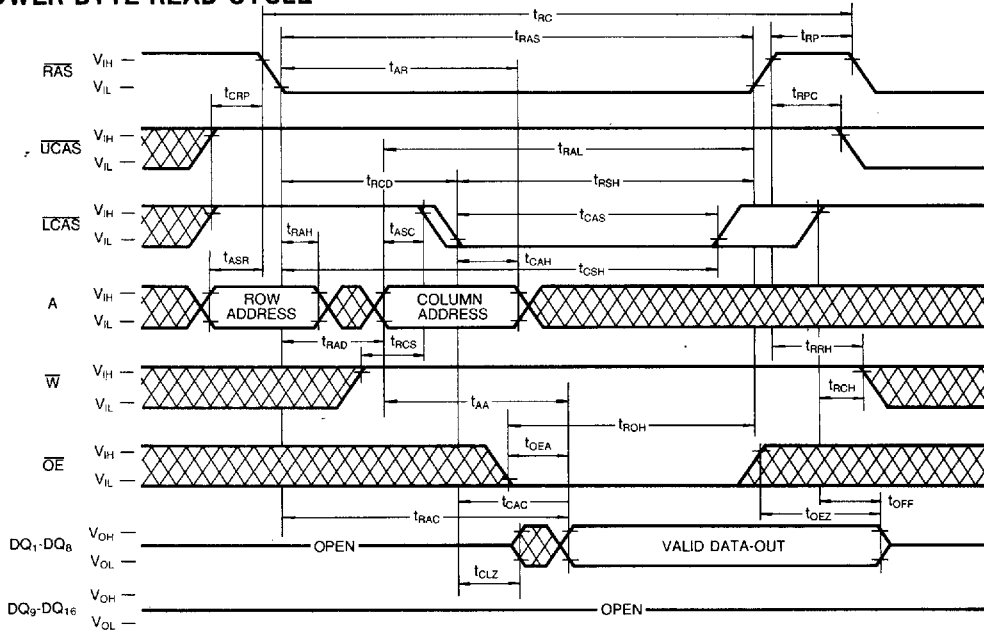


TIMING DIAGRAMS
WORD READ CYCLE

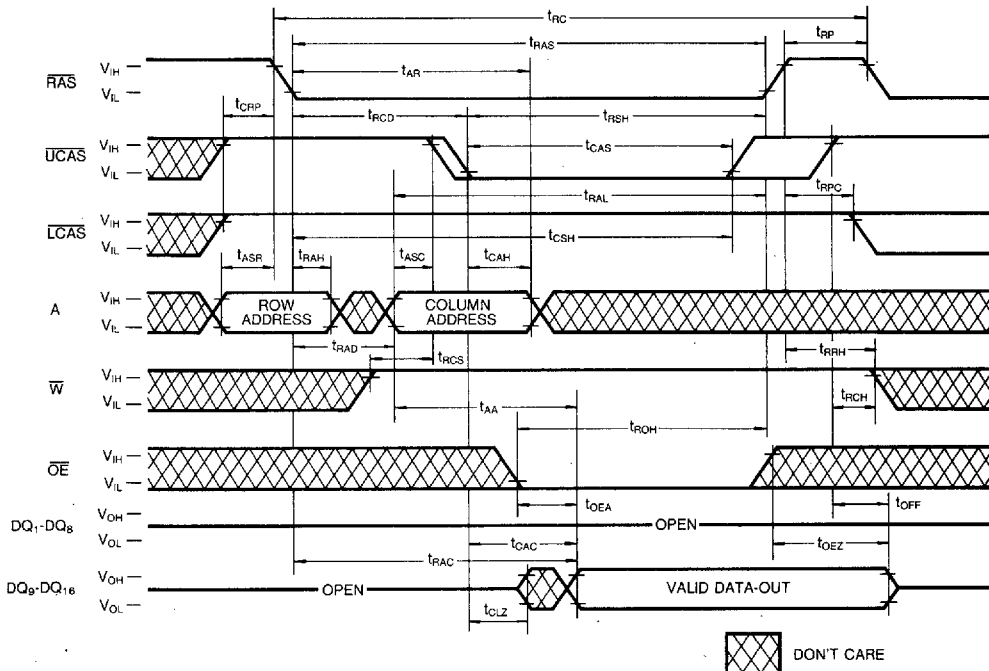


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE



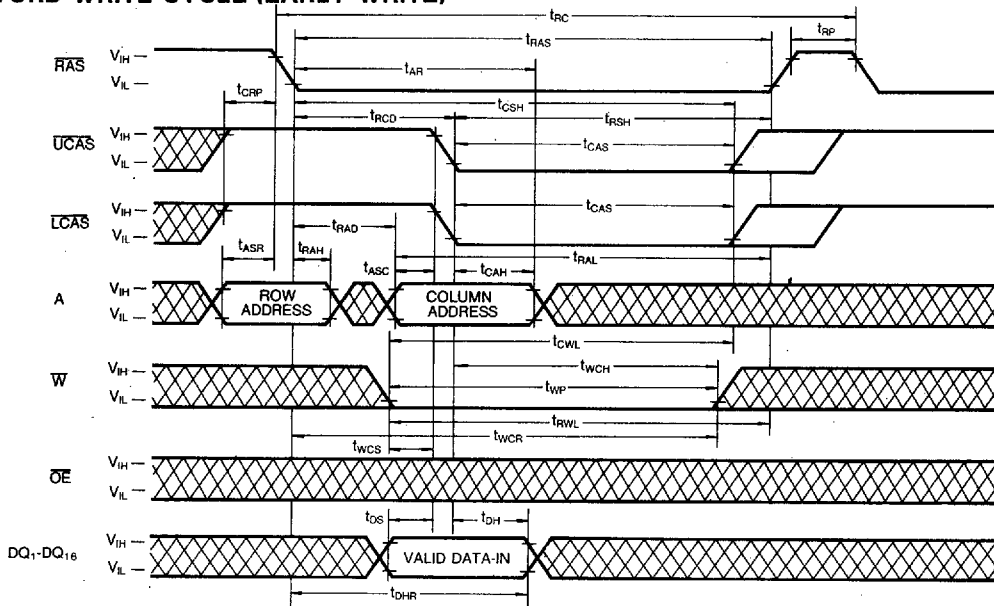
UPPER BYTE READ CYCLE



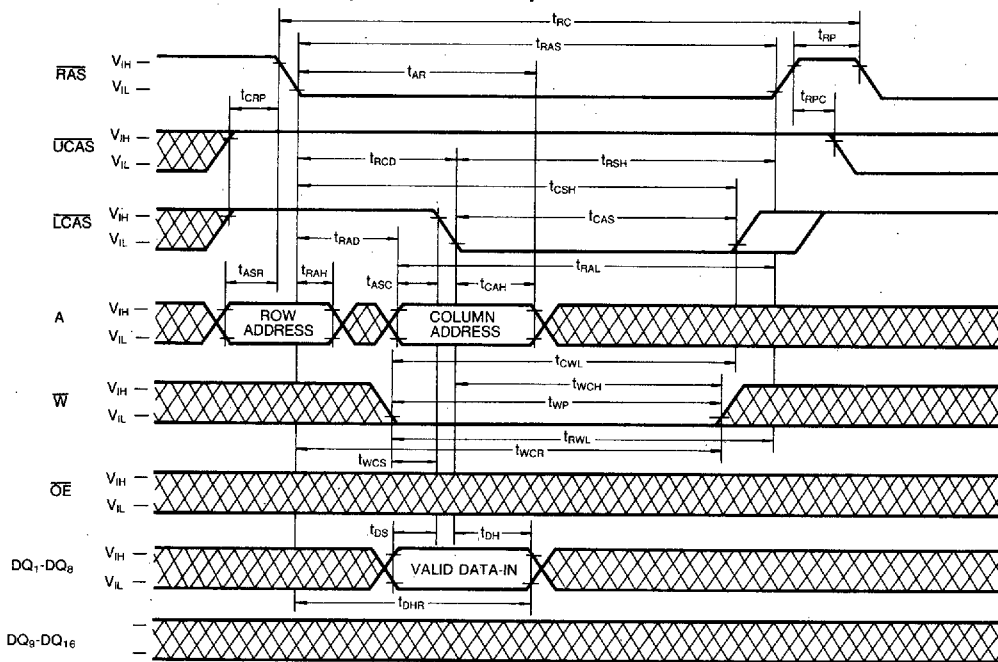
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
TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)



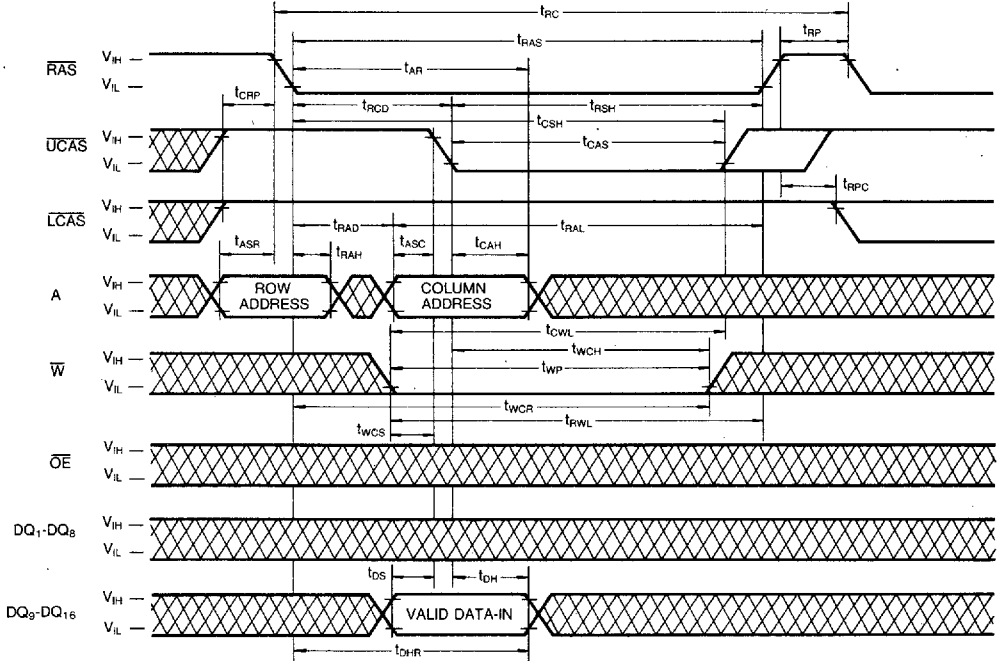
LOWER BYTE WRITE CYCLE (EARLY WRITE)



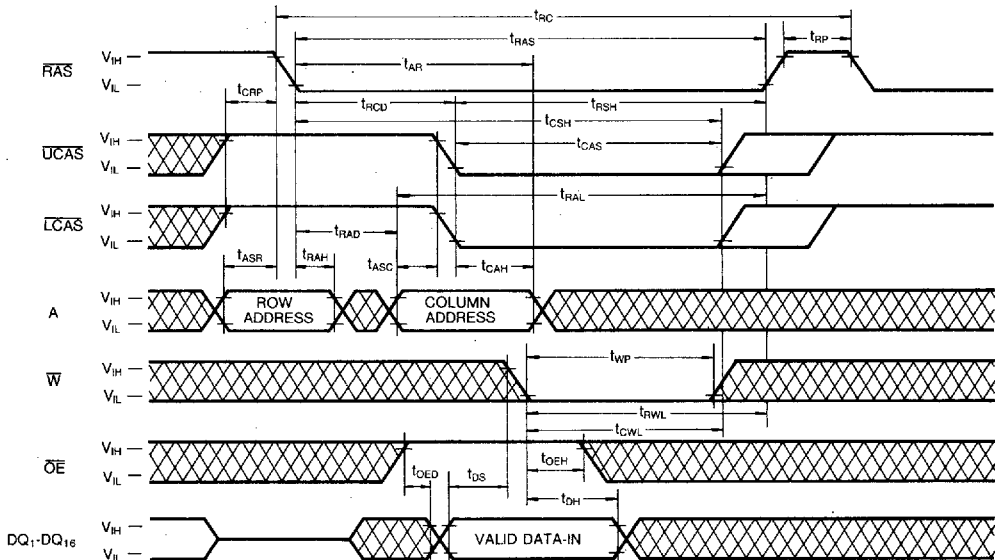
 DON'T CARE

TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)



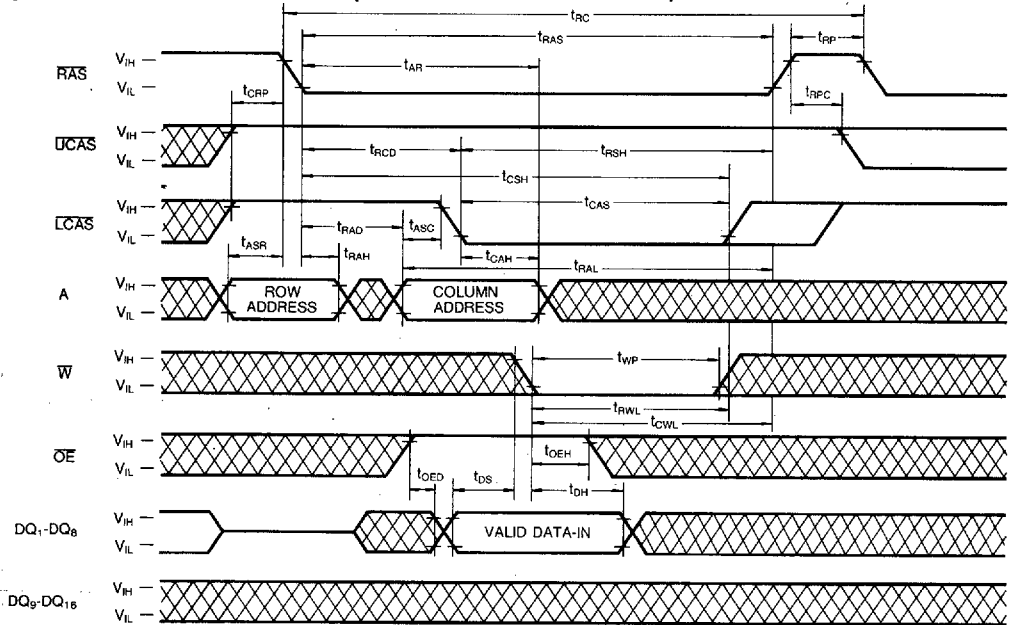
WORD WRITE CYCLE (OE CONTROLLED WRITE)



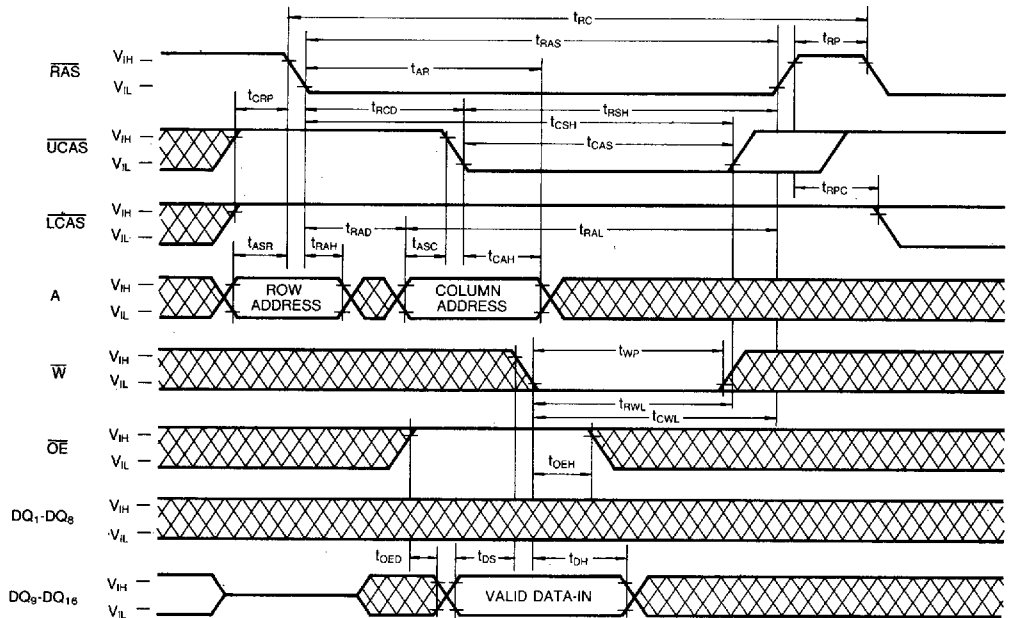
DONT CARE

TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)



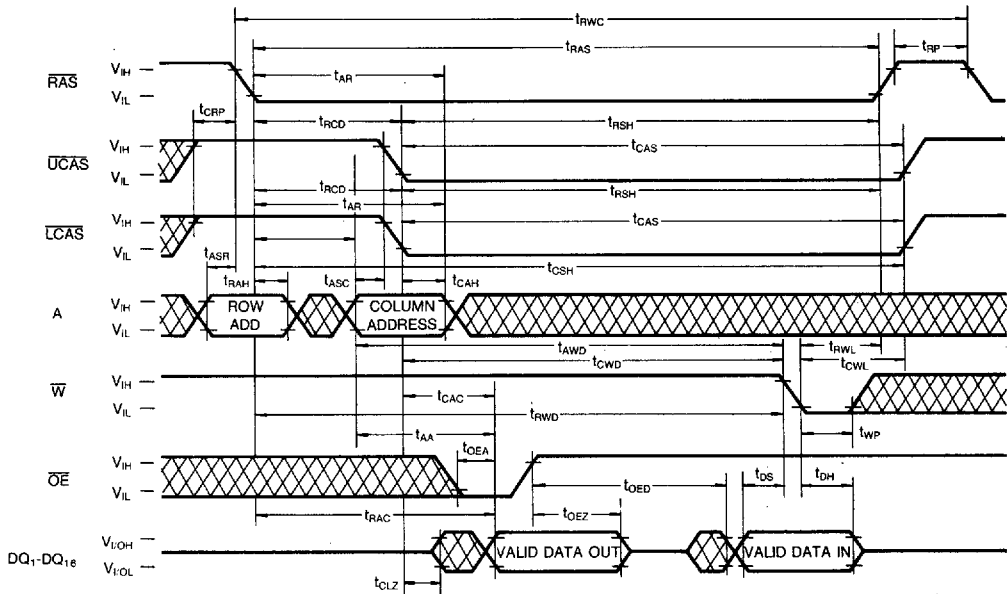
UPPER BYTE WRITE CYCLE (OE CONTROLLED WRITE)



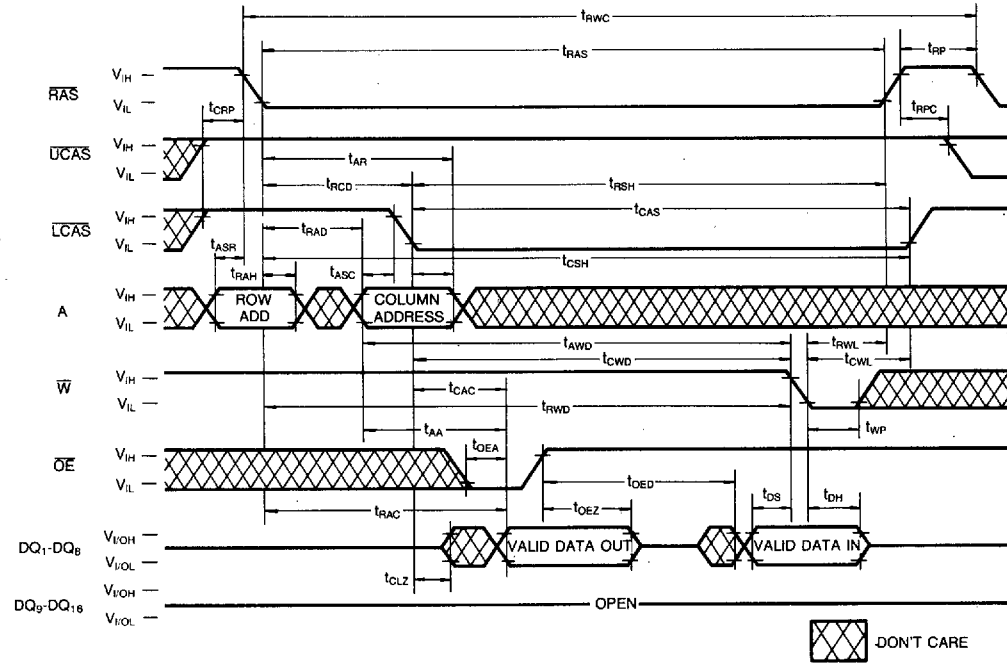
DON'T CARE

TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE



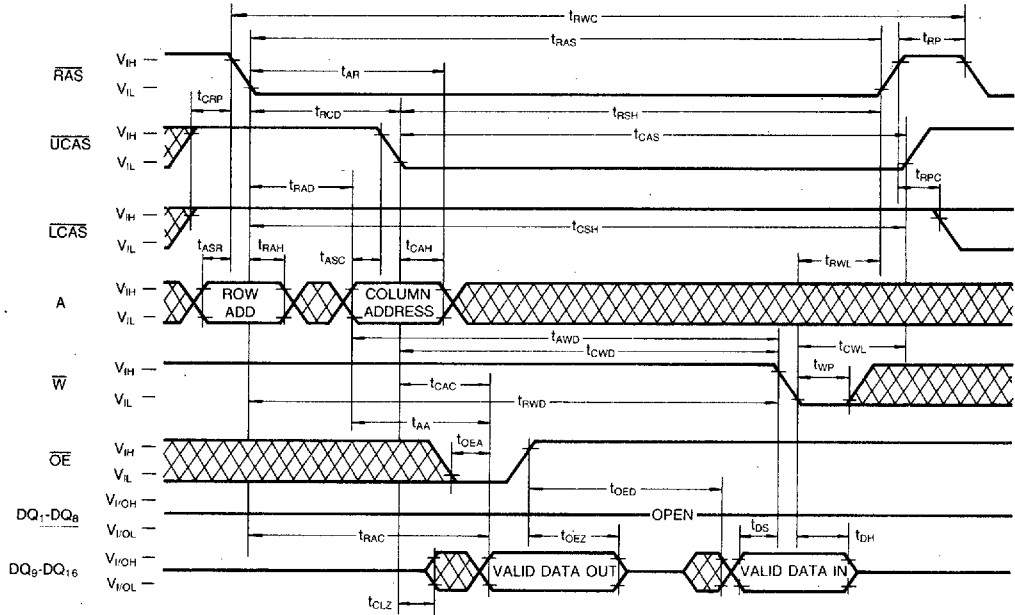
READ-MODIFY-LOWER-BYTE-WRITE CYCLE



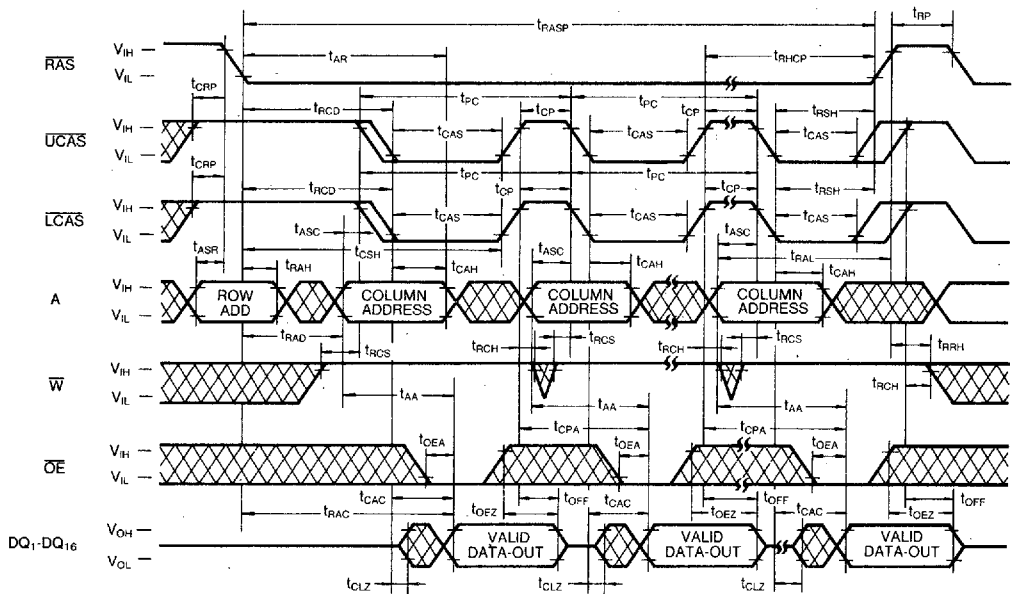
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TIMING DIAGRAMS (Continued)

READ-MODIFY-UPPER-BYTE-WRITE CYCLE



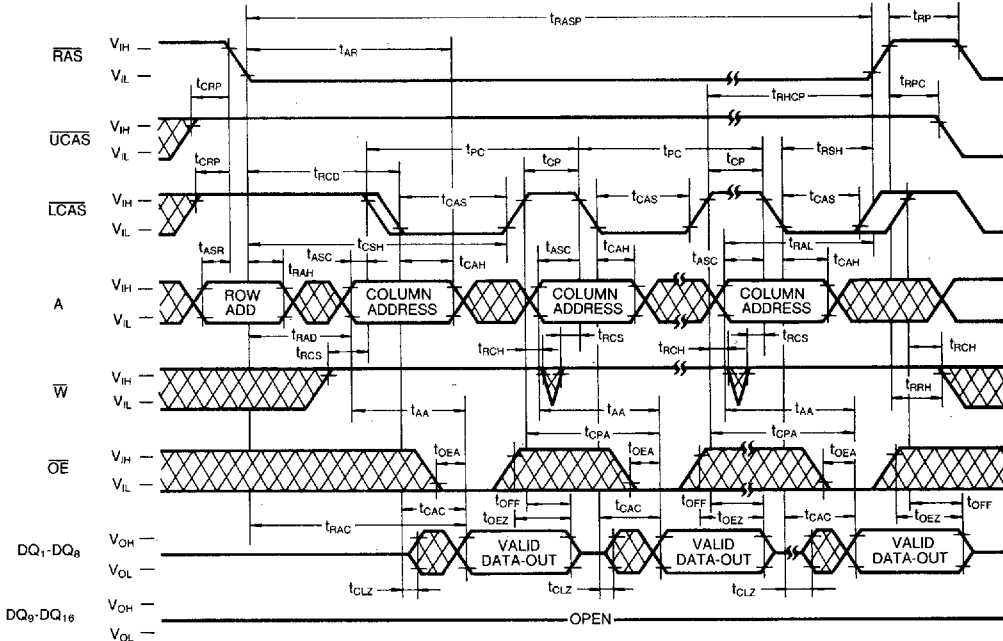
FAST PAGE MODE WORD READ CYCLE



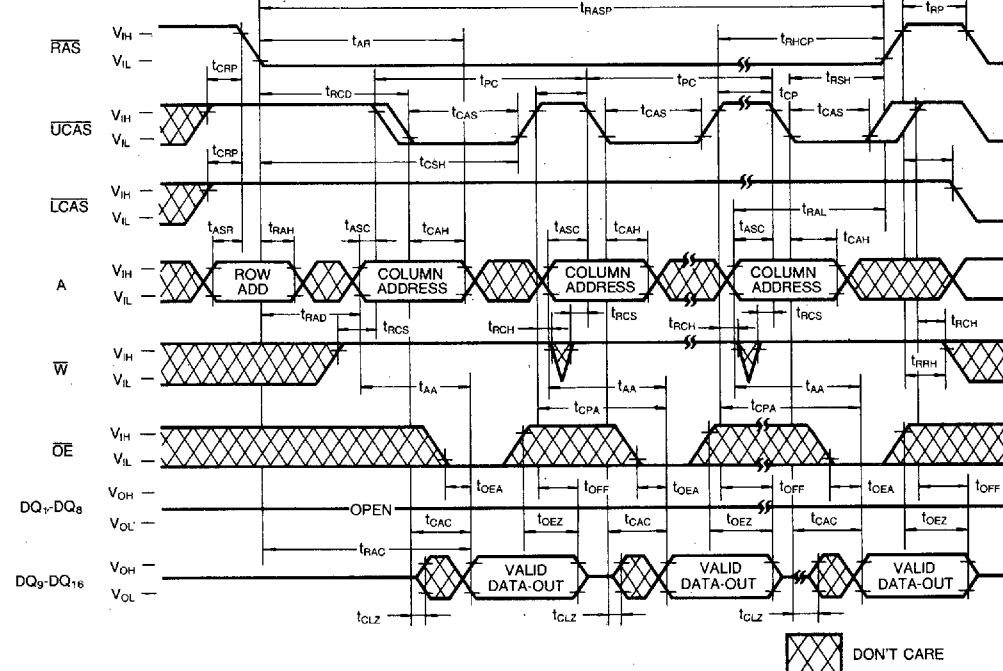
 DONT CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE



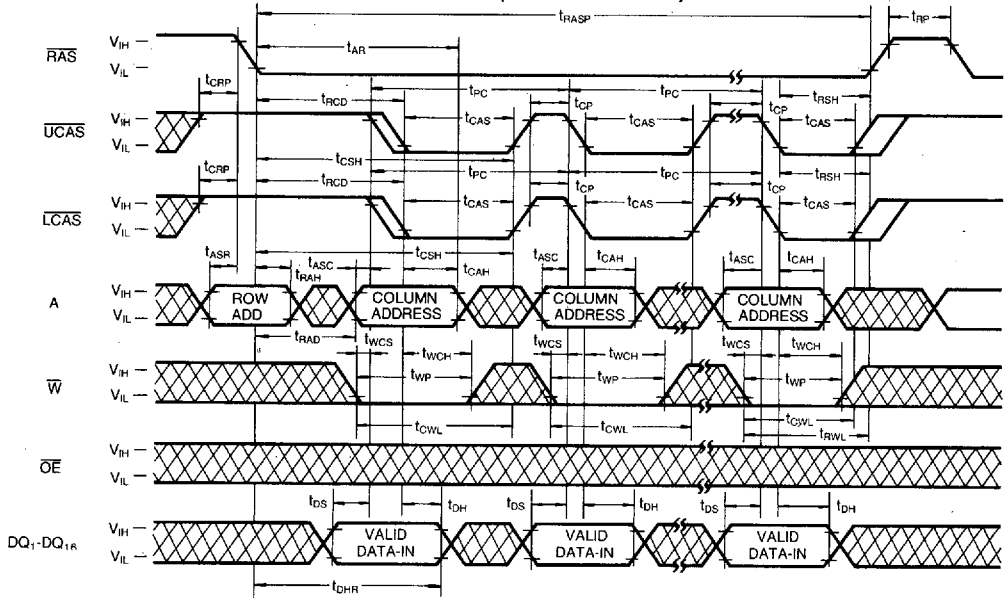
FAST PAGE MODE UPPER BYTE READ CYCLE



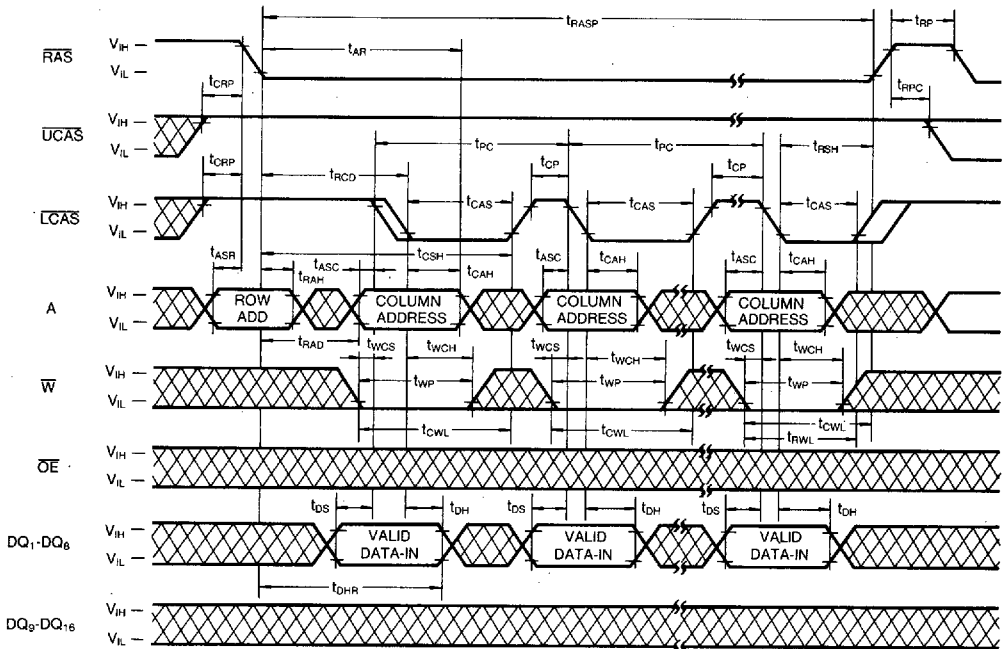
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TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)



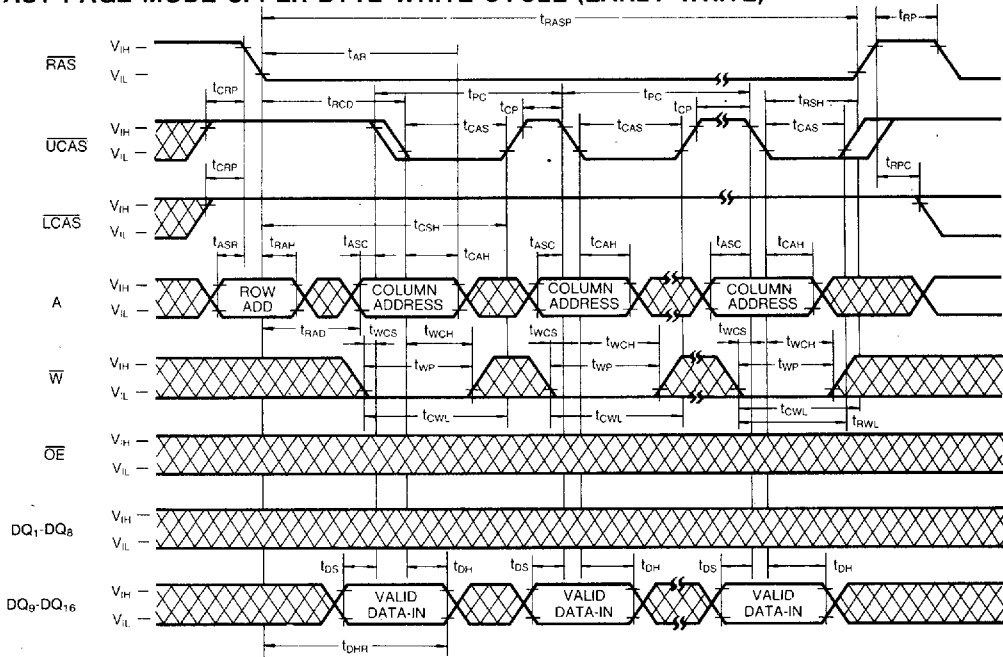
FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)



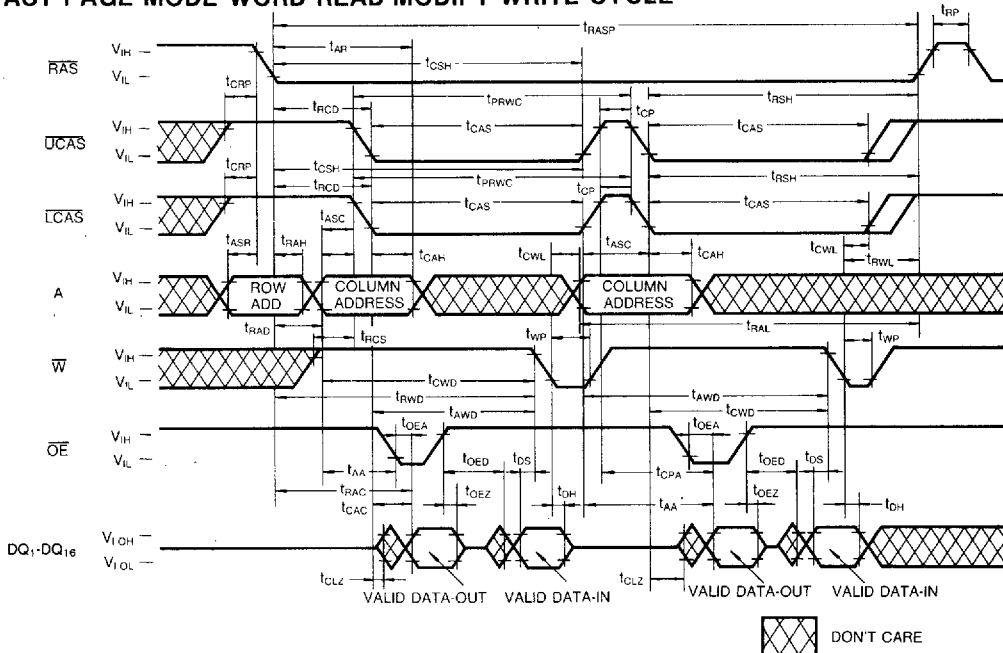
 DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)



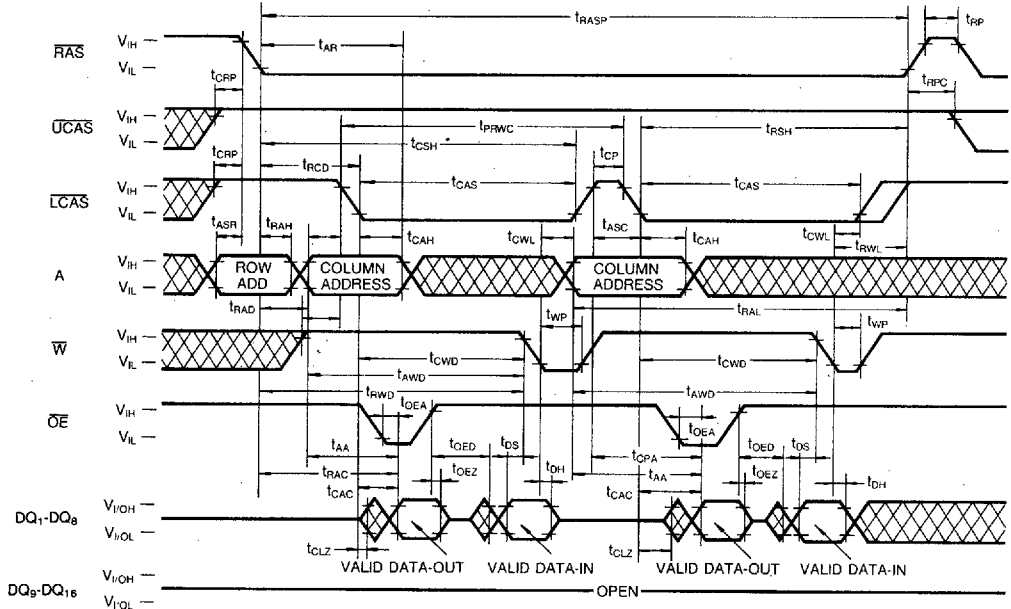
FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE



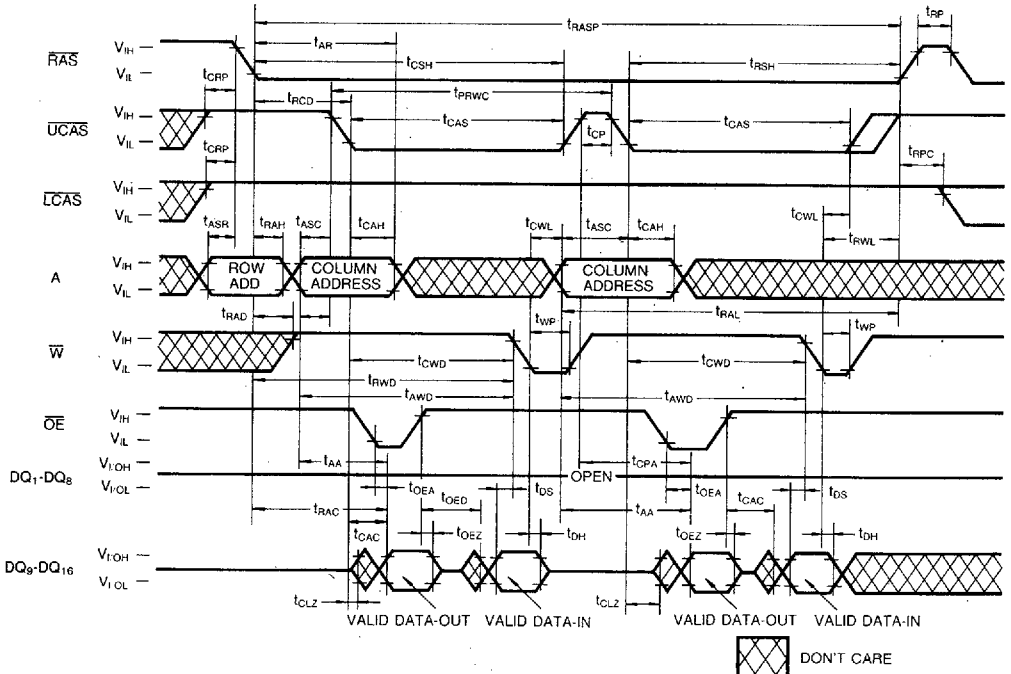
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TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



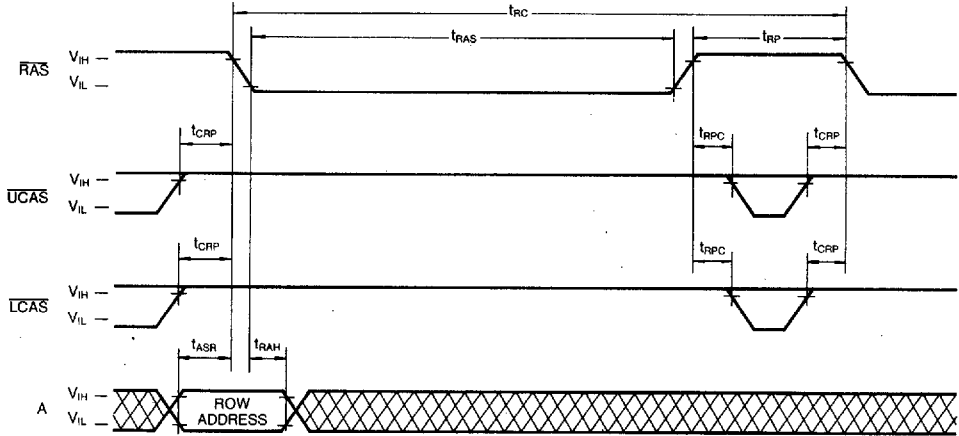
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



TIMING DIAGRAMS (Continued)

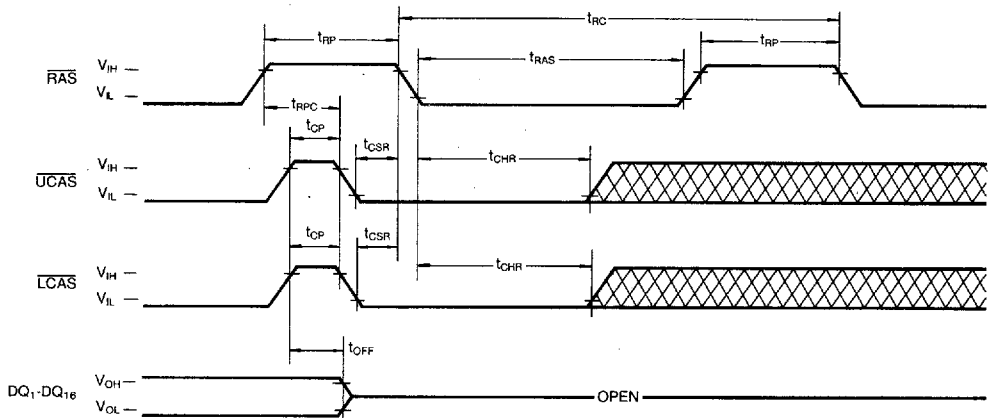
RAS ONLY REFRESH CYCLE

NOTE: \overline{W} , \overline{OE} =Don't Care



CAS-BEFORE-RAS REFRESH CYCLE

NOTE: $\overline{W}=V_{IH}$, \overline{OE} , A=Don't Care

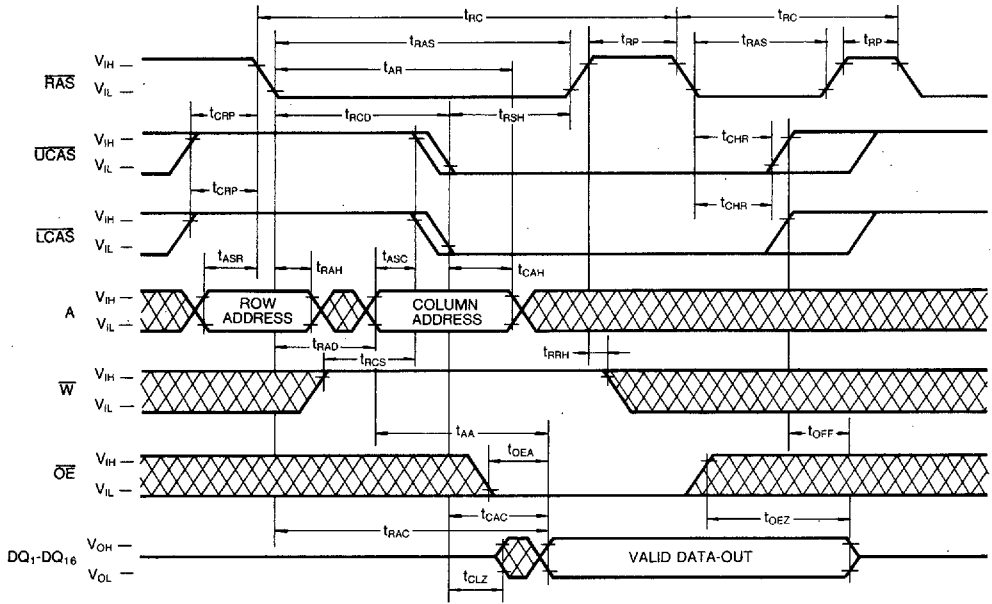


 DON'T CARE

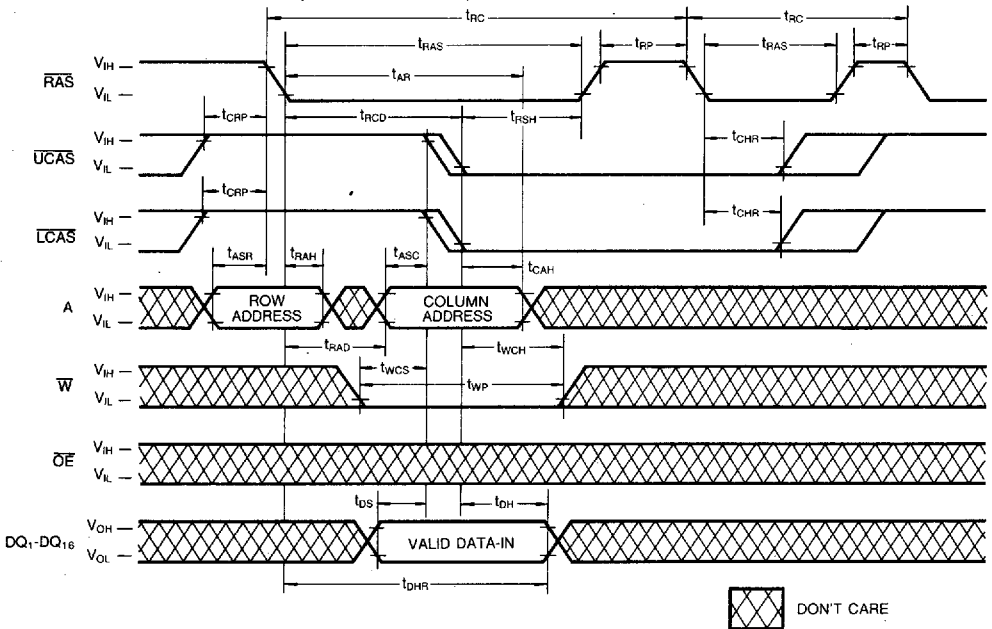
6

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

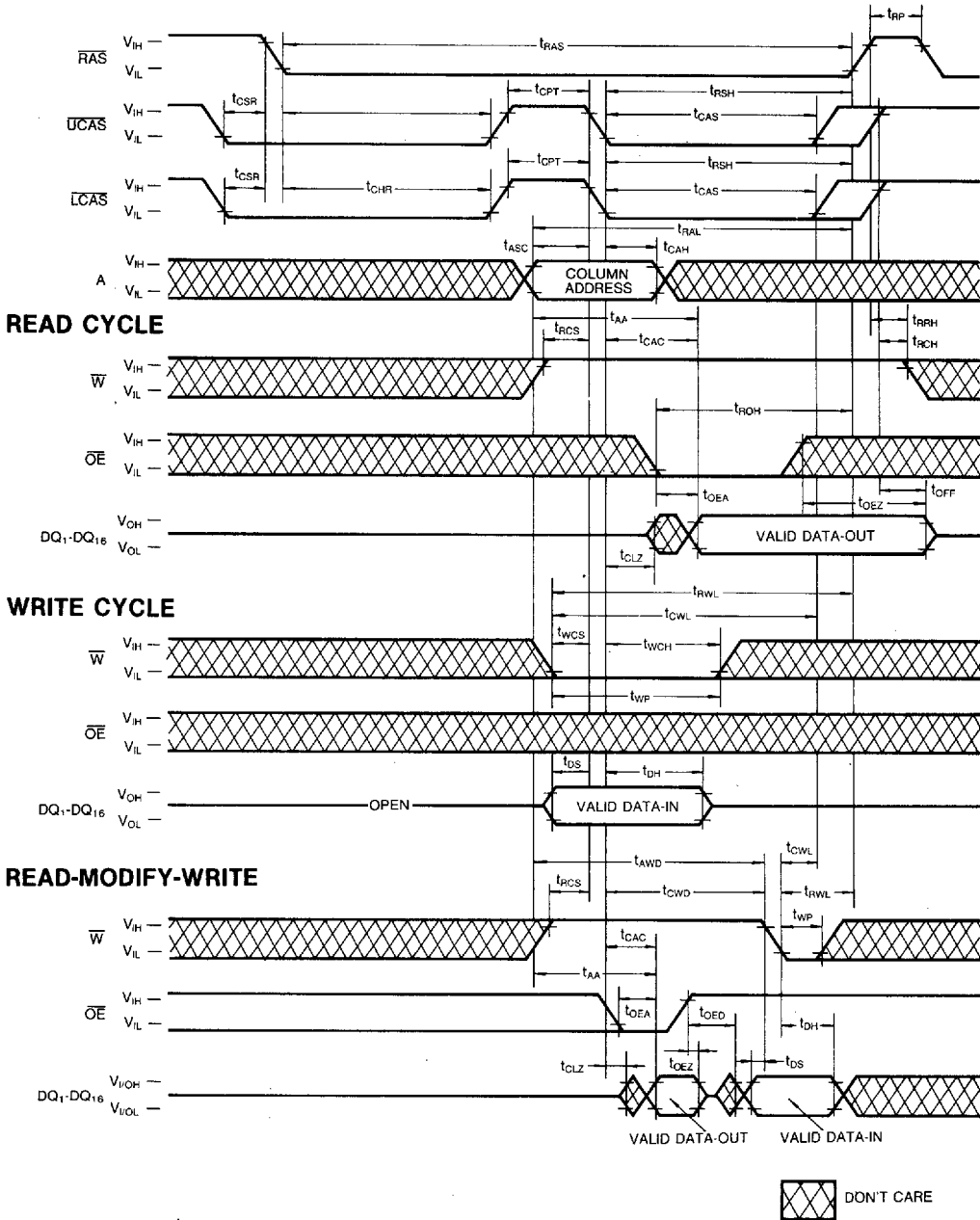


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

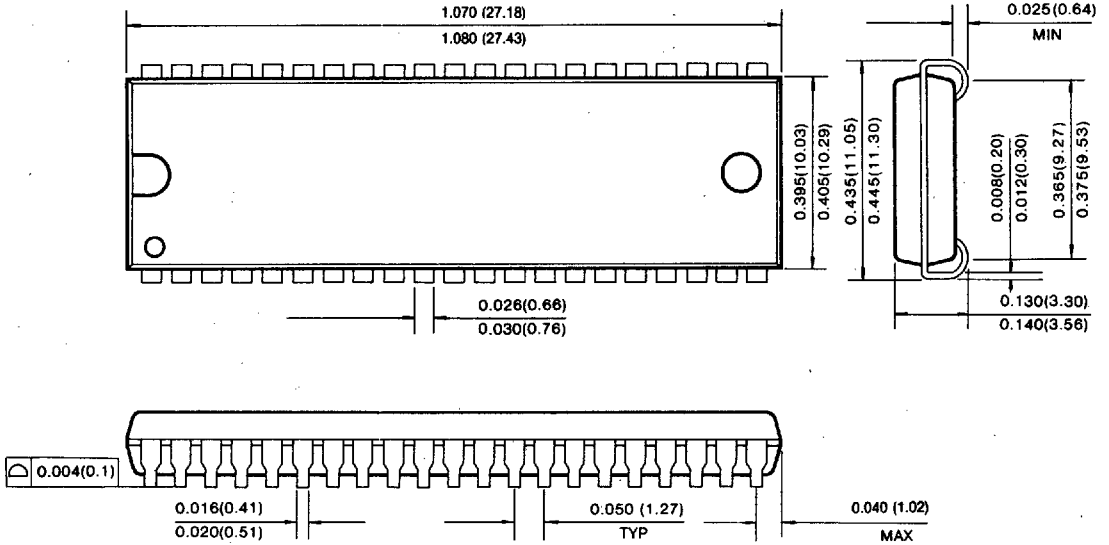
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



6

PACKAGE DIMENSION
42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

