UA78L Series Positive-Voltage Linear Regulators

1 Features

- Input voltage range (V_I): 4.75 V to 35 V
- Output voltage range (V_O):
  - 2.6 V to 15 V (for legacy chip)
  - 3.3 V to 15 V (for new chip)
- Output current: Up to 100 mA
- Quiescent current I_Q: 3.8 mA
- Built-in short-circuit current limiting and thermal protection
- Stable without any external component
- Supported temperature range:
  - Legacy chip C and AC versions: 0°C to +125°C
  - Legacy chip AI version: –40°C to +125°C
  - New chip: –40°C to +125°C
- Packages:
  - 8-pin, 4.9-mm × 3.91-mm SOIC
  - 3-pin, 4.3-mm × 4.3-mm TO-92
  - 3-pin, 4.5-mm × 2.5-mm SOT-89

2 Applications

- Motor drives
- Appliances
- Building automation
- Flow transmitters
- Factory automation and control

3 Description

The UA78L series of fixed-voltage linear regulators is designed for a wide range of applications. The UA78L series can be used for on-card regulation to eliminate the noise and distribution problems associated with single-point regulation. The UA78L can also be used with power-pass elements to make high-current voltage regulators. The UA78L series regulators can deliver up to 100 mA of output current. Additionally, the UA78L does not need an external capacitor for stable operation across the load current range. The internal current-limiting and thermal-shutdown features of these regulators help protect the device from overload.

For the legacy chip, the UA78L00C and UA78L00AC series are characterized for the junction temperature range of 0°C to +125°C and the UA78L05AI device is characterized for the operating junction temperature range of –40°C to +125°C.

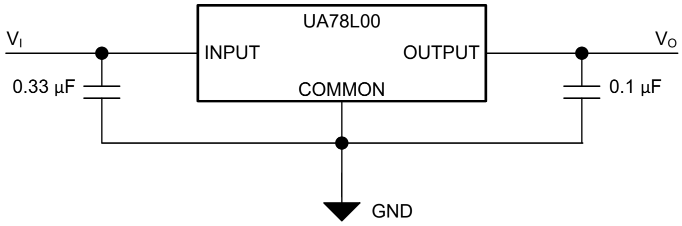
For the new chip, the UA78L series is characterized for the junction temperature range of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
UA78L	D (SOIC, 8)	4.9 mm × 6 mm
	LP (TO-92, 3)	5.2 mm × 3.68 mm
	PK (SOT-89, 3)	4.5 mm × 4.095 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision W (April 2023) to Revision X (June 2023)	Page
• Changed M3 device status from *Advance Information* to *Production Data*	1

Changes from Revision V (November 2016) to Revision W (April 2023)	Page
• Added M3 devices to document	1
• Changed *Features*, *Applications*, and *Description* sections	1
• Changed *Description* column of *Pin Functions* table	3
• Added plots for new chip, reordered plots for legacy chip, and changed condition statement in *Typical Characteristics* section	13
• Changed *Overview* section	17
• Changed *Feature Description* section and added subsections	17
• Changed *Device Functional Modes* section: added *Device Functional Mode Comparison* table, deleted *Fixed-Output Mode* subsection, and added *Normal Operation* and *Dropout Operation* subsections	19
• Changed *Detailed Design Procedure* section and added subsections	20
• Added plots for new chip and changed condition statement in *Application Curves* section	24
• Added *Device Nomenclature* and *Evaluation Module* sections	27

5 Pin Configuration and Functions

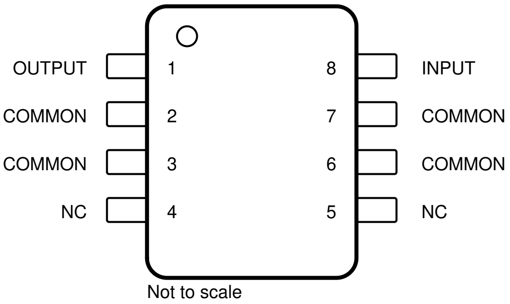


Figure 5-1. D Package, 8-Pin SOIC (Top View)

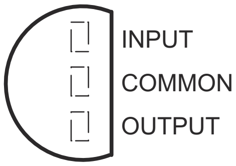


Figure 5-2. LP Package, 3-Pin TO-92 (Top View)

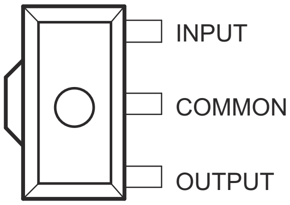


Figure 5-3. PK Package, 3-Pin SOT-89 (Top View)

PIN				TYPE	DESCRIPTION
NAME	**SOIC**	**TO-92**	**SOT-89**		
COMMON	2, 3, 6, 7	2	2	—	Ground
INPUT	8	3	3	I	Input pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.
OUTPUT	1	1	1	O	Output pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible.
NC	4, 5	—	—	—	No connect pin. This pin is not connected internally. Connect this pin to ground for best thermal performance or leave floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage, V_I (for legacy chip)	UA78L02AC, UA78L05C, UA78L09C, and UA78L10AC		30	V
	UA78L12C, UA78L12AC, UA78L15C, and UA78L15AC		35	
Input voltage, V_I (for new chip)	UA78L33AI, UA78L05AC, UA78L05AI, UA78L05C, UA78L12AC and UA78L15AC		45	
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE (Legacy Chip)	VALUE (New Chip)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	1000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	TYP	MAX	UNIT
V_I	Input voltage	UA78L02AC (for legacy chip only)	4.75		20	V
		UA78L033AC (for new chip only)	4.75		20	
		UA78L05C and UA78L05AC (for both legacy and new chip)	7		20	
		UA78L06C and UA78L06AC (for legacy chip only)	8.5		20	
		UA78L08C and UA78L08AC (for legacy chip only)	10.5		23	
		UA78L09C and UA78L09AC (for legacy chip only)	11.5		24	
		UA78L10AC (for legacy chip only)	12.5		25	
		UA78L12C and UA78L12AC (for both legacy and new chip)	14.5		27	
		UA78L15C and UA78L15AC (for both legacy and new chip)	17.5		30	
I_O	Output current				100	mA
C_{IN} (2)	Input capacitor (3)			0.33		µF
C_{OUT} (2)	Output capacitor (4)			0.1		
T_J	Operating junction temperature	UA78L00C and UA78L00AC series (for legacy chip)	0		125	°C
		UA78L05AI (for legacy chip)	–40		125	
		UA78L00C , UA78L00AC, and UA78L05AI series (for new chip)	–40		125	

(1) All voltages are with respect to GND.
(2) UA78L regulator doesn't need any external capacitors for the the LDO stability.
(3) An input capacitor with value of 0.33 µF is recommended to counteract the effect of source resistance and inductance, which can in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.
(4) An output capacitor with value of 0.1 µF is recommended to improve the load and line transient performance of the UA78L regulator.

6.4 Thermal Information

THERMAL METRIC(1)		UA78L00			UNIT
		D (SOIC)	LP (TO-92)	PK (SOT-89)	
		8 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115	143.6	54.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.3	74.4	88.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.6	—	9.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.2	24.2	6.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	55	120.9	9.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	7.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: UA78L02 (Legacy Chip Only)

at specified junction temperature, V_I = 9 V, C_{IN} = 0.33 μF, C_{OUT} = 0.1μF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)		MIN	TYP	MAX	UNIT
Output voltage	V_I = 4.75 V to 20 V, and I_O = 1 mA to 40 mA	T_J = 25°C	2.5	2.6	2.7	V
		T_J = 0°C to 125°C	2.45		2.75	
	I_O = 1 mA to 70 mA, and T_J = 0°C to 125°C		2.45		2.75	
Input voltage regulation	V_I = 4.75 V to 20 V, and T_J = 25°C			20	100	mV
	V_I = 5 V to 20 V, and T_J = 25°C			16	75	
Ripple rejection	V_I = 6 V to 20 V, f = 120 Hz, and T_J = 25°C		43	51		dB
Output voltage regulation	I_O = 1 mA to 100 mA, and T_J = 25°C			12	50	mV
	I_O = 1 mA to 40 mA, and T_J = 25°C			6	25	
Output noise voltage	f = 10 Hz to 100 kHz, and T_J = 25°C			30		μV
Dropout voltage	T_J = 25°C			1.7		V
Bias current	T_J = 25°C			3.6	6	mA
	T_J = 125°C				5.5	
Bias current change	V_I = 5 V to 20 V, and T_J = 0°C to 125°C				2.5	mA
	I_O = 1 mA to 40 mA, and T_J = 0°C to 125°C				0.1	

(1) Applies to UA78L02AC.
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L02AC is T_J = 0°C to 125°C.

6.6 Electrical Characteristics: UA78L033 (New Chip Only)

at specified junction temperature, V_I = 9 V, C_{IN} = 0.33 μF, C_{OUT} = 0.1μF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
Output voltage	V_I = 5.5 V to 20 V, and I_O = 1 mA to 40 mA, T_J = 25°C	3.26	3.3	3.44	V
	V_I = 5.5 V to 20 V, and I_O = 1 mA to 40 mA, T_J = -40°C to 125°C	3.21		3.47	
	I_O = 1 mA to 70 mA, T_J = -40°C to 125°C	3.23		3.45	
Input voltage regulation	V_I = 5.5 V to 20 V, and T_J = 25°C		15	25	mV
	V_I = 6 V to 20 V, and T_J = 25°C		14	27	
Ripple rejection	V_I = 6 V to 20 V, f = 120 Hz, and T_J = 25°C	49	57.5		dB
Output voltage regulation	I_O = 1 mA to 100 mA, and T_J = 25°C		13.5	28	mV
	I_O = 1 mA to 40 mA, and T_J = 25°C		4.25	13	
Output noise voltage	f = 10 Hz to 100 kHz, and T_J = 25°C		85		μV
Dropout voltage	T_J = 25°C		1.7		V

6.6 Electrical Characteristics: UA78L033 (New Chip Only) (continued)

at specified junction temperature, V_I = 9 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
Bias current	T_J = 25°C		3.53	4.1	mA
	T_J = 125°C			4.1	
Bias current change	V_I = 6 V to 20 V, and T_J = -40°C to 125°C			0.675	mA
	I_O = 1 mA to 40 mA, and T_J = -40°C to 125°C			0.01	

(1) Applies to UA78L033
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

6.7 Electrical Characteristics: UA78L05 (Both Legacy and New Chip)

at specified junction temperature, V_I = 10 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)			MIN	TYP	MAX	UNIT
Output voltage	V_I = 7 V to 20 V, and I_O = 1 mA to 40 mA (for legacy chip)	T_J = 25°C	UA78L05C	4.6	5	5.4	V
			UA78L05AC and UA78L05AI	4.8	5	5.2	
		T_J = full range	UA78L05C	4.5		5.5	
			UA78L05AC and UA78L05AI	4.75		5.25	
	I_O = 1 mA to 70 mA, and T_J = full range (for legacy chip)	UA78L05C		4.5		5.5	
		UA78L05AC and UA78L05AI		4.75		5.25	
	V_I = 7 V to 20 V, and I_O = 1 mA to 40 mA (for new chip)	T_J = 25°C	UA78L05C	4.95	5	5.15	
			UA78L05AC and UA78L05AI	4.95	5	5.15	
		T_J = full range	UA78L05C	4.85		5.15	
			UA78L05AC and UA78L05AI	4.85		5.15	
	I_O = 1 mA to 70 mA, and T_J = full range (for new chip)	UA78L05C		4.80		5.14	
		UA78L05AC and UA78L05AI		4.80		5.14	
Input voltage regulation	V_I = 7 V to 20 V, and T_J = 25°C (for legacy chip)	UA78L05C			32	200	mV
		UA78L05AC and UA78L05AI			32	150	
	V_I = 8 V to 20 V, and T_J = 25°C (for legacy chip)	UA78L05C			26	150	
		UA78L05AC and UA78L05AI			26	100	
	V_I = 7 V to 20 V, and T_J = 25°C (for new chip)	UA78L05C			32	33	
		UA78L05AC and UA78L05AI			32	33	
	V_I = 8 V to 20 V, and T_J = 25°C (for new chip)	UA78L05C			26	28	
		UA78L05AC and UA78L05AI			26	28	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz, and T_J = 25°C (for legacy chip)	UA78L05C		40	49		dB
		UA78L05AC and UA78L05AI		41	49		
	V_I = 8 V to 18 V, f = 120 Hz, and T_J = 25°C (for new chip)	UA78L05C		48	55		
		UA78L05AC and UA78L05AI		48	55		
Output voltage regulation	for legacy chip	I_O = 1 mA to 100 mA, and T_J = 25°C			15	60	mV
		I_O = 1 mA to 40 mA, and T_J = 25°C			8	30	
	for new chip	I_O = 1 mA to 100 mA, and T_J = 25°C			15	35	
		I_O = 1 mA to 40 mA, and T_J = 25°C			8	15	
Output noise voltage	for legacy chip	f = 10 Hz to 100 kHz, and T_J = 25°C			42		µV
	for new chip	f = 10 Hz to 100 kHz, and T_J = 25°C			125		
Dropout voltage	for legacy chip	T_J = 25°C			1.7		V
	for new chip				1.7		V

6.7 Electrical Characteristics: UA78L05 (Both Legacy and New Chip) (continued)

at specified junction temperature, V_I = 10 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)		MIN	TYP	MAX	UNIT
Bias current	for legacy chip	T_J = 25°C		3.8	6	mA
		T_J = 125°C			5.5	mA
	for new chip	T_J = 25°C		3.53	3.95	mA
		T_J = 125°C			4.0	
Bias current change	V_I = 8 V to 20 V, and T_J = full range (for new legacy chip)				1.5	mA
	I_O = 1 mA to 40 mA, and T_J = full range (for legacy chip)	UA78L05C			1.5	mA
		UA78L05AC and UA78L05AI			1.5	mA
	V_I = 8 V to 20 V, and T_J = full range (for new chip)				0.485	mA
	I_O = 1 mA to 40 mA, and T_J = full range (for new chip)	UA78L05C			0.01	
		UA78L05AC and UA78L05AI			0.01	

(1) Applies to UA78L05C, UA78L05AC and UA78L05AI.
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L05C, UA78L05AC is T_J = 0°C to 125°C, and for the UA78L05AI is T_J = –40°C to 125°C. For new chip, temperature range for the UA78L05C, UA78L05AC and UA78L05AI is T_J = –40°C to 125°C.

6.8 Electrical Characteristics: UA78L12 (Both Legacy and New Chip)

at specified junction temperature, V_I = 19 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)			MIN	TYP	MAX	UNIT
Output voltage	V_I = 14 V to 27 V, and I_O = 1 mA to 40 mA	T_J = 25°C	UA78L12C (legacy chip)	11.1	12	12.9	V
			UA78L12AC (legacy chip)	11.5	12	12.5	
		T_J = 0°C to 125°C	UA78L12C (legacy chip)	10.8		13.2	
			UA78L12AC (legacy chip)	11.4		12.6	
	T_J = 0°C to 125°C, and I_O = 1 mA to 70 mA		UA78L12C (legacy chip)	10.8		13.2	
			UA78L12AC (legacy chip)	11.4		12.6	
	V_I = 14 V to 27 V, and I_O = 1 mA to 40 mA	T_J = 25°C	UA78L12C (new chip)	11.83	12	12.31	
			UA78L12AC (new chip)				
		T_J = -40°C to 125°C	UA78L12C (new chip)	11.65		12.35	
			UA78L12AC (new chip)				
	T_J = -40°C to 125°C, and I_O = 1 mA to 70 mA		UA78L12C (new chip)	11.47		12.35	
			UA78L12AC (new chip)				
Input voltage regulation	T_J = 25°C	V_I = 14.5 V to 27 V	for legacy chip		55	250	mV
		V_I = 16 V to 27 V			49	200	
		V_I = 14.0 V to 27 V	for new chip		55	80	
		V_I = 16 V to 27 V			49	65	
Ripple rejection	T_J = 25°C	V_I = 15 V to 25 V, and f = 120 Hz	UA78L12C (legacy chip)	36	42		dB
			UA78L12AC (legacy chip)	37	42		
			UA78L12C (new chip)	40	50		
			UA78L12AC (new chip)				

6.8 Electrical Characteristics: UA78L12 (Both Legacy and New Chip) (continued)

at specified junction temperature, V_I = 19 V, C_{IN} = 0.33 μF, C_{OUT} = 0.1μF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)			MIN	TYP	MAX	UNIT
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA	for legacy chip		22	100	mV
		I_O = 1 mA to 40 mA			13	50	
		I_O = 1 mA to 100 mA	for new chip		22	70	
		I_O = 1 mA to 40 mA			13	30	
Output noise voltage	T_J = 25°C, and f = 10 Hz to 100 kHz	for legacy chip			70		μV
		for new chip			290		μV
Dropout voltage	T_J = 25°C	for legacy chip			1.7		V
		for new chip			1.7		
Bias current	T_J = 25°C	for legacy chip			4.3	6.5	mA
	T_J = 125°C					6	
	T_J = 25°C	for new chip			3.84	4.350	mA
	T_J = 125°C					4.355	
Bias current change	T_J = 0°C to 125°C	V_I = 16 V to 27 V (legacy chip)				1.5	mA
		I_O = 1 mA to 40 mA	UA78L12C (legacy chip)			0.2	
			UA78L12AC (legacy chip)			0.1	
	T_J = –40°C to 125°C	V_I = 16 V to 27 V (new chip)				0.450	
		I_O = 1 mA to 40 mA	UA78L12C (new chip)			0.01	
			UA78L12AC (new chip)				

(1) Applies to UA78L12C and UA78L12AC.

(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L12C, UA78L12AC is T_J = 0°C to 125°C. For new chip, temperature range for the UA78L12C and UA78L12AC is T_J = –40°C to 125°C.

6.9 Electrical Characteristics: UA78L06 (Legacy Chip Only)

at specified junction temperature, V_I = 12 V, C_{IN} = 0.33 μF, C_{OUT} = 0.1μF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)			MIN	TYP	MAX	UNIT
Output voltage	V_I = 8.5 V to 20 V, I_O = 1 mA to 40 mA	T_J = 25°C	UA78L06C	5.7	6.2	6.7	V
			UA78L06AC	5.95	6.2	6.45	
		T_J = 0°C to 125°C	UA78L06C	5.6		6.8	
			UA78L06AC	5.9		6.5	
	T_J = 0°C to 125°C, and I_O = 1 mA to 70 mA		UA78L06C	5.6		6.8	
			UA78L06AC	5.9		6.5	
Input voltage regulation	T_J = 25°C	V_I = 8.5 V to 20 V	UA78L06C		35	200	mV
			UA78L06AC		35	175	
		V_I = 9 V to 20 V	UA78L06C		29	150	
			UA78L06AC		29	125	
Ripple rejection	T_J = 25°C, V_I = 10 V to 20 V, and f = 120 Hz		UA78L06C	39	48		dB
			UA78L06AC	40	48		
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA			16	80	mV
		I_O = 1 mA to 40 mA			9	40	
Output noise voltage	T_J = 25°C, and f = 10 Hz to 100 kHz				46		μV
Dropout voltage	T_J = 25°C				1.7		V
Bias current	T_J = 25°C				3.9	6	mA
	T_J = 125°C					5.5	

6.9 Electrical Characteristics: UA78L06 (Legacy Chip Only) (continued)

at specified junction temperature, V_I = 12 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)			MIN	TYP	MAX	UNIT
Bias current change	T_J = 0°C to 125°C	V_I = 9 V to 20 V				1.5	mA
		I_O = 1 mA to 40 mA	UA78L06C			0.2	
			UA78L06AC			0.1	

(1) Applies to UA78L06C and UA78L06AC.
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L06C and UA78L06AC is T_J = 0°C to 125°C.

6.10 Electrical Characteristics: UA78L08 (Legacy Chip Only)

at specified junction temperature, V_I = 14 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)			MIN	TYP	MAX	UNIT
Output voltage	V_I = 10.5 V to 23 V, I_O = 1 mA to 40 mA	T_J = 25°C	UA78L08C	7.36	8	8.64	V
			UA78L08AC	7.7	8	8.3	
		T_J = 0°C to 125°C	UA78L08C	7.2		8.8	
			UA78L08AC	7.6		8.4	
	I_O = 1 mA to 70 mA	T_J = 0°C to 125°C	UA78L08C	7.2		8.8	
			UA78L08AC	7.6		8.4	
Input voltage regulation	T_J = 25°C	V_I = 10.5 V to 23 V	UA78L08C		42	200	mV
			UA78L08AC		42	175	
		V_I = 11 V to 23 V	UA78L08C		36	150	
			UA78L08AC		36	125	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz, and T_J = 25°C		UA78L08C	36	46		dB
			UA78L08AC	37	46		
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA			18	80	mV
		I_O = 1 mA to 40 mA			10	40	
Output noise voltage	f = 10 Hz to 100 kHz, and T_J = 25°C				54		µV
Dropout voltage	T_J = 25°C				1.7		V
Bias current	T_J = 25°C				4	6	mA
	T_J = 125°C					5.5	
Bias current change	T_J = 0°C to 125°C	V_I = 11 V to 23 V				1.5	mA
		I_O = 1 mA to 40 mA	UA78L08C			0.2	
			UA78L08AC			0.1	

(1) Applies to UA78L08C and UA78L08AC.
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L08C and UA78L08AC is T_J = 0°C to 125°C.

6.11 Electrical Characteristics: UA78L09 (Legacy Chip Only)

at specified junction temperature, V_I = 16 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)			MIN	TYP	MAX	UNIT
Output voltage	V_I = 12 V to 24 V, I_O = 1 mA to 40 mA	T_J = 25°C	UA78L09C	8.3	9	9.7	V
			UA78L09AC	8.6	9	9.4	
		T_J = 0°C to 125°C	UA78L09C	8.1		9.9	
			UA78L09AC	8.55		9.45	
	I_O = 1 mA to 70 mA, and T_J = 0°C to 125°C		UA78L09C	8.1		9.9	
			UA78L09AC	8.55		9.45	
Input voltage regulation	T_J = 25°C	V_I = 12 V to 24 V	UA78L09C		45	225	mV
			UA78L09AC		45	175	
		V_I = 13 V to 24 V	UA78L09C		40	175	
			UA78L09AC		40	125	

6.11 Electrical Characteristics: UA78L09 (Legacy Chip Only) (continued)

at specified junction temperature, V_I = 16 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)			MIN	TYP	MAX	UNIT
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz, and T_J = 25°C		UA78L09C	36	45		dB
			UA78L09AC	38	45		
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA			19	90	mV
		I_O = 1 mA to 40 mA			11	40	
Output noise voltage	f = 10 Hz to 100 kHz, and T_J = 25°C				58		µV
Dropout voltage	T_J = 25°C				1.7		V
Bias current	T_J = 25°C				4.1	6	mA
	T_J = 125°C					5.5	
Bias current change	T_J = 0°C to 125°C	V_I = 13 V to 24 V				1.5	mA
		I_O = 1 mA to 40 mA	UA78L09C			0.2	
			UA78L09AC			0.1	

(1) Applies to UA78L09C ad UA78L09AC.
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L09C and UA78L09AC is T_J = 0°C to 125°C.

6.12 Electrical Characteristics: UA78L10 (Legacy Chip Only)

at specified junction temperature, V_I = 14 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)		MIN	TYP	MAX	UNIT
Output voltage	V_I = 13 V to 25 V, and I_O = 1 mA to 40 mA	T_J = 25°C	9.6	10	10.4	V
		T_J = 0°C to 125°C	9.5		10.5	
	T_J = 0°C to 125°C, and I_O = 1 mA to 70 mA		9.5		10.5	
Input voltage regulation	T_J = 25°C	V_I = 13 V to 25 V		51	175	mV
		V_I = 14 V to 25 V		42	125	
Ripple rejection	T_J = 25°C, V_I = 15 V to 25 V, and f = 120 Hz		37	44		dB
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA		20	90	mV
		I_O = 1 mA to 40 mA		11	40	
Output noise voltage	T_J = 25°C, and f = 10 Hz to 100 kHz			62		µV
Dropout voltage	T_J = 25°C			1.7		V
Bias current	T_J = 25°C			4.2	6	mA
	T_J = 125°C				5.5	
Bias current change	T_J = 0°C to 125°C	V_I = 14 V to 25 V			1.5	mA
		I_O = 1 mA to 40 mA			0.1	

(1) Applies to UA78L10AC.
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L10AC is T_J = 0°C to 125°C.

6.13 Electrical Characteristics: UA78L15 (Both Legacy and New Chip)

at specified junction temperature, V_I = 23 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted) (1)

PARAMETER	TEST CONDITIONS (2)			MIN	TYP	MAX	UNIT
Output voltage	V_I = 17.5 V to 30 V, and I_O = 1 mA to 40 mA	T_J = 25°C	UA78L15C (legacy chip)	13.8	15	16.2	V
			UA78L15AC (legacy chip)	14.4	15	15.6	V
		T_J = 0°C to 125°C	UA78L15C (legacy chip)	13.5		16.5	V
			UA78L15AC (legacy chip)	14.25		15.75	V
	T_J = 0°C to 125°C, and I_O = 1 mA to 70 mA		UA78L15C (legacy chip)	13.5		16.5	V
			UA78L15AC (legacy chip)	14.25		15.75	V
	V_I = 17.5 V to 30 V, and I_O = 1 mA to 40 mA	T_J = 25°C	UA78L15C (new chip)	14.750	15	15.425	V
			UA78L15AC (new chip)	14.750	15	15.425	
		T_J = -40°C to 125°C	UA78L15C (new chip)	14.575		15.450	
			UA78L15AC (new chip)	14.575		15.450	
	T_J = -40°C to 125°C, and I_O = 1 mA to 70 mA		UA78L15C (new chip)	14.35		15.45	
			UA78L15AC (new chip)	14.35		15.45	
Input voltage regulation	T_J = 25°C	V_I = 17.5 V to 30 V	for legacy chip		65	300	mV
		V_I = 20 V to 30 V			58	250	
		V_I = 17.5 V to 30 V	for new chip		65	82	
		V_I = 20 V to 30 V			58	60	
Ripple rejection	T_J = 25°C	V_I = 18.5 V to 28.5 V, and f = 120 Hz	UA78L15C (legacy chip)	33	39		dB
			UA78L15AC (legacy chip)	34	39		
		V_I = 18.5 V to 28.5 V, and f = 120 Hz	UA78L15C (new chip)	40	45		
			UA78L15AC (new chip)	40	45		
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA	for legacy chip		25	150	mV
		I_O = 1 mA to 40 mA			15	75	
		I_O = 1 mA to 100 mA	for new chip		25	27	
		I_O = 1 mA to 40 mA			15	60	
Output noise voltage	T_J = 25°C, and f = 10 Hz to 100 kHz	for legacy chip			82		μV
		for new chip			388		
Dropout voltage	T_J = 25°C	for legacy chip			1.7		V
		for new chip			1.7		
Bias current	T_J = 25°C	for legacy chip			4.6	6.5	mA
	T_J = 125°C					6	
	T_J = 25°C	for new chip			4.1	4.670	
	T_J = 125°C					4.675	

6.13 Electrical Characteristics: UA78L15 (Both Legacy and New Chip) (continued)

at specified junction temperature, V_I = 23 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted) (1)

PARAMETER	TEST CONDITIONS (2)			MIN	TYP	MAX	UNIT
Bias current change	T_J = 0°C to 125°C	V_I = 10 V to 30 V	legacy chip			1.5	mA
		I_O = 1 mA to 40 mA	UA78L15C (legacy chip)			0.2	
			UA78L15AC (legacy chip)			0.1	
	T_J = -40°C to 125°C	V_I = 20 V to 30 V	new chip			0.425	
		I_O = 1 mA to 40 mA	UA78L15C (new chip)			0.01	
			UA78L15AC (new chip)			0.02	

(1) Applies to UA78L15C and UA78L15AC.

(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L15C, UA78L15AC is T_J = 0°C to 125°C. For new chip, temperature range for the UA78L15C and UA78L15AC is T_J = –40°C to 125°C.

6.14 Typical Characteristics

at specified junction temperature T_J = 25 °C, V_I = 10 V, V_O = 5 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF, and I_O = 1 mA (unless otherwise noted)

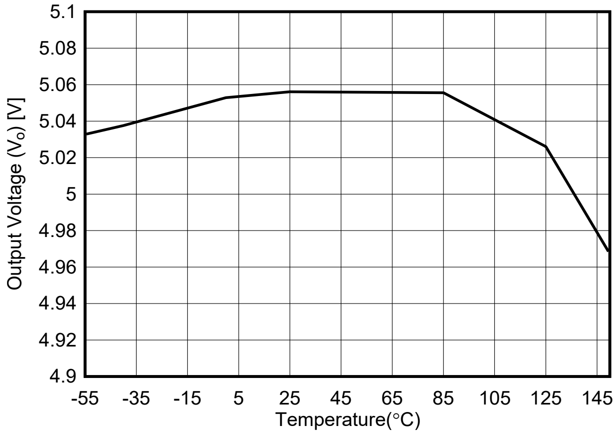
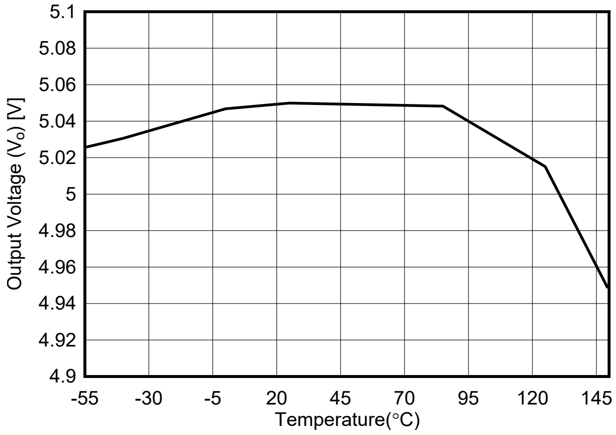


Figure 6-1. V_O vs Temperature for New Chip



I_O = 40 mA

Figure 6-2. V_O vs Temperature for New Chip

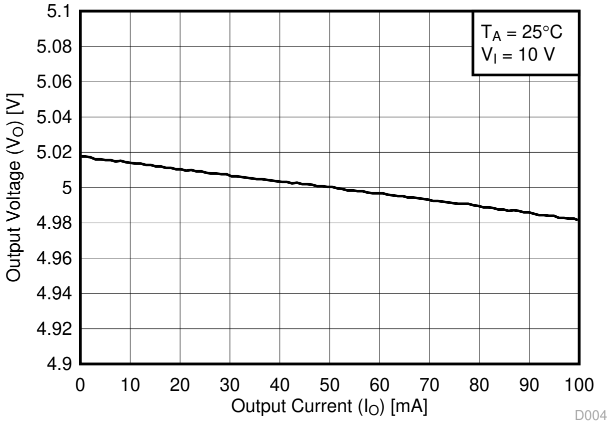


Figure 6-3. Load Regulation for Legacy Chip

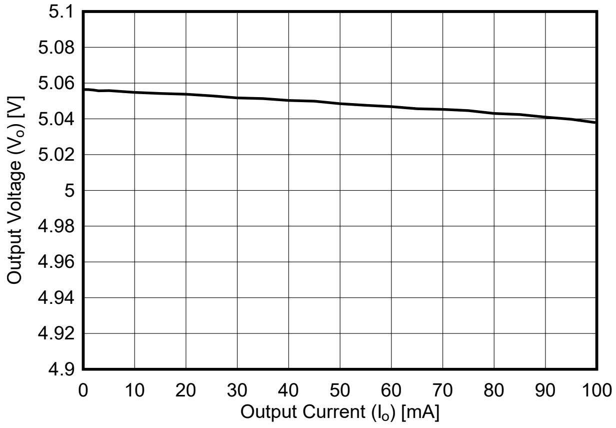


Figure 6-4. Load Regulation for New Chip at T_J = 25°C

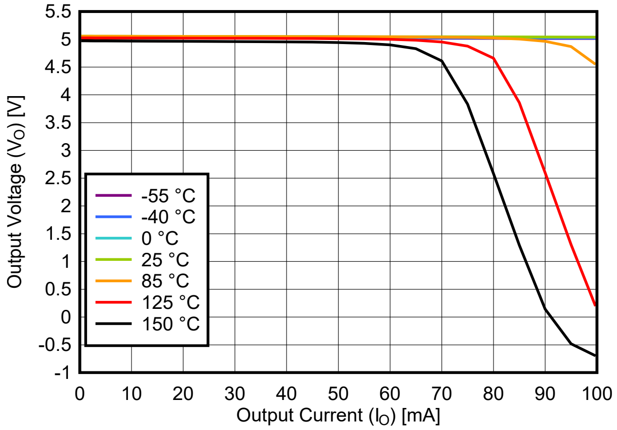
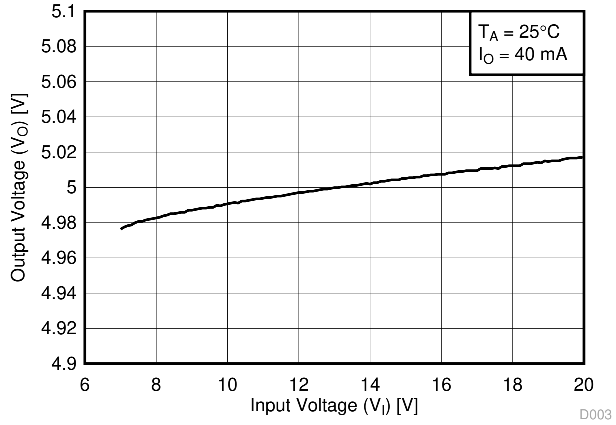


Figure 6-5. Load Regulation for New Chip



I_O = 40 mA

Figure 6-6. Line Regulation at I_O = 40 mA for Legacy Chip

6.14 Typical Characteristics (continued)

at specified junction temperature T_J = 25 °C, V_I = 10 V, V_O = 5 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF, and I_O = 1 mA (unless otherwise noted)

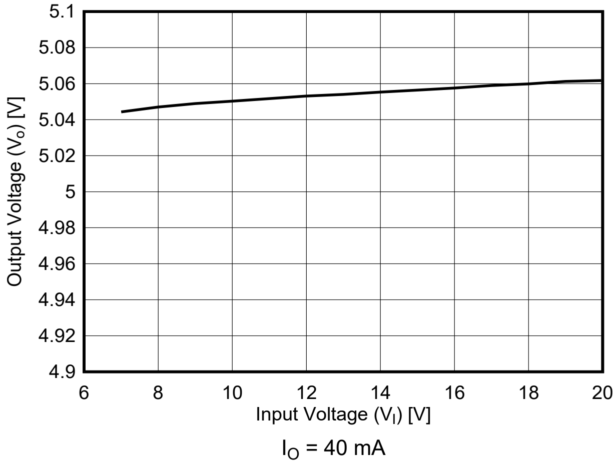


Figure 6-7. Line Regulation at I_O = 40 mA for New Chip at T_J = 25°C

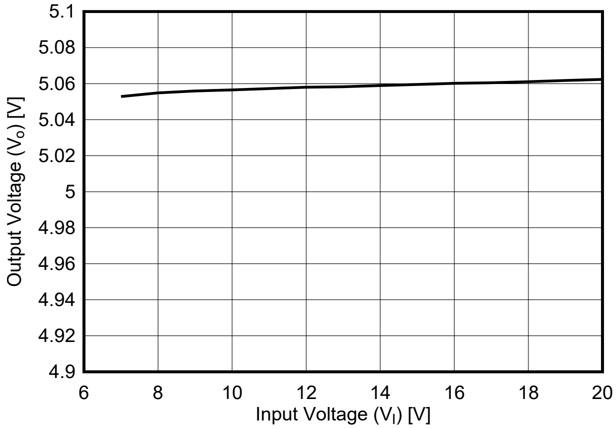


Figure 6-8. Line Regulation at I_O = 1 mA for New Chip at T_J = 25°C

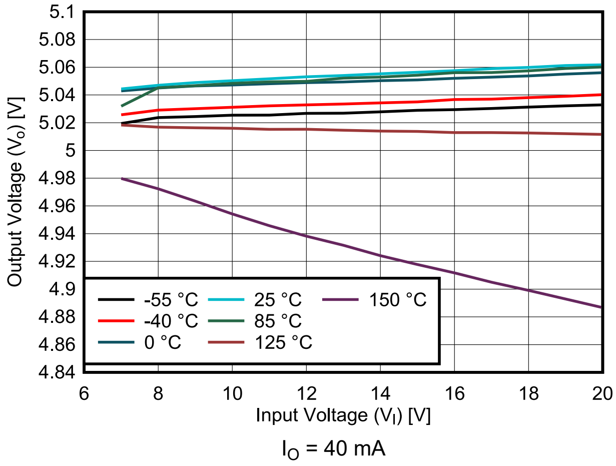


Figure 6-9. Line Regulation at I_O = 40 mA for New Chip

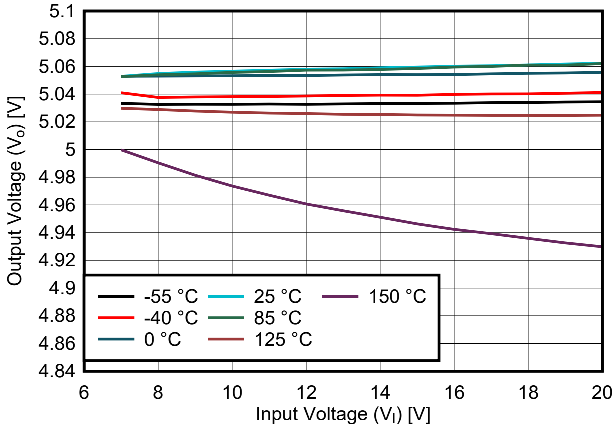


Figure 6-10. Line Regulation at I_O = 1 mA for New Chip

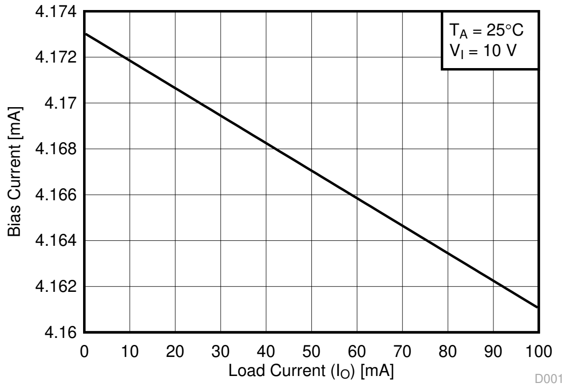


Figure 6-11. Bias Current vs Load Current for Legacy Chip

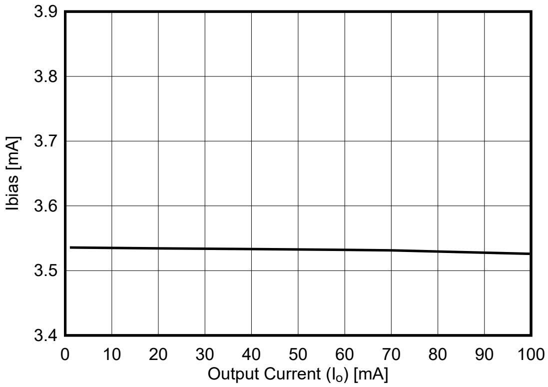


Figure 6-12. Bias Current vs Load Current for New Chip at T_J = 25°C

6.14 Typical Characteristics (continued)

at specified junction temperature T_J = 25 °C, V_I = 10 V, V_O = 5 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF, and I_O = 1 mA (unless otherwise noted)

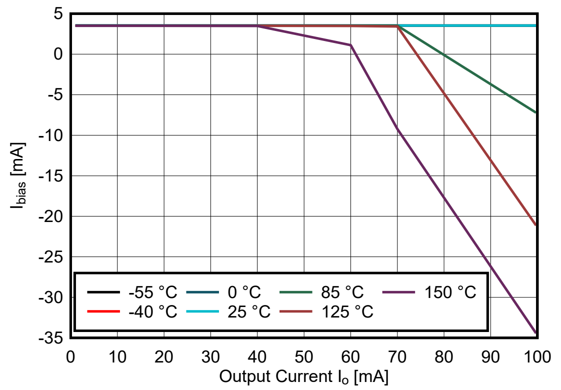
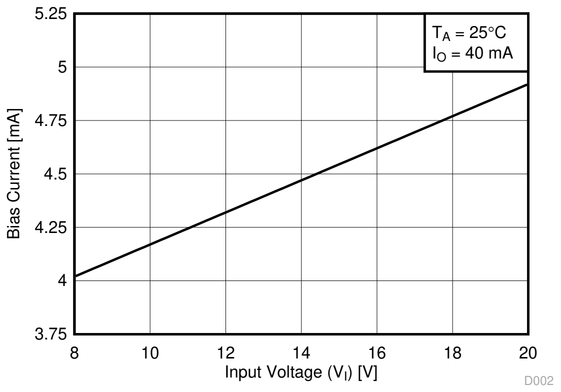
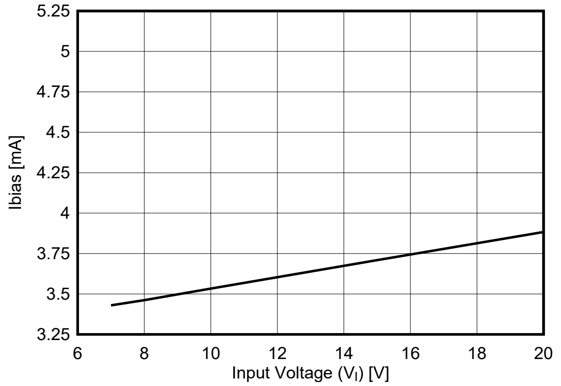


Figure 6-13. Bias Current vs Load Current for New Chip



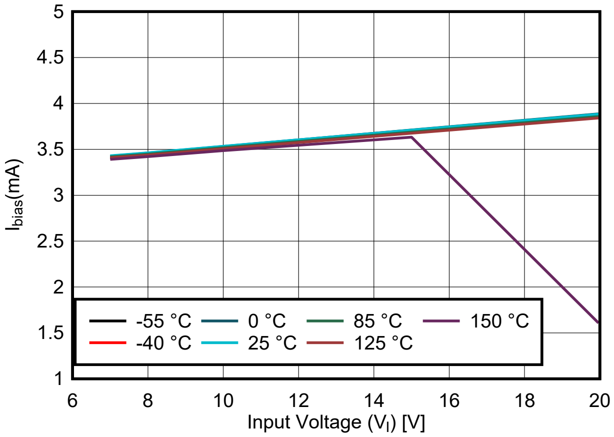
I_O = 40 mA

Figure 6-14. Bias Current vs Input Voltage for Legacy Chip



I_O = 40 mA

Figure 6-15. Bias Current vs Input Voltage for New Chip at T_J = 25°C



I_O = 40 mA

Figure 6-16. Bias Current vs Input Voltage for New Chip

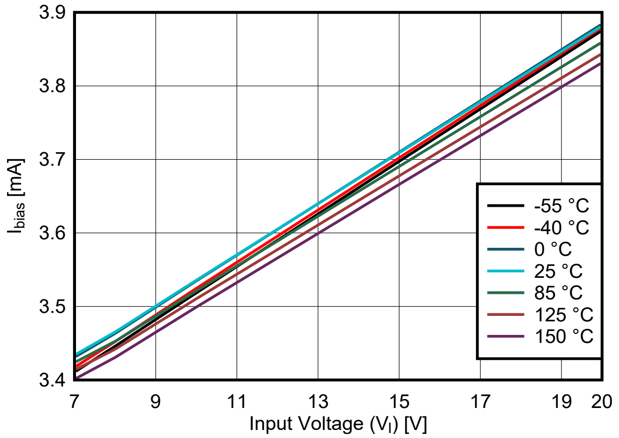
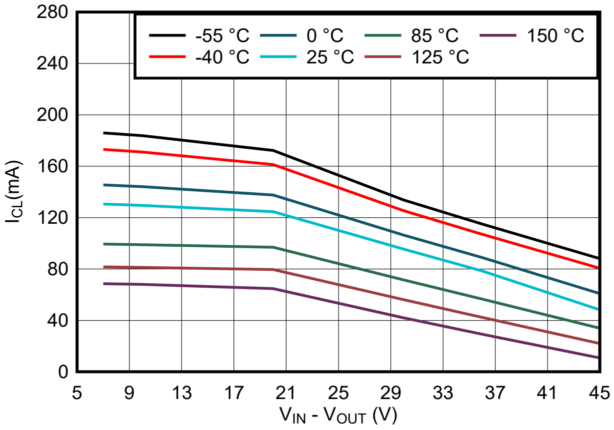


Figure 6-17. Bias Current vs Input Voltage at I_O = 1 mA for New Chip

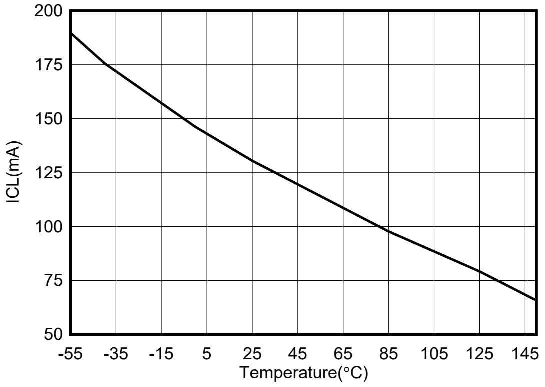


V_O = 0 V

Figure 6-18. I_{SC} vs V_I for New Chip

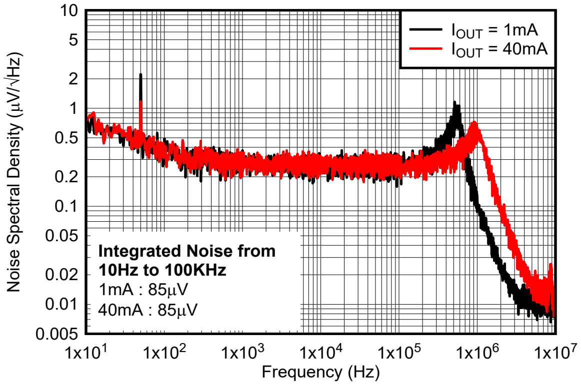
6.14 Typical Characteristics (continued)

at specified junction temperature T_J = 25 °C, V_I = 10 V, V_O = 5 V, C_{IN} = 0.33 μF, C_{OUT} = 0.1μF, and I_O = 1 mA (unless otherwise noted)



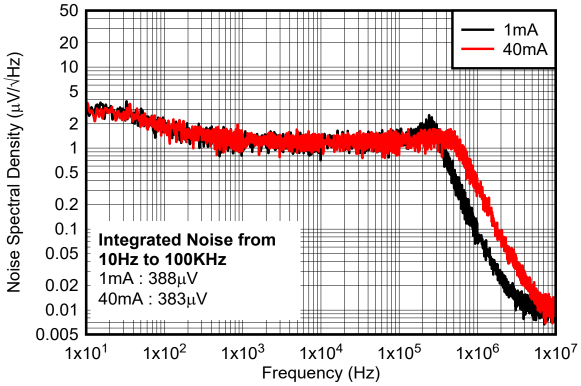
V_O = 90% of V_O (typ)

Figure 6-19. I_{CL} vs Temperature for New Chip



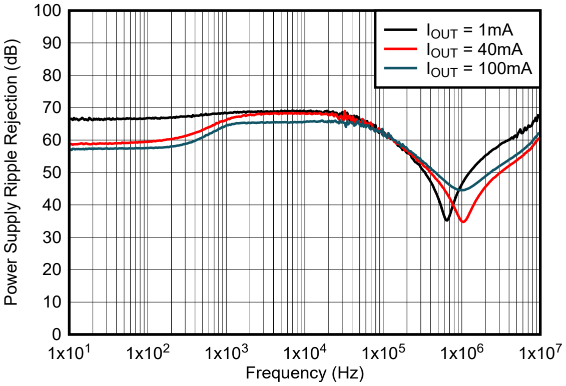
V_I = 9 V, V_O = 3.3 V

Figure 6-20. Noise Spectral Density vs Frequency and I_O for New Chip



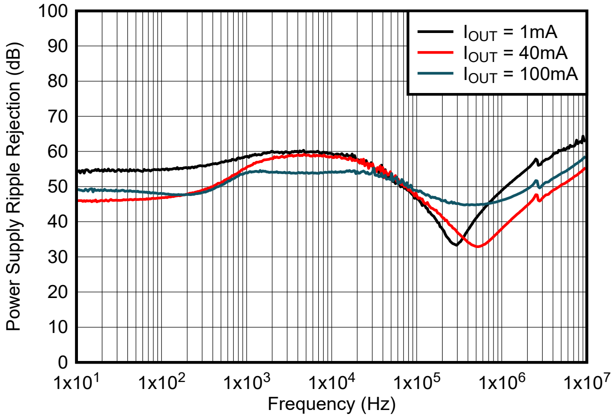
V_I = 23 V, V_O = 15 V

Figure 6-21. Noise Spectral Density vs Frequency and I_O for New Chip



V_I = 9 V, V_O = 3.3 V

Figure 6-22. PSRR vs Frequency and I_O for New Chip



V_I = 23 V, V_O = 15 V

Figure 6-23. PSRR vs Frequency and I_O for New Chip

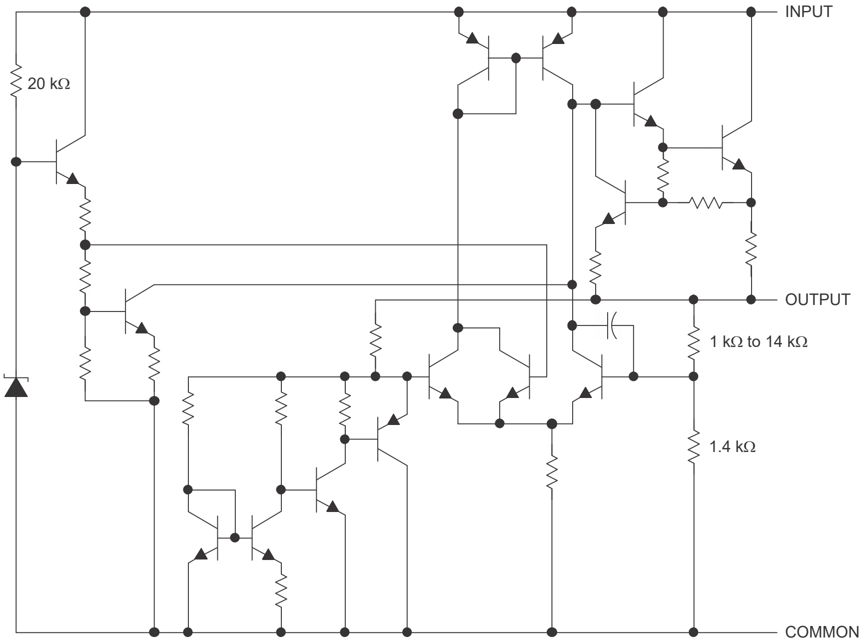
7 Detailed Description

7.1 Overview

The UA78L series of fixed-voltage, integrated-circuit voltage regulators is designed for a wide range of applications. The UA78L series supports a wide range of input voltages and can deliver 100 mA of load current.

This device features internal current-limiting and thermal shutdown mechanisms. To provide reliable operation across wide V_I ranges, the current-limiting mechanism modulates the load current capacity both by monitoring the V_O level and the difference between the V_I and V_O voltage levels. The operating ambient temperature range of the device is –40°C to +125°C for all variants of the new chip.

7.2 Functional Block Diagram



NOTE: Resistor values shown are nominal.

7.3 Feature Description

7.3.1 Current Limit

The device has an internal current-limit circuit that protects the regulator during transient high-load current faults or shorting events. In a high-load current fault, the current limit scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current-limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in current limit, the pass transistor dissipates power [$(V_I - V_O) \times I_{CL}$]. For more information on current limits, see the *Know Your Limits* application note.

To achieve a safe operation across a wide range of Input voltage, the UA78L series also has a built-in protection mechanism with current limit. The protection mechanism decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. This protection is designed to provide some output current at all values of input-to-output voltage limits defined in the *Recommended Operating Conditions* table. Figure 7-1 shows the behavior of the current limit variation.

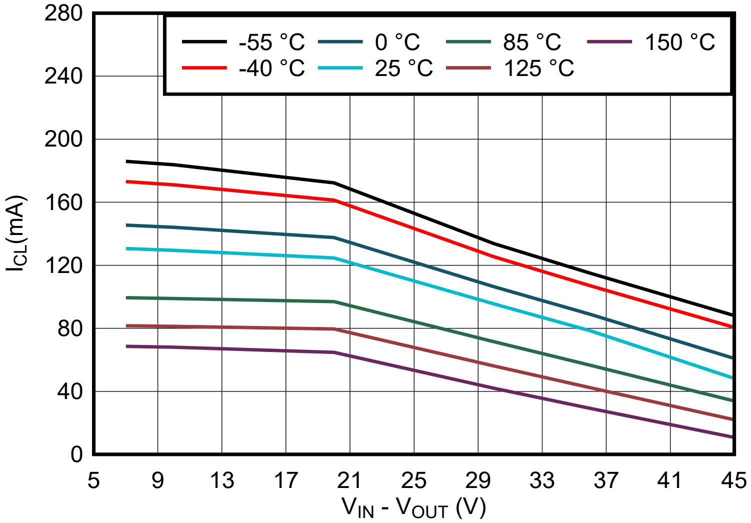


Figure 7-1. Current-Limit vs $V_{Head\text{-}room}$ Behavior for New Chip Only

7.3.2 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up can be high from large $V_I – V_O$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.3.3 Dropout Voltage (V_{DO})

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_I – V_O$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_O listed in the *Recommended Operating Conditions* table. In dropout operation, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to maintain output regulation, then the output voltage falls as well.

7.4 Device Functional Modes

Table 7-1 provides a quick comparison between the normal and dropout modes of operation.

Table 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_I	I_O
Normal	$V_I > V_{OUT(nom)} + V_{DO}$	$I_O < I_{CL}$
Dropout	$V_I < V_{OUT(nom)} + V_{DO}$	$I_O < I_{CL}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_O < I_{CL}$)
- The device junction temperature is greater than –40°C and less than +125°C

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_I < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

8 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The UA78L series is designed for use as a linear regulator with only a few external components needed. The UA78L can also be used to clean power-supply noise by attenuating ripple on the input signal.

8.2 Typical Application

The UA78L series is typically used as a fixed-output linear regulator, sourcing current up to 100 mA into a load.

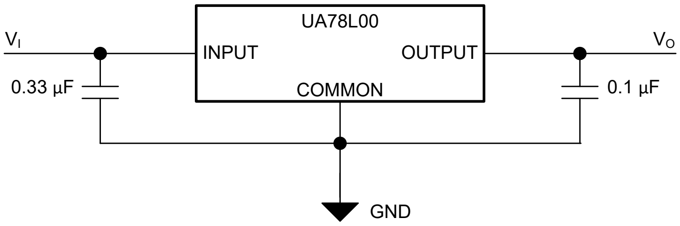


Figure 8-1. Fixed-Output Regulator

8.2.1 Design Requirements

The COMMON pin must be tied to ground to set the OUTPUT pin to the desired fixed output voltage.

Although not required, a 0.33-µF bypass capacitor is recommended on the input, and a 0.1-µF bypass capacitor is recommend on the output.

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Although both input and output capacitor are not required for stability, good analog design practice is to connect a capacitor from IN to COMMON and from OUT to COMMON. The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5 Ω. A higher value capacitor can be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of a large output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

8.2.2.2 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_I - V_O) \times I_O \quad (1)$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation, use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{2}$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance. As mentioned in the *An empirical analysis of the impact of board layout on LDO thermal performance* application note, $R_{\theta JA}$ can be improved by 35% to 55% compared to the *Thermal Information* table value with the PCB board layout optimization.

8.2.2.3 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \tag{3}$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \Psi_{JB} \times P_D \tag{4}$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

8.2.2.4 External Capacitor Requirements

The UA78L is designed to be stable without any external component. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.2.2.5 Overload Recovery

As the input voltage rises when power is first turned on, the output follows the input, allowing the regulator to start up into very heavy loads. The input-to-output voltage differential is small during start up when the input voltage is rising, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur where removing an output short does not allow the output voltage to recover. Other regulators also exhibit this phenomenon, so the behavior is not unique to the UA78L.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations occur immediately after removing a short circuit or when the shutdown pin is pulled high after the input voltage is already turned on. The load line for such a load has the possibility to intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply can possibly need to be cycled down to zero and brought up again to make the output recover to the desired voltage operating point.

8.2.2.6 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the emitter-base junction of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_O \leq V_I + 7$ V. These conditions are:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated. Limit reverse current to 5% or less of the rated output current of the device in the event this current cannot be avoided.

Figure 8-2 shows one approach for protecting the device.

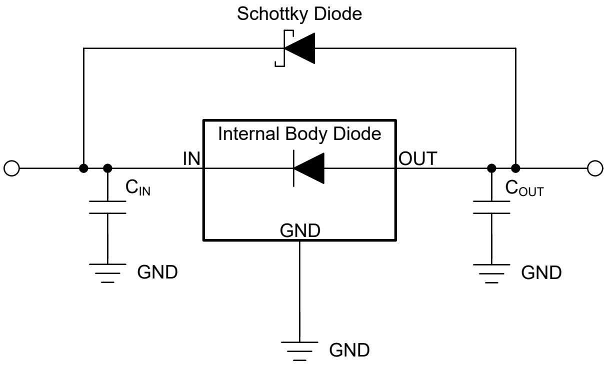


Figure 8-2. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.2.2.7 Polarity Reversal Protection

In many applications, a voltage regulator powers a load that is not connected to ground, but instead, is connected to a voltage source of the opposite polarity (for example, operational amplifiers, level-shifting circuits, and so on). During start-up and short-circuit events, this connection can lead to polarity reversal of the regulator output and can damage the internal components of the regulator.

To avoid polarity reversal on the regulator output, use external protection to protect the device.

Figure 8-3 shows one approach for protecting the device.

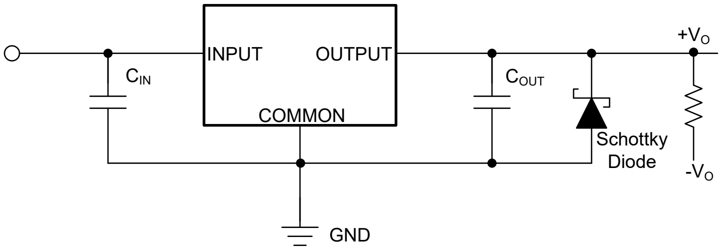


Figure 8-3. Example Circuit for Polarity Reversal Protection Using a Schottky Diode

8.2.3 Application Curves

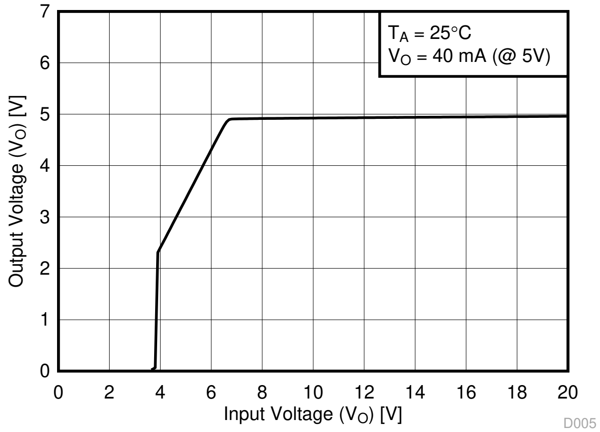


Figure 8-4. Output Voltage vs Input Voltage for Legacy Chip

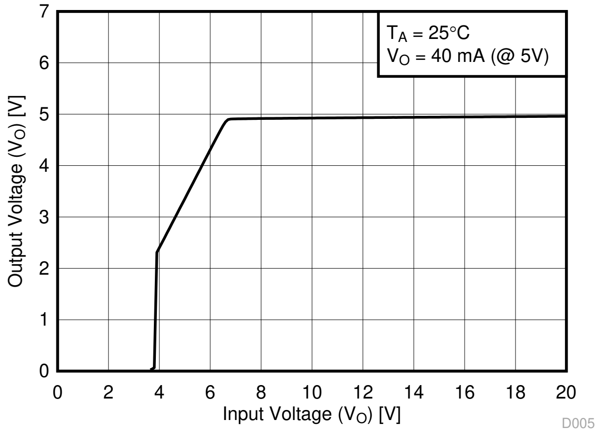
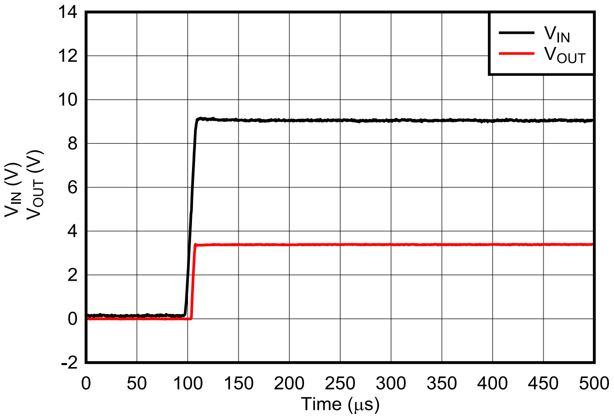
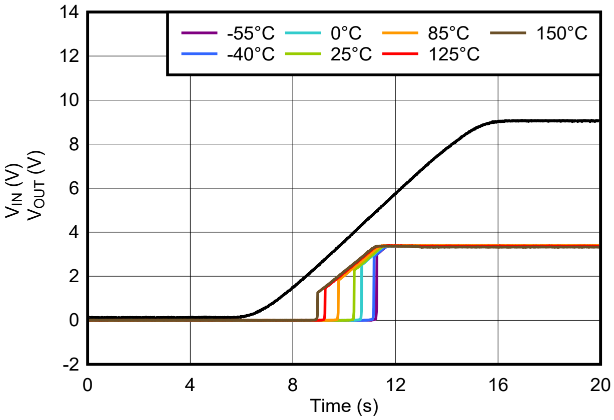


Figure 8-5. Output Voltage vs Input Voltage for New Chip



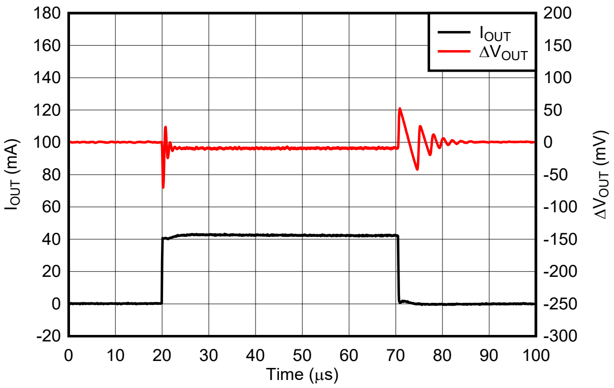
V_O = 3.3 V

Figure 8-6. Start-Up With Fast V_I Ramp for New Chip



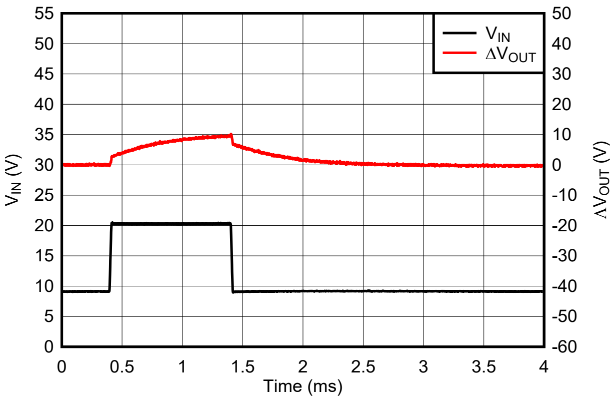
V_O = 3.3 V

Figure 8-7. Start-Up With Slow V_I Ramp Across Temperature for New Chip



V_O = 3.3 V, dI_O/dt = 1 A/µs

Figure 8-8. Load Transient Behavior for New Chip



V_O = 3.3 V, dV_{IN}/dt = 1 V/µs

Figure 8-9. Line Transient Behavior for New Chip

8.3 System Examples

8.3.1 Positive Regulator in Negative Configuration

Figure 8-10 shows the UA78L as a positive regulator used in a negative configuration.

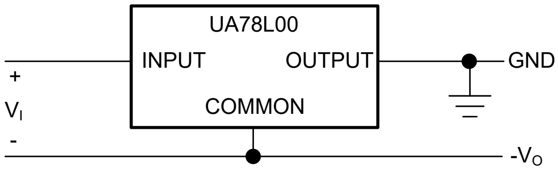


Figure 8-10. Positive Regulator in Negative Configuration (V_I Must Float)

8.3.2 Current Limiter Circuit

Figure 8-11 shows an example of using the UA78L as a current limiter. The output current limit is set by Equation 5.

$$I_O = \left(\frac{V_O}{R1}\right) + I_O \text{ Bias Current} \tag{5}$$

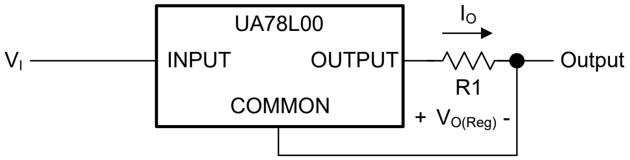


Figure 8-11. Current Limiter Example

8.4 Power Supply Recommendations

See the *Recommended Operating Conditions* table for the recommended power-supply voltages for each variation of the UA78L. Each device variant can have a different recommended maximum operating voltage.

8.5 Layout

8.5.1 Layout Guidelines

Keep trace widths large enough to eliminate problematic I×R voltage drops at the input and output pins. Place bypass capacitors as close to the UA78L as possible. Additional copper and vias connected to ground facilitate additional thermal dissipation, preventing the device from reaching thermal overload.

8.5.2 Layout Example

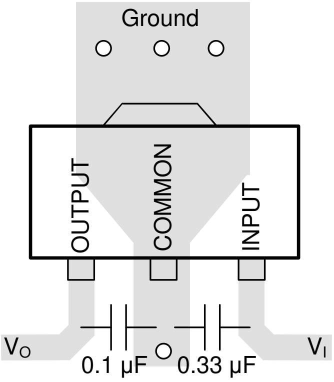


Figure 8-12. Example Layout for the PK Package

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the UA78L. The UA78LEVM-075 (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

9.1.2 Device Nomenclature

Table 9-1. Device Nomenclature[1]

PRODUCT	V_{OUT}
UA78L**xx*yyy*z** Legacy chip	**xx** is the nominal output voltage (for example, 05 = 5.0 V, 15 = 15.0 V). **yyy** is the package designator. **z** is the package quantity.
UA78L**xx*yyy*z M3** New chip	**xx** is the nominal output voltage (for example, 05 = 5.0 V, 15 = 15.0 V). **yyy** is the package designator. **z** is the package quantity. **M3** is a suffix designator for new chip redesigns on the latest TI process technology.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PUA78L033AIPK	ACTIVE	SOT-89	PK	3	1000	TBD	Call TI	Call TI	-40 to 125		Samples
PUA78L05ACPKM3	ACTIVE	SOT-89	PK	3	1000	TBD	Call TI	Call TI	-40 to 125		Samples
UA78L02ACD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L02A	
UA78L02ACDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L02A	
UA78L033AIPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	O7	Samples
UA78L033AIPKR2	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	O7	Samples
UA78L05ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACDRM3	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05A	Samples
UA78L05ACLP	LIFEBUY	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L05AC	
UA78L05ACLPE3	LIFEBUY	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L05AC	
UA78L05ACLPM	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L05AC	
UA78L05ACLPME3	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L05AC	
UA78L05ACLPR	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L05AC	
UA78L05ACLPRE3	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L05AC	
UA78L05ACPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	F5	Samples
UA78L05ACPKE6	LIFEBUY	SOT-89	PK	3	1000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	0 to 125	F5	
UA78L05ACPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	F5	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA78L05ACPKM3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	F5	Samples
UA78L05AID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05AI	
UA78L05AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05AI	Samples
UA78L05AIDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05AI	Samples
UA78L05AILP	LIFEBUY	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	78L05AI	
UA78L05AILPE3	LIFEBUY	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	78L05AI	
UA78L05AILPR	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	78L05AI	
UA78L05AILPRE3	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	78L05AI	
UA78L05AIPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	J5	Samples
UA78L05AIPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	J5	Samples
UA78L05CD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C	
UA78L05CDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C	
UA78L05CDR	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C	
UA78L05CDRE4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C	
UA78L05CLPR	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L05C	
UA78L05CPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	B5	Samples
UA78L05CPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	B5	Samples
UA78L06ACLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L06AC	Samples
UA78L06ACPK	LIFEBUY	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	F6	
UA78L06ACPKG3	LIFEBUY	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	F6	
UA78L08ACDR	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 125	78L08A	
UA78L08ACDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L08A	Samples
UA78L08ACLPR	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L08AC	
UA78L08ACLPRE3	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L08AC	
UA78L08ACPK	LIFEBUY	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	F8	
UA78L08ACPKG3	LIFEBUY	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	F8	
UA78L09ACD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L09A	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA78L09ACDR	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L09A	
UA78L09ACDRE4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L09A	
UA78L09ACLP	LIFEBUY	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L09AC	
UA78L09ACLPE3	LIFEBUY	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L09AC	
UA78L09ACLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L09AC	Samples
UA78L09ACLPRE3	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L09AC	Samples
UA78L09ACPK	LIFEBUY	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	F9	
UA78L09ACPKE6	LIFEBUY	SOT-89	PK	3	1000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	0 to 125	F9	
UA78L09ACPKG3	LIFEBUY	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	F9	
UA78L10ACD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L10A	
UA78L10ACDR	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L10A	
UA78L10ACDRE4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L10A	
UA78L10ACLP	LIFEBUY	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L10AC	
UA78L10ACLPE3	LIFEBUY	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L10AC	
UA78L10ACLPR	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L10AC	
UA78L10ACLPRE3	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L10AC	
UA78L10ACPK	LIFEBUY	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	FA	
UA78L10ACPKG3	LIFEBUY	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	FA	
UA78L12ACD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A	
UA78L12ACDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A	
UA78L12ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 125	78L12A	Samples
UA78L12ACDRE4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A	
UA78L12ACDRG4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A	
UA78L12ACDRM3	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L12A	Samples
UA78L12ACLPR	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L12AC	
UA78L12ACPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	FC	Samples
UA78L12ACPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	FC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA78L15ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L15A	Samples
UA78L15ACDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L15A	Samples
UA78L15ACDRM3	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L15A	Samples
UA78L15ACLPR	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L15AC	
UA78L15ACLPRE3	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L15AC	
UA78L15ACPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	FF	Samples
UA78L15ACPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	FF	Samples
UA78L15ACPKM3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	FF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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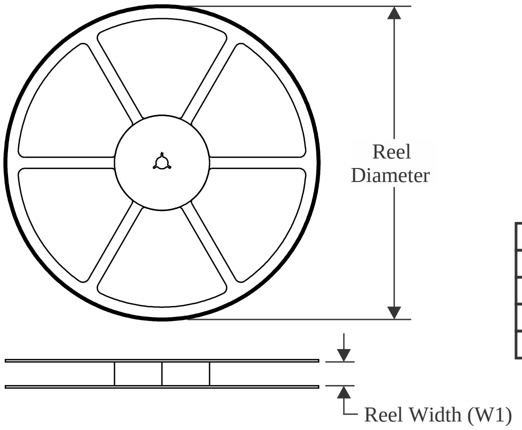
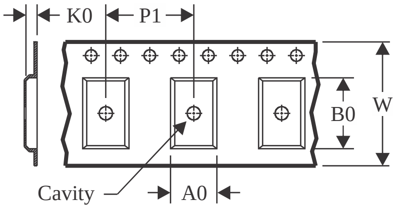
TAPE AND REEL INFORMATION

REEL DIMENSIONS

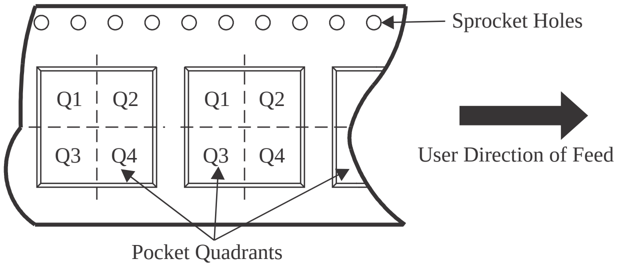


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

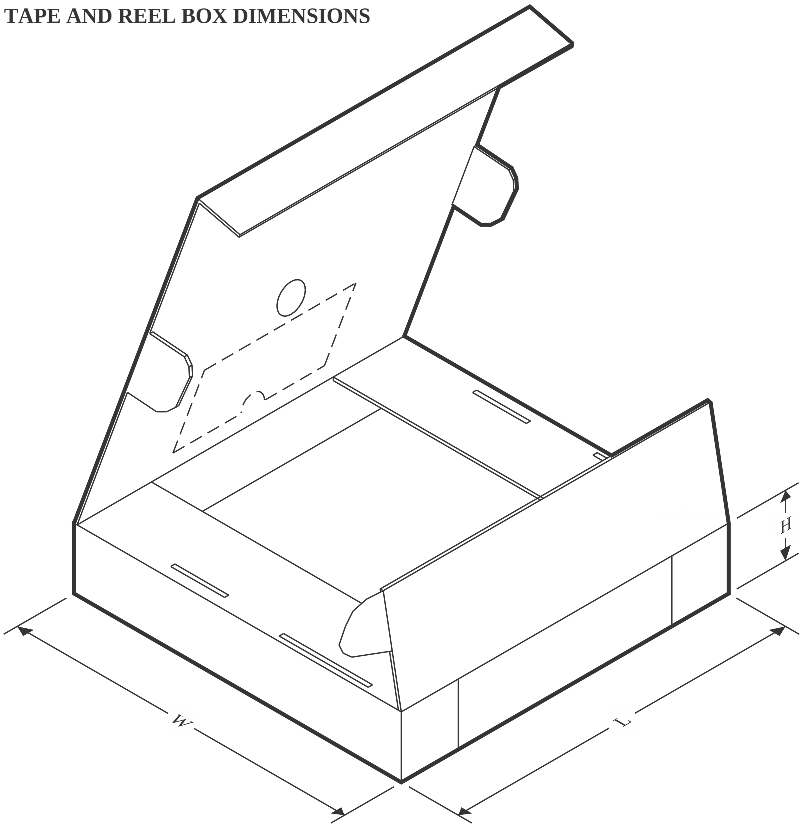


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA78L033AIPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L05ACDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05ACDRM3	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L05ACPKE6	SOT-89	PK	3	1000	180.0	13.0	4.91	4.52	1.9	8.0	12.0	Q3
UA78L05ACPKM3	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L05AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05AIPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L05CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05CPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L06ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L08ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L08ACDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L08ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L09ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L09ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA78L09ACPKE6	SOT-89	PK	3	1000	180.0	13.0	4.91	4.52	1.9	8.0	12.0	Q3
UA78L10ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L10ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L12ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L12ACDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L12ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L15ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L15ACDRM3	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L15ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L15ACPKM3	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS

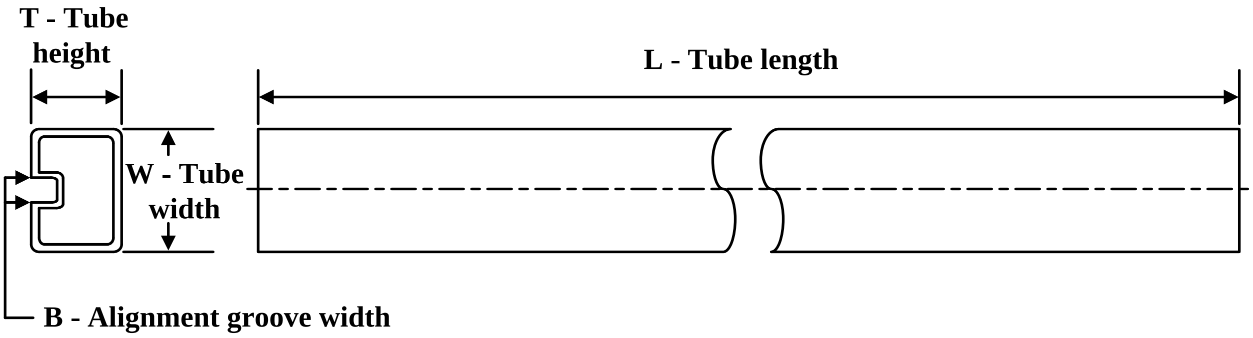


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA78L033AIPK	SOT-89	PK	3	1000	190.0	190.0	30.0
UA78L05ACDRG4	SOIC	D	8	2500	340.5	338.1	20.6
UA78L05ACDRM3	SOIC	D	8	2500	533.4	186.0	36.0
UA78L05ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L05ACPKE6	SOT-89	PK	3	1000	182.0	182.0	20.0
UA78L05ACPKM3	SOT-89	PK	3	1000	190.0	190.0	30.0
UA78L05AIDR	SOIC	D	8	2500	340.5	338.1	20.6
UA78L05AIPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L05CDR	SOIC	D	8	2500	340.5	338.1	20.6
UA78L05CPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L06ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L08ACDR	SOIC	D	8	2500	340.5	338.1	20.6
UA78L08ACDRG4	SOIC	D	8	2500	340.5	338.1	20.6
UA78L08ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L09ACDR	SOIC	D	8	2500	340.5	338.1	20.6
UA78L09ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L09ACPKE6	SOT-89	PK	3	1000	182.0	182.0	20.0
UA78L10ACDR	SOIC	D	8	2500	340.5	338.1	20.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA78L10ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L12ACDR	SOIC	D	8	2500	340.5	338.1	20.6
UA78L12ACDRG4	SOIC	D	8	2500	340.5	338.1	20.6
UA78L12ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L15ACDR	SOIC	D	8	2500	340.5	338.1	20.6
UA78L15ACDRM3	SOIC	D	8	2500	533.4	186.0	36.0
UA78L15ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L15ACPKM3	SOT-89	PK	3	1000	190.0	190.0	30.0

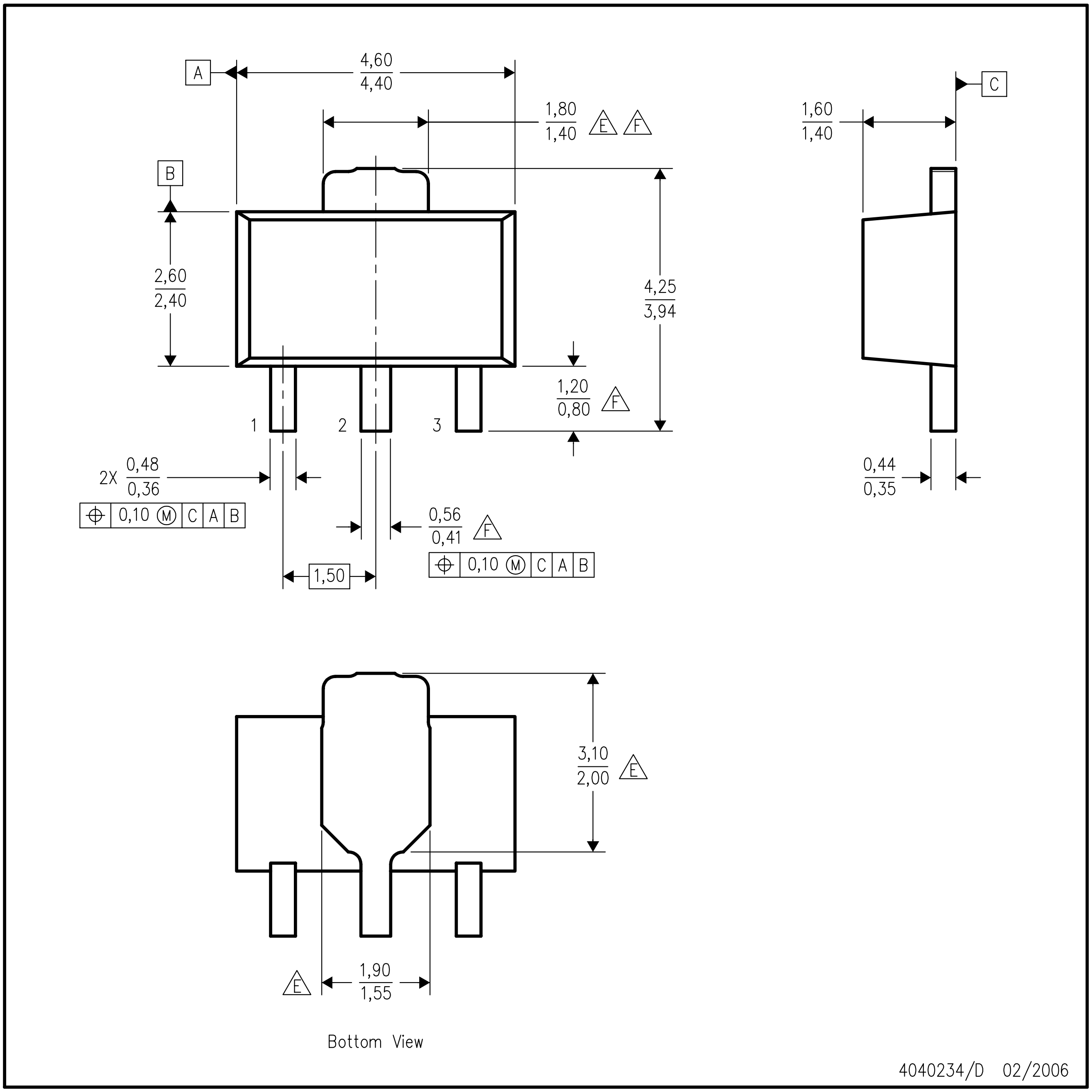
TUBE



*All dimensions are nominal

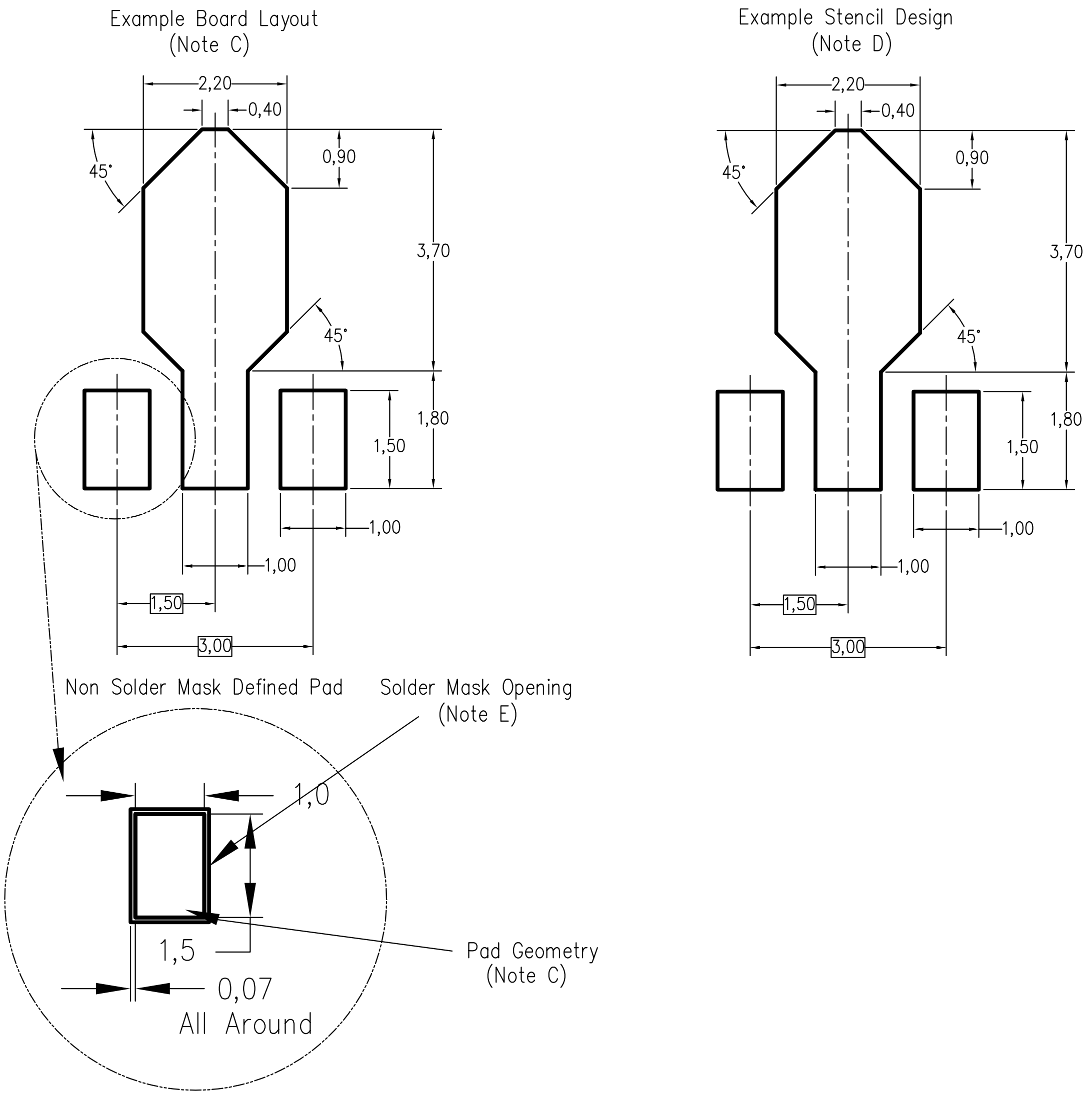
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UA78L02ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L02ACDG4	D	SOIC	8	75	507	8	3940	4.32
UA78L05ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L05ACDE4	D	SOIC	8	75	507	8	3940	4.32
UA78L05ACDG4	D	SOIC	8	75	507	8	3940	4.32
UA78L05AID	D	SOIC	8	75	507	8	3940	4.32
UA78L05CD	D	SOIC	8	75	507	8	3940	4.32
UA78L05CDG4	D	SOIC	8	75	507	8	3940	4.32
UA78L09ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L10ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L12ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L12ACDG4	D	SOIC	8	75	507	8	3940	4.32

PK (R–PSSO–F3) PLASTIC SINGLE–IN–LINE PACKAGE



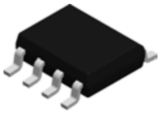
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. The center lead is in electrical contact with the tab.
- D. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
- E Thermal pad contour optional within these dimensions.
- F Falls within JEDEC TO–243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

PK (R-PDSO-G3)



4208221/A 09/06

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

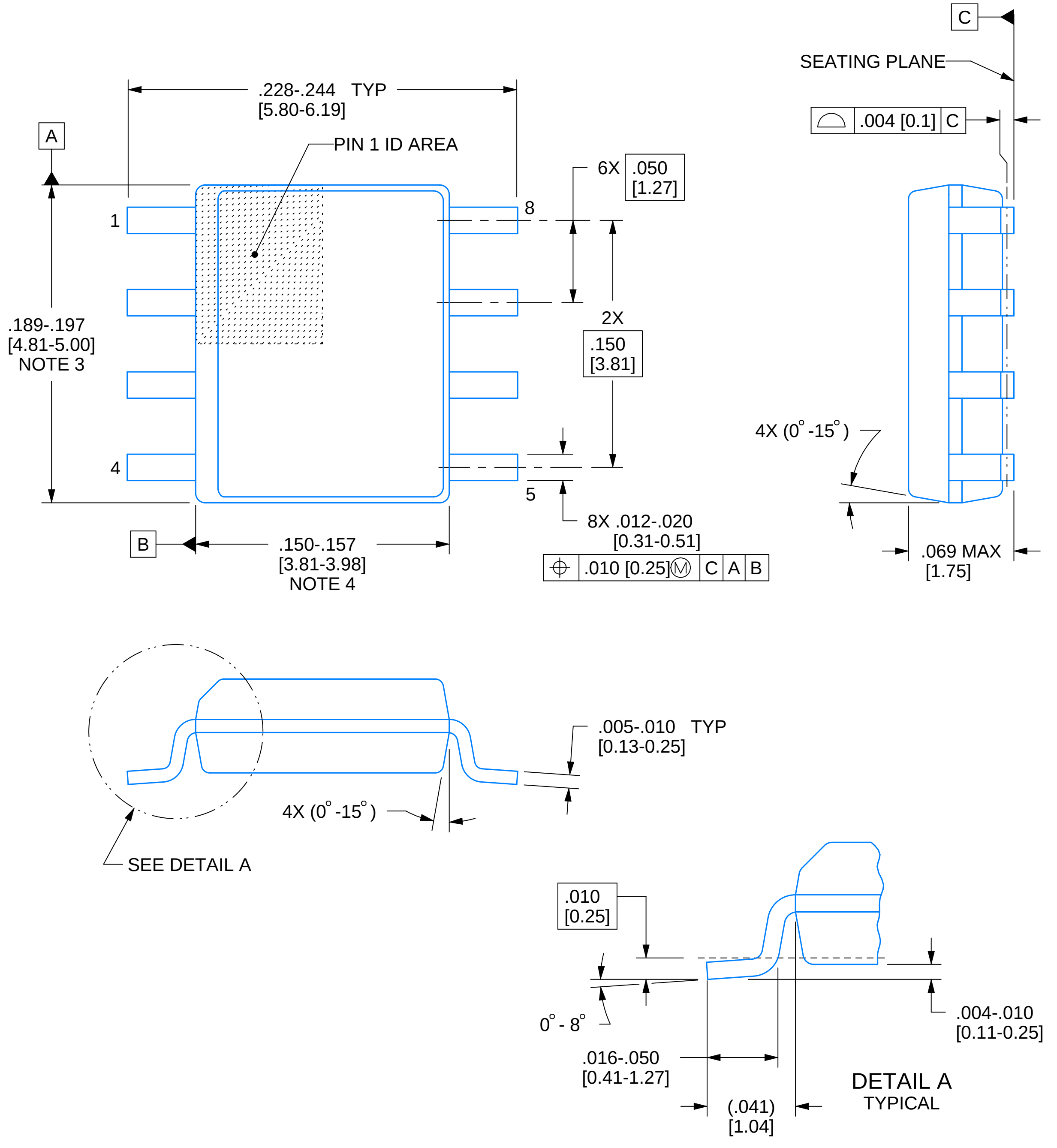


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

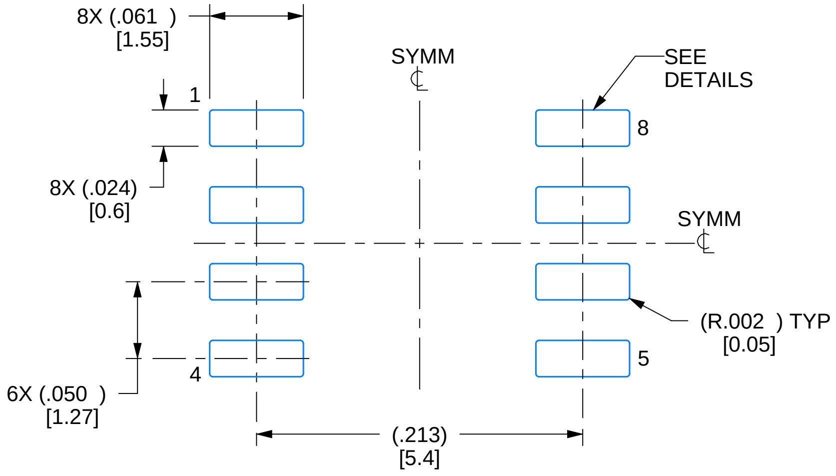
SMALL OUTLINE INTEGRATED CIRCUIT



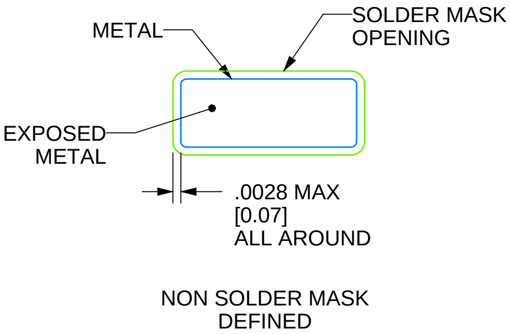
4214825/C 02/2019

NOTES:

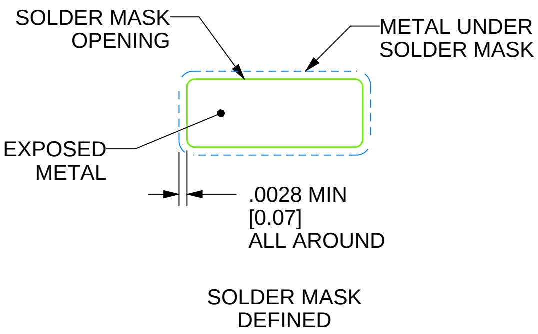
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED



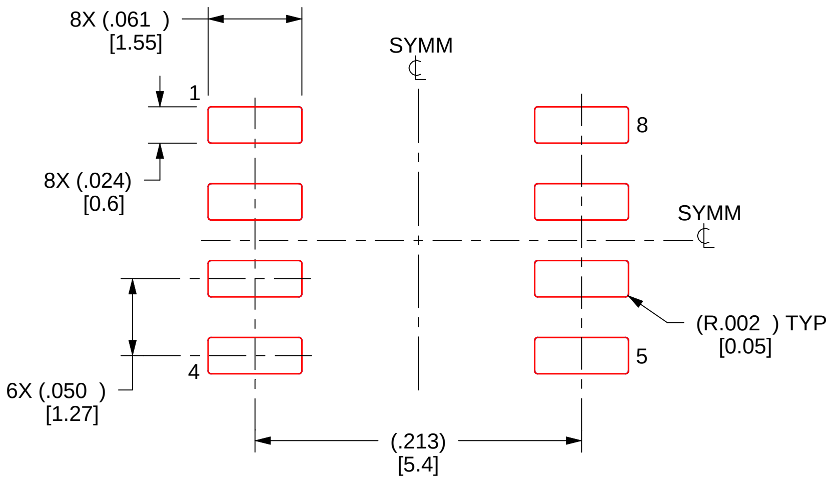
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

LP 3 **TO-92 - 5.34 mm max height**

TRANSISTOR OUTLINE

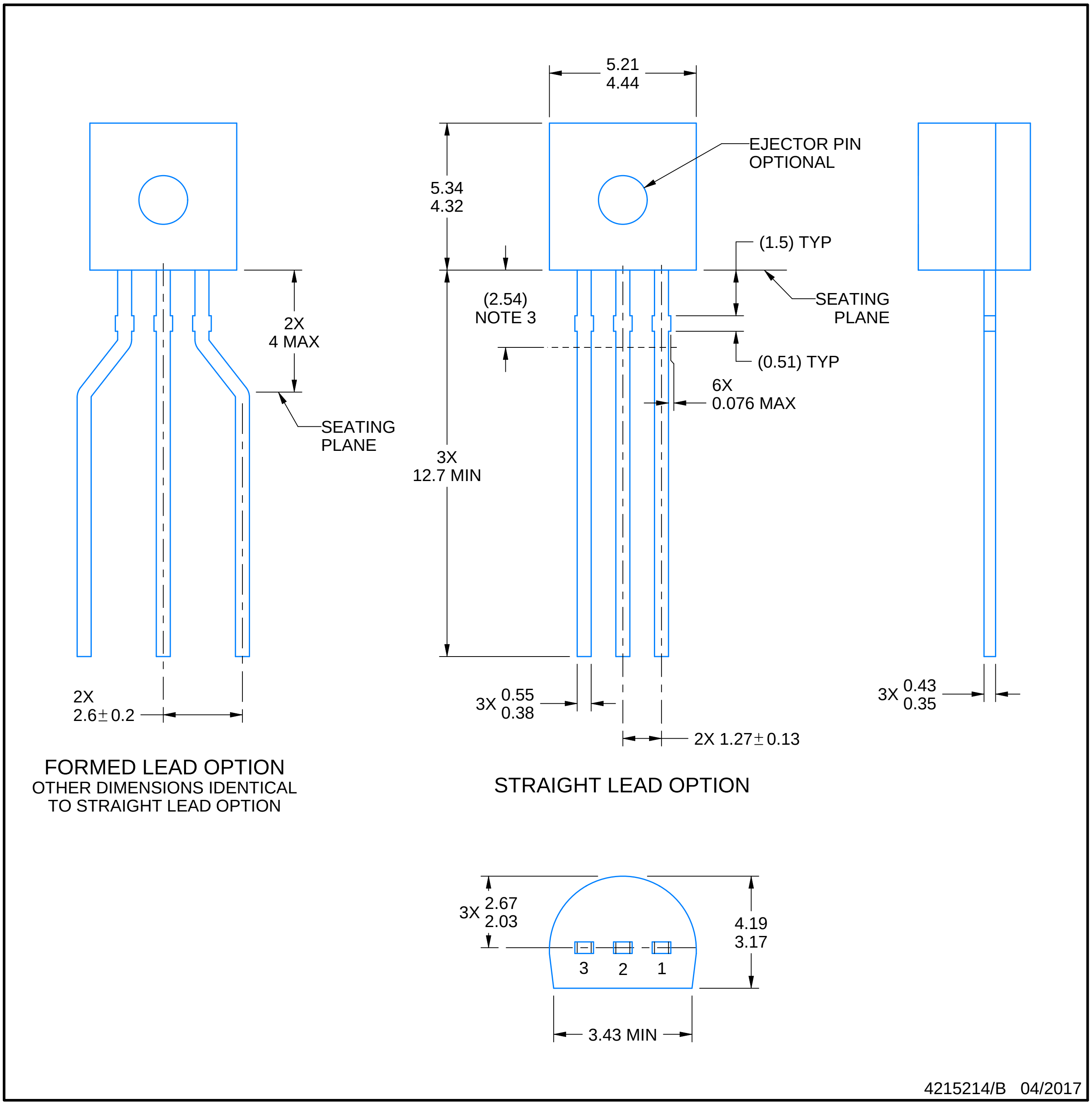
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040001-2/F

PACKAGE OUTLINE

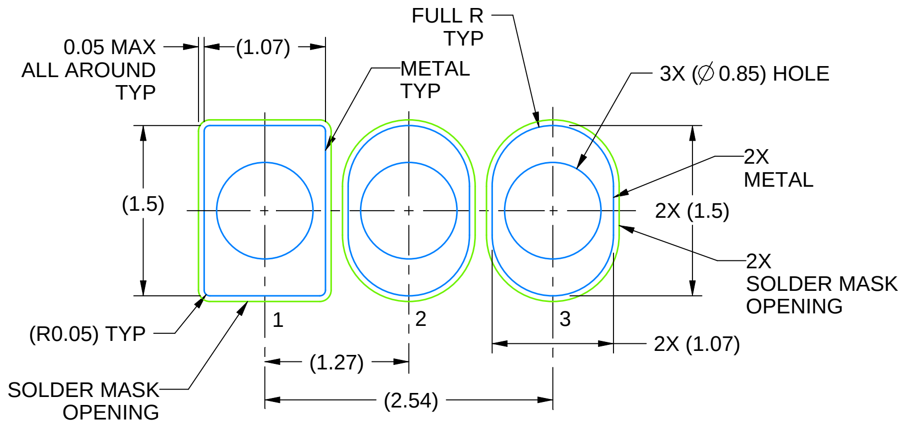
TO-92 - 5.34 mm max height

TO-92

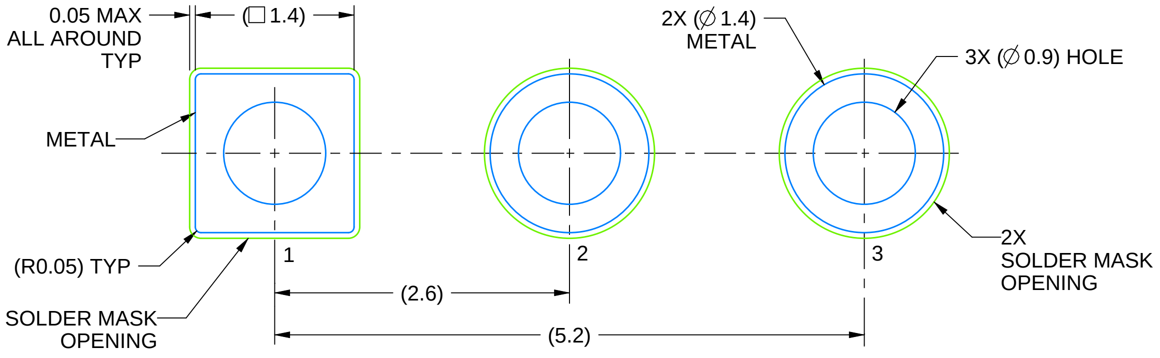


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.

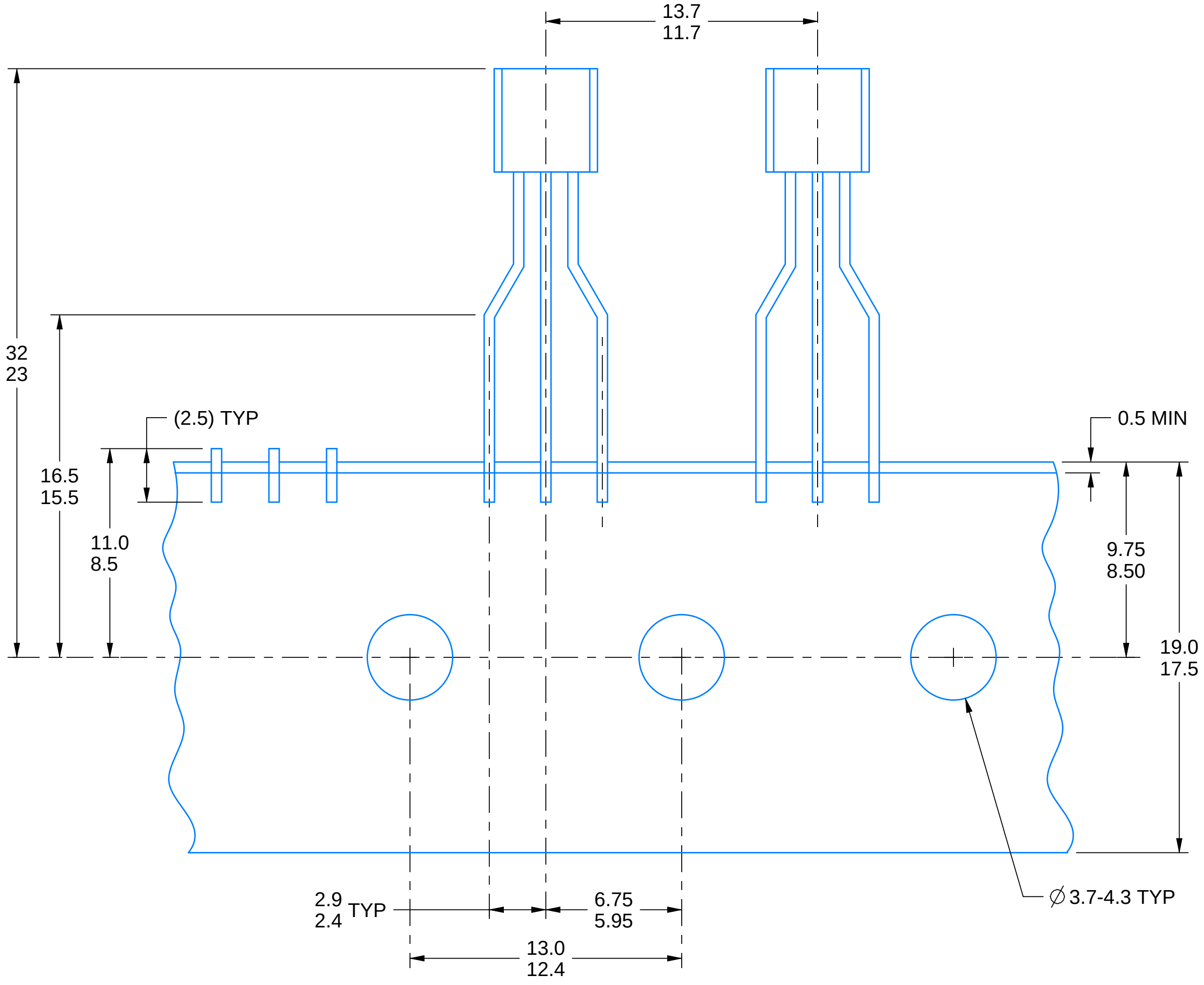


LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017



FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017

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