

IS61SF25632T/D IS61LF25632T/D
IS61SF25636T/D IS61LF25636T/D
IS61SF51218T/D IS61LF51218T/D



**256K x 32, 256K x 36, 512K x 18
 SYNCHRONOUS FLOW-THROUGH
 STATIC RAM**

FEBRUARY 2002

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Pentium™ or linear burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- Common data inputs and data outputs
- JEDEC 100-Pin TQFP and 119-pin PBGA package
- Single +3.3V, +10%, -5% power supply
- Power-down snooze mode
- 3.3V I/O for SF
- 2.5V I/O for LF
- Snooze MODE for reduced-power standby
- T version (three chip selects)
- D version (two chip selects)

DESCRIPTION

The *ISSI* IS61SF25632, IS61SF25636, IS61SF51218, IS61LF25632, IS61LF25636, and IS61LF51218 are high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance, secondary cache for the Pentium™, 680X0™, and PowerPC™ microprocessors. The IS61SF25632 and IS61LF25632 are organized as 262,144 words by 32 bits and the IS61SF25636 and IS61LF25636 are organized as 262,144 words by 36 bits. The IS61SF51218 and IS61LF51218 are organized as 524,288 words by 18 bits. Fabricated with *ISSI*'s advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers that are controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be from one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. Byte write operation is performed by using byte write enable (BWE).input combined with one or more individual byte write signals (BWx). In addition, Global Write (GW) is available for writing all bytes at one time, regardless of the byte write controls.

Bursts can be initiated with either \overline{ADSP} (Address Status Processor) or \overline{ADSC} (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the \overline{ADV} (burst address advance) input pin.

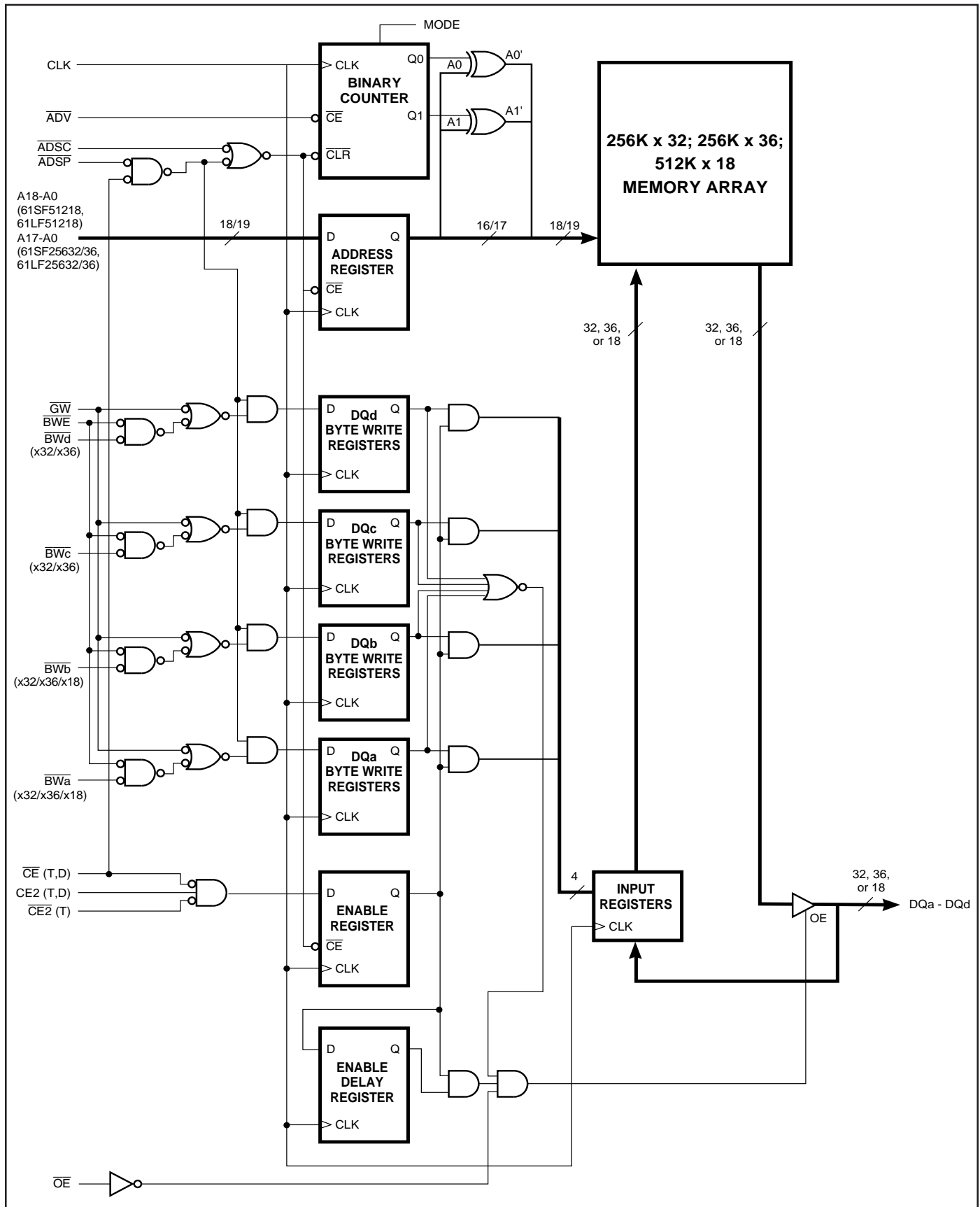
The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

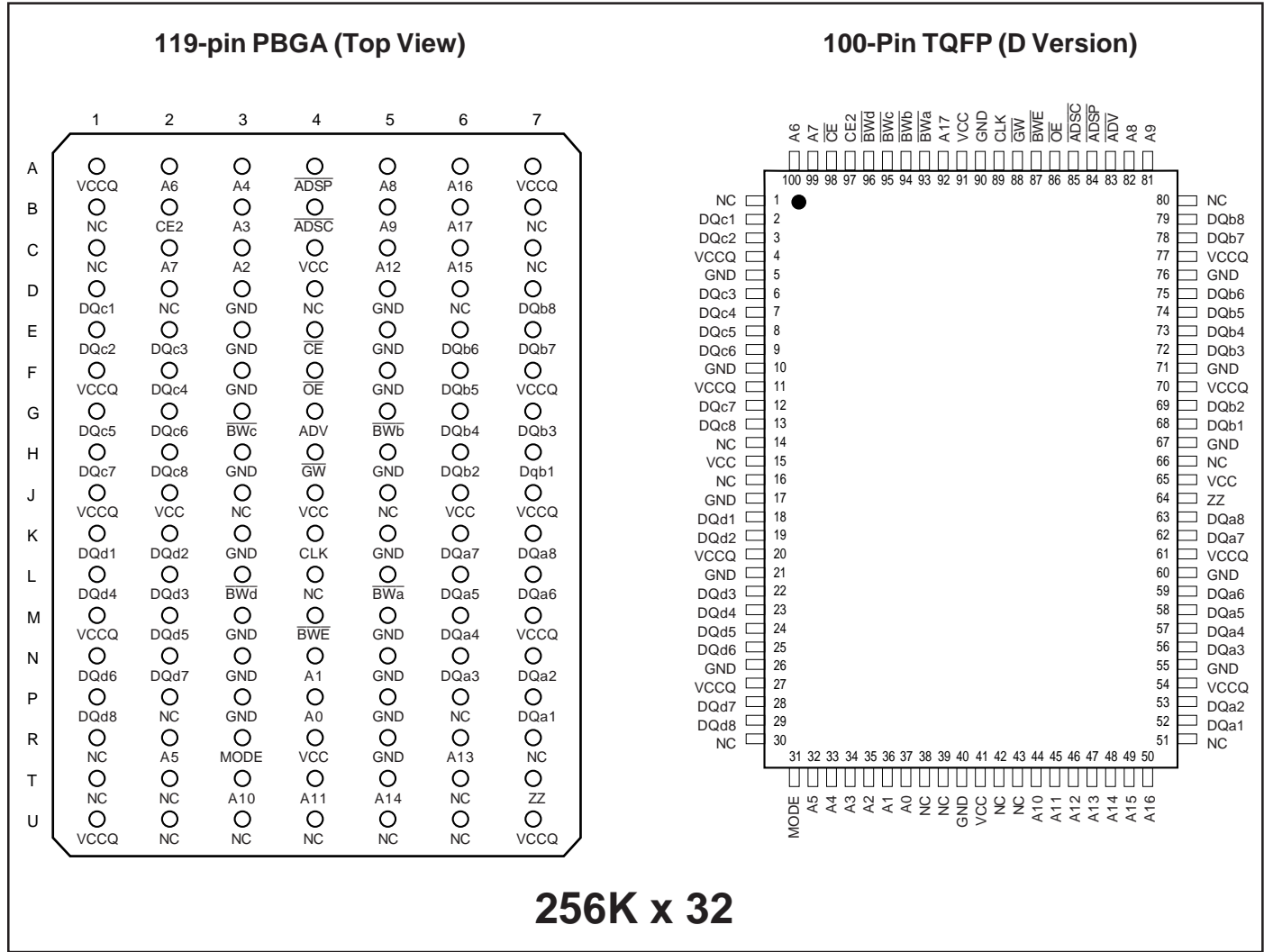
Symbol	Parameter	-8.5	-9	-10	Units
tkQ	Clock Access Time	8.5	9	10	ns
tkC	Cycle Time	11	15	15	ns
	Frequency	90	66	66	MHz

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BLOCK DIAGRAM



PIN CONFIGURATION

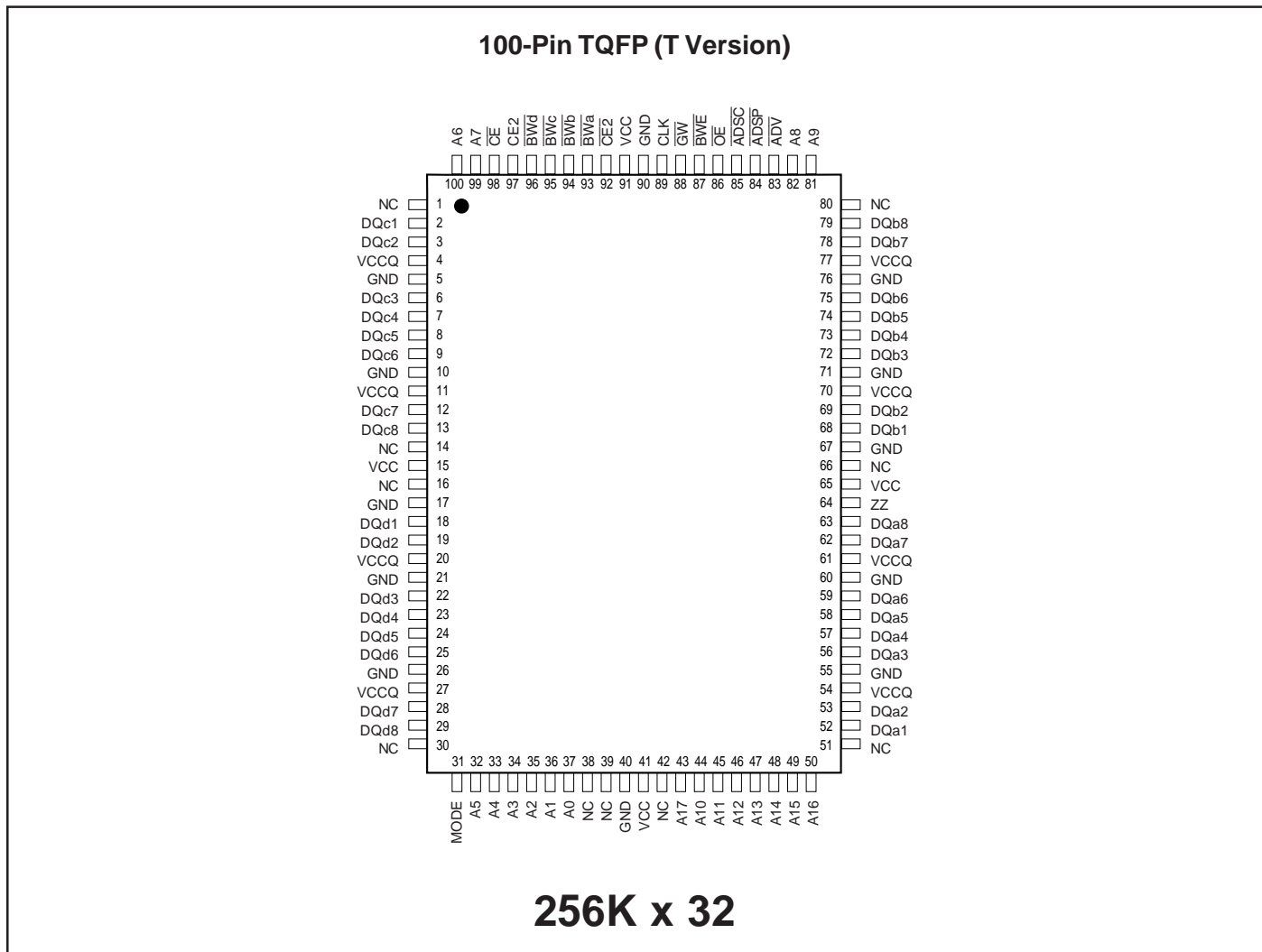


PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must be tied to the two LSBs of the address bus.
A2-A17	Synchronous Address Inputs
CLK	Synchronous Clock
ADSP	Synchronous Processor Address Status
ADSC	Synchronous Controller Address Status
ADV	Synchronous Burst Address Advance
BW _a -BW _d	Synchronous Byte Write Enable
BWE	Synchronous Byte Write Enable

GW	Synchronous Global Write Enable
CE, CE2	Synchronous Chip Enable
OE	Output Enable
DQ _a -DQ _d	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V _{cc}	+3.3V Power Supply
GND	Ground
V _{ccq}	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable

PIN CONFIGURATION

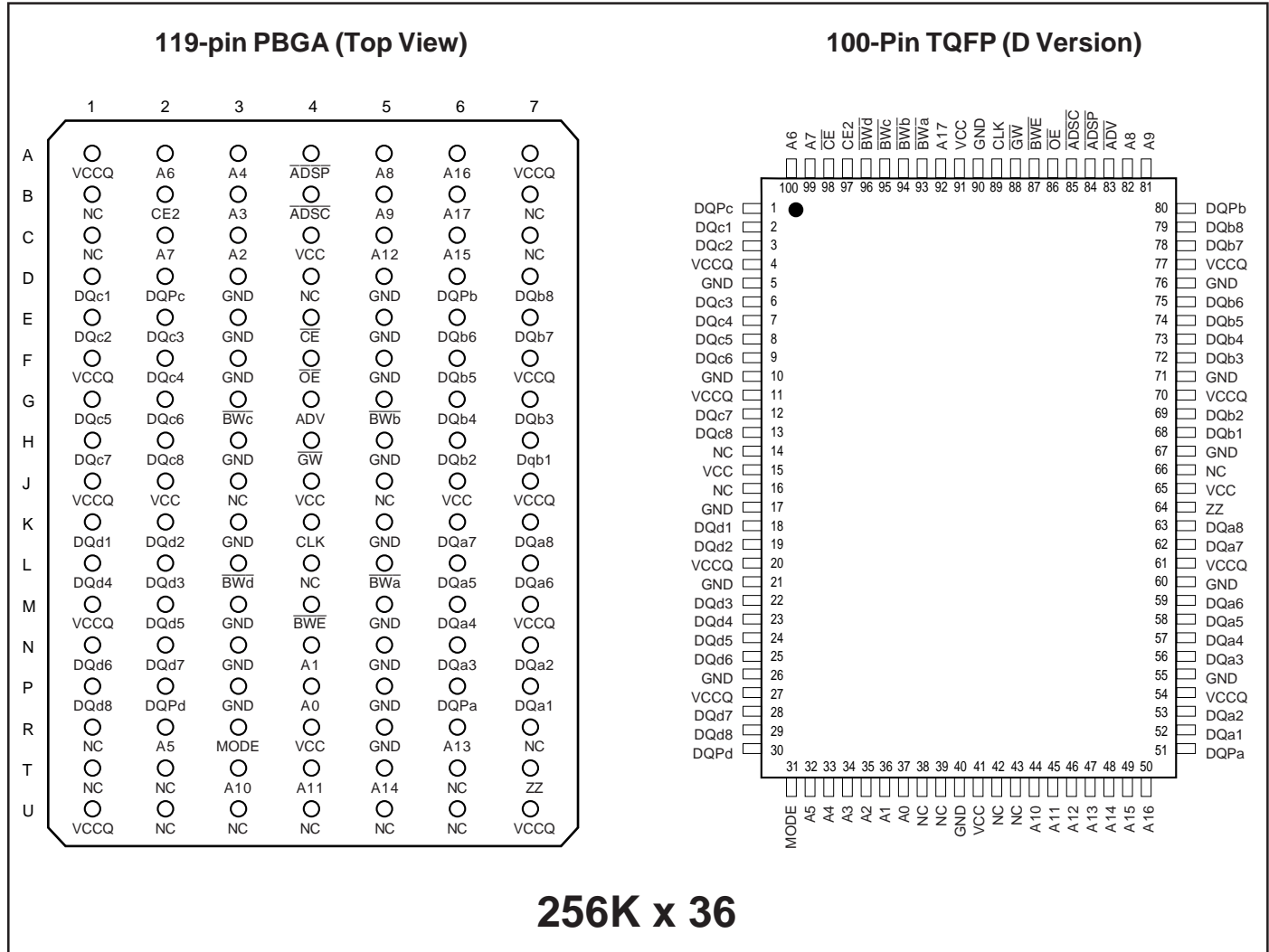


PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A17	Synchronous Address Inputs
CLK	Synchronous Clock
ADSP	Synchronous Processor Address Status
ADSC	Synchronous Controller Address Status
ADV	Synchronous Burst Address Advance
BW \bar{a} -BWD	Synchronous Byte Write Enable
BWE	Synchronous Byte Write Enable

$\bar{G}W$	Synchronous Global Write Enable
$\bar{C}E$, $\bar{C}E2$, CE2	Synchronous Chip Enable
$\bar{O}E$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
Vcc	+3.3V Power Supply
GND	Ground
Vccq	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable

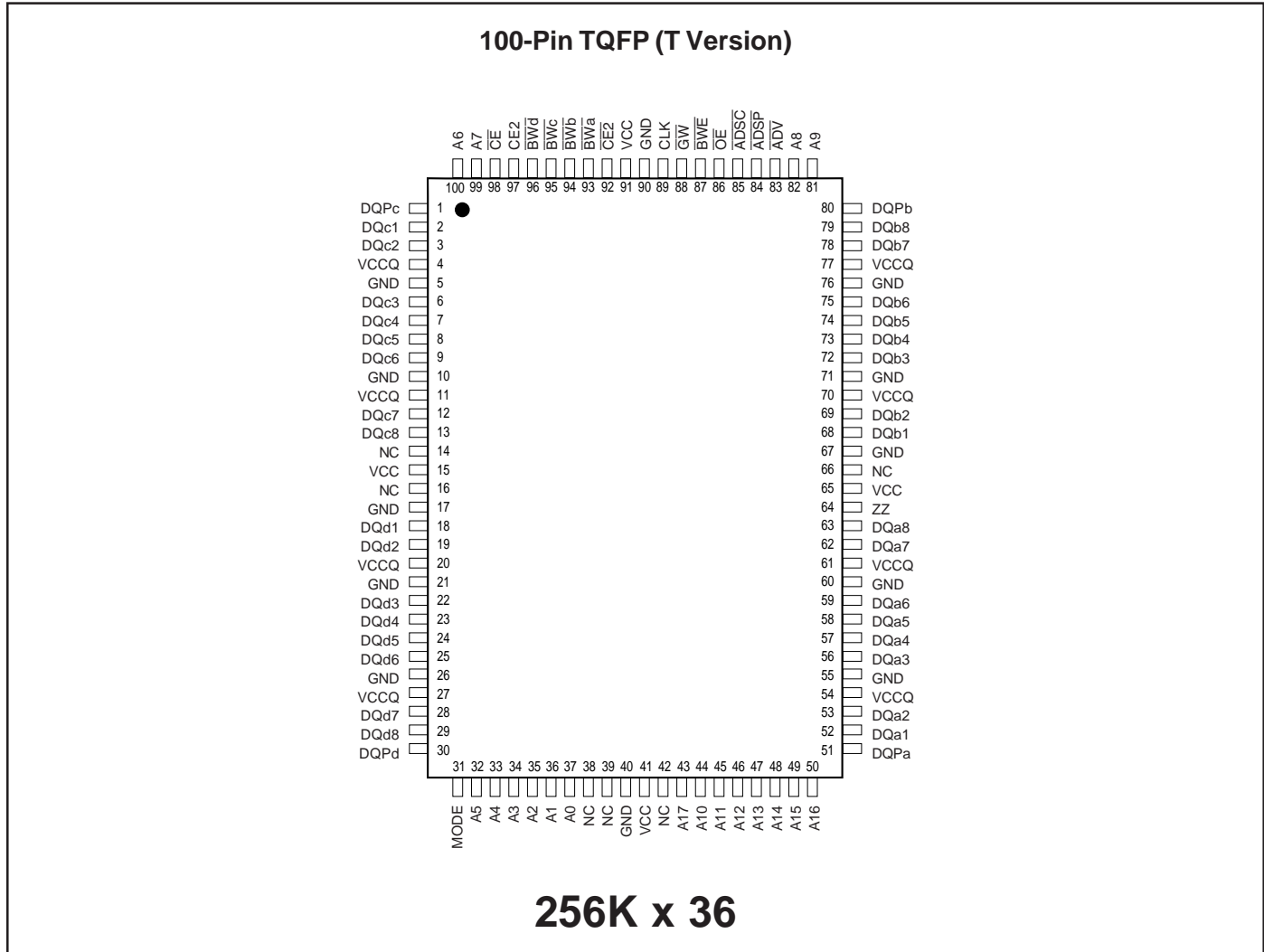
PIN CONFIGURATION



PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.	\overline{GW}	Synchronous Global Write Enable
A2-A17	Synchronous Address Inputs	\overline{CE} , CE2	Synchronous Chip Enable
CLK	Synchronous Clock	\overline{OE}	Output Enable
\overline{ADSP}	Synchronous Processor Address Status	DQa-DQd	Synchronous Data Input/Output
\overline{ADSC}	Synchronous Controller Address Status	MODE	Burst Sequence Mode Selection
\overline{ADV}	Synchronous Burst Address Advance	Vcc	+3.3V Power Supply
\overline{BWA} - \overline{BWD}	Synchronous Byte Write Enable	GND	Ground
\overline{BWE}	Synchronous Byte Write Enable	Vccq	Isolated Output Buffer Supply: +3.3V or 2.5V
		ZZ	Snooze Enable
		DQPd-DQPa	Parity Data I/O

PIN CONFIGURATION

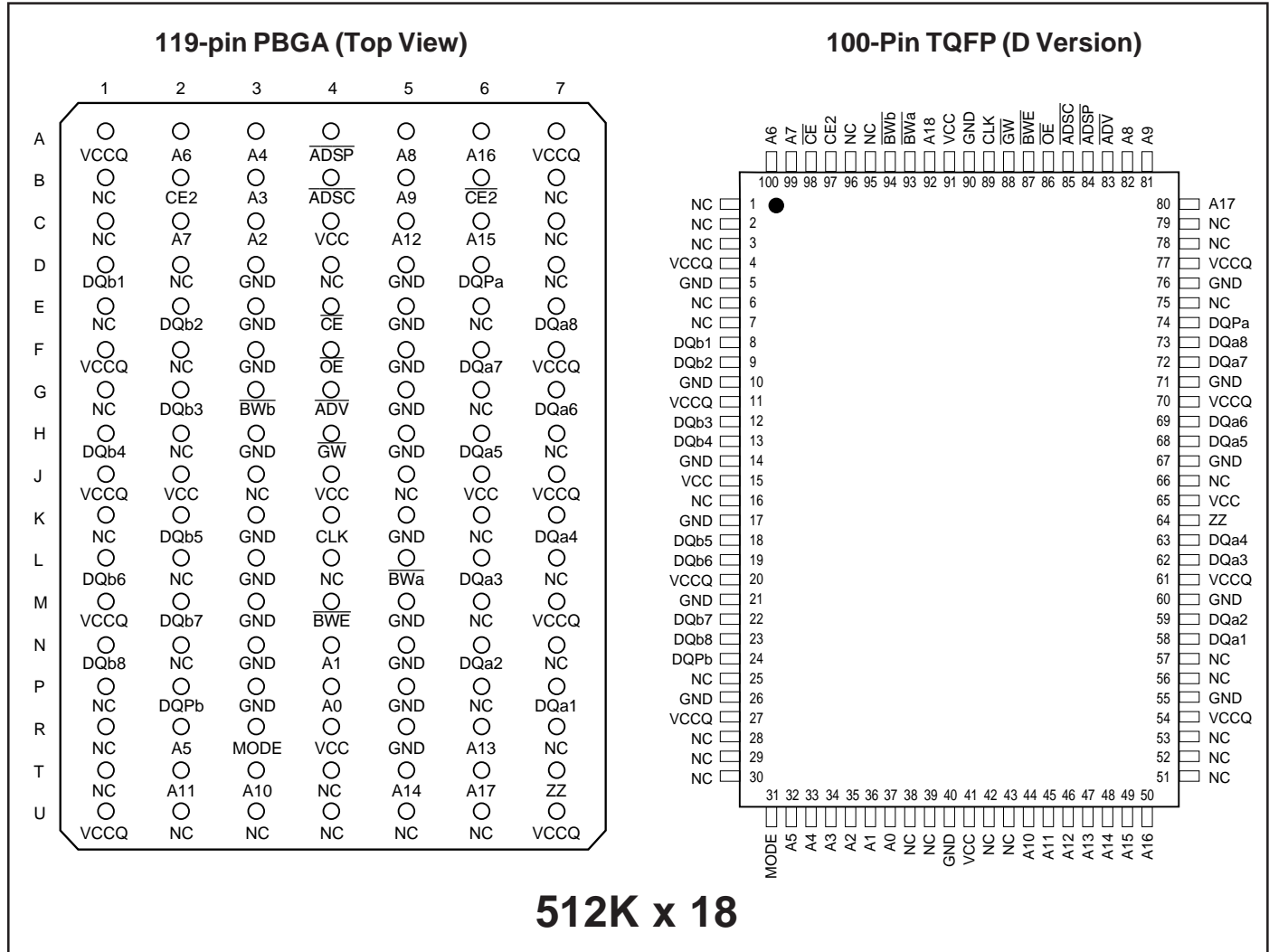


PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must be tied to the two LSBs of the address bus.
A2-A17	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{\text{ADSP}}$	Synchronous Processor Address Status
$\overline{\text{ADSC}}$	Synchronous Controller Address Status
ADV	Synchronous Burst Address Advance
$\overline{\text{BwA}}-\overline{\text{BwD}}$	Synchronous Byte Write Enable
$\overline{\text{BwE}}$	Synchronous Byte Write Enable

$\overline{\text{GW}}$	Synchronous Global Write Enable
$\overline{\text{CE}}, \overline{\text{CE2}}, \text{CE2}$	Synchronous Chip Enable
$\overline{\text{OE}}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
Vcc	+3.3V Power Supply
GND	Ground
Vccq	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable
DQPa-DQPd	Parity Data I/O

PIN CONFIGURATION

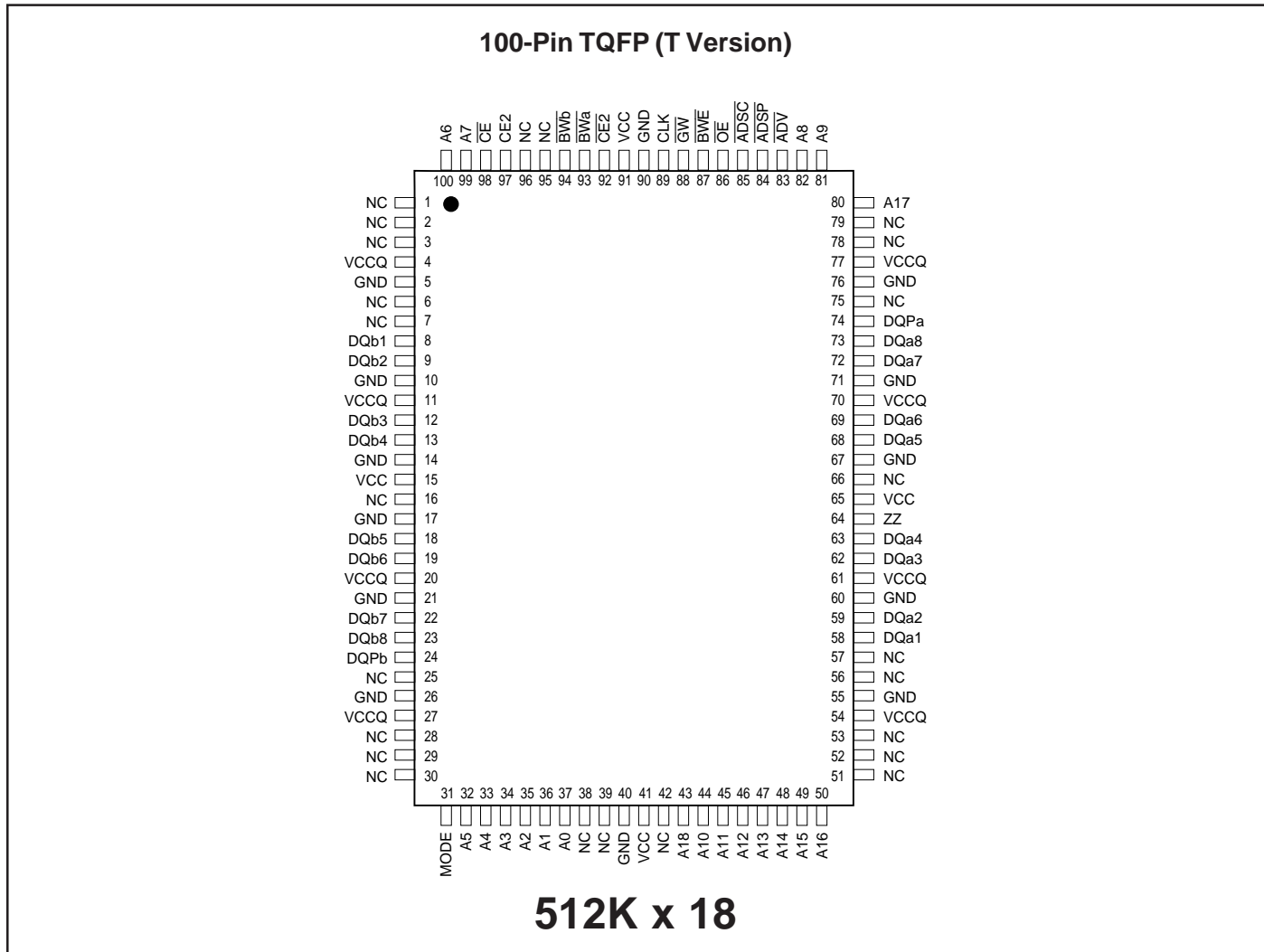


512K x 18

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.	\overline{GW}	Synchronous Global Write Enable
A2-A18	Synchronous Address Inputs	\overline{CE} , CE2	Synchronous Chip Enable
CLK	Synchronous Clock	\overline{OE}	Output Enable
\overline{ADSP}	Synchronous Processor Address Status	DQa-DQb	Synchronous Data Input/Output
\overline{ADSC}	Synchronous Controller Address Status	MODE	Burst Sequence Mode Selection
\overline{ADV}	Synchronous Burst Address Advance	Vcc	+3.3V Power Supply
\overline{BWA} - \overline{BWb}	Synchronous Byte Write Enable	GND	Ground
\overline{BWE}	Synchronous Byte Write Enable	Vccq	Isolated Output Buffer Supply: 3.3V or 2.5V
		ZZ	Snooze Enable
		DQPa-DQPb	Parity Data I/O DQPa is parity for DQa1-a8; DQPb is parity for DQb1-b8

PIN CONFIGURATION



PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.	\overline{GW}	Synchronous Global Write Enable
A2-A18	Synchronous Address Inputs	$\overline{CE}, \overline{CE2}, \overline{CE2}$	Synchronous Chip Enable
CLK	Synchronous Clock	\overline{OE}	Output Enable
\overline{ADSP}	Synchronous Processor Address Status	DQa-DQb	Synchronous Data Input/Output
\overline{ADSC}	Synchronous Controller Address Status	MODE	Burst Sequence Mode Selection
ADV	Synchronous Burst Address Advance	Vcc	+3.3V Power Supply
$\overline{BWA-BWb}$	Synchronous Byte Write Enable	GND	Ground
\overline{BWE}	Synchronous Byte Write Enable	Vccq	Isolated Output Buffer Supply: 3.3V or 2.5V
		ZZ	Snooze Enable
		DQPa-DQPb	Parity Data I/O DQPa is parity for DQa1-a8; DQPb is parity for DQb1-b8

TRUTH TABLE

Operation	Address									
	Used	\overline{CE}	CE2	$\overline{CE2}$	\overline{ADSP}	\overline{ADSC}	\overline{ADV}	\overline{WRITE}	\overline{OE}	DQ
Deselected, Power-down	None	H	X	X	X	L	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	H	L	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	H	L	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	Q
Read Cycle, Begin Burst	External	L	H	L	H	L	X	Read	X	Q
Write Cycle, Begin Burst	External	L	H	L	H	L	X	Write	X	D
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	Write	X	D
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	Write	X	D
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	Write	X	D
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	Write	X	D

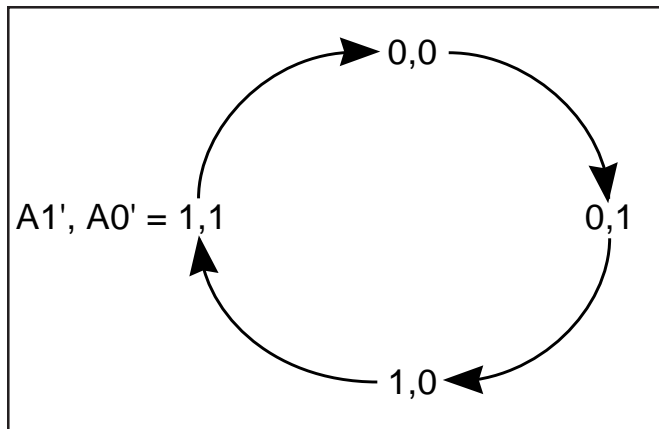
PARTIAL TRUTH TABLE

Function	\overline{GW}	\overline{BWE}	\overline{Bwa}	\overline{Bwb}	\overline{Bwc}	\overline{Bwd}
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{CCQ} or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND_Q)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
T _{BIAS}	Temperature Under Bias	-40 to +85	°C
T _{STG}	Storage Temperature	-55 to +150	°C
P _D	Power Dissipation	1.6	W
I _{OUT}	Output Current (per I/O)	100	mA
V _{IN} , V _{OUT}	Voltage Relative to GND for I/O Pins	-0.5 to V _{CCQ} + 0.3	V
V _{IN}	Voltage Relative to GND for for Address and Control Inputs	-0.5 to V _{CC} + 0.5	V
V _{CC}	Voltage on V _{CC} Supply Relative to GND	-0.5 to 4.6	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	V _{CC}	V _{CCQ}
Commercial	0°C to +70°C	3.3V, +10%, -5%	2.375–3.6V
Industrial	-40°C to +85°C	3.3V, +10%, -5%	2.375–3.6V

DC ELECTRICAL CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit	
V _{OH}	Output HIGH Voltage	I _{OH} = -2.0 mA, V _{CCQ} = 2.5V	1.7	—	V	
		I _{OH} = -4.0 mA, V _{CCQ} = 3.3V	2.4	—	V	
V _{OL}	Output LOW Voltage	I _{OL} = 2.0 mA, V _{CCQ} = 2.5V	—	0.7	V	
		I _{OL} = 8.0 mA, V _{CCQ} = 3.3V	—	0.4	V	
V _{IH}	Input HIGH Voltage	V _{CCQ} = 2.5V	1.7	V _{CCQ} + 0.3	V	
		V _{CCQ} = 3.3V	2.0	V _{CCQ} + 0.3	V	
V _{IL}	Input LOW Voltage	V _{CCQ} = 2.5V	-0.3	0.7	V	
		V _{CCQ} = 3.3V	-0.3	0.8	V	
I _{LI}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CCQ} ⁽²⁾	Com.	-2	2	μA
			Ind.	-5	5	
I _{LO}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CCQ} , $\overline{OE} = V_{IH}$	Com.	-2	2	μA
			Ind.	-5	5	

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	-8.5 Max.	-9 Max.	-10 Max.	Unit	
I _{CC}	AC Operating Supply Current	Device Selected, All Inputs = V _{IL} or V _{IH} $\overline{OE} = V_{IH}$, V _{CC} = Max. Cycle Time ≥ t _{kc} min.	Com.	200	175	150	mA
			Ind.		185	160	mA
I _{SB}	Standby Current	Device Deselected, V _{CC} = Max., All Inputs = V _{IH} or V _{IL} CLK Cycle Time ≥ t _{kc} min.	Com.	20	20	20	mA
			Ind.		25	25	mA

Notes:

1. The MODE pin has an internal pullup. This pin may be a No Connect, tied to GND, or tied to V_{CC}.
2. The MODE pin should be tied to V_{CC} or GND. It exhibits ±10 μA maximum leakage current when tied to - GND + 0.2V or ≥ V_{CC} - 0.2V.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V for 3.3V I/O V _{CCQ} /2 for 2.5V I/O
Output Load	See Figures 1 and 2

AC TEST LOADS

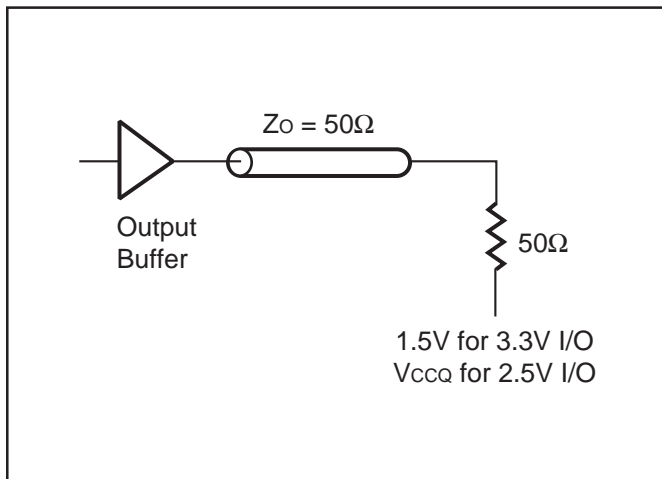


Figure 1

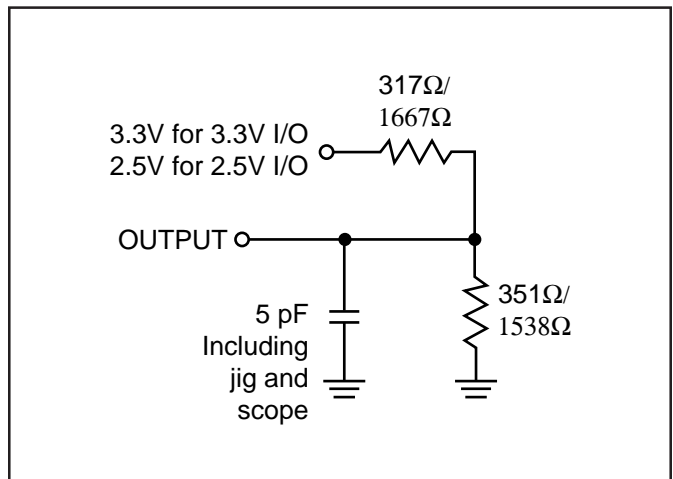


Figure 2

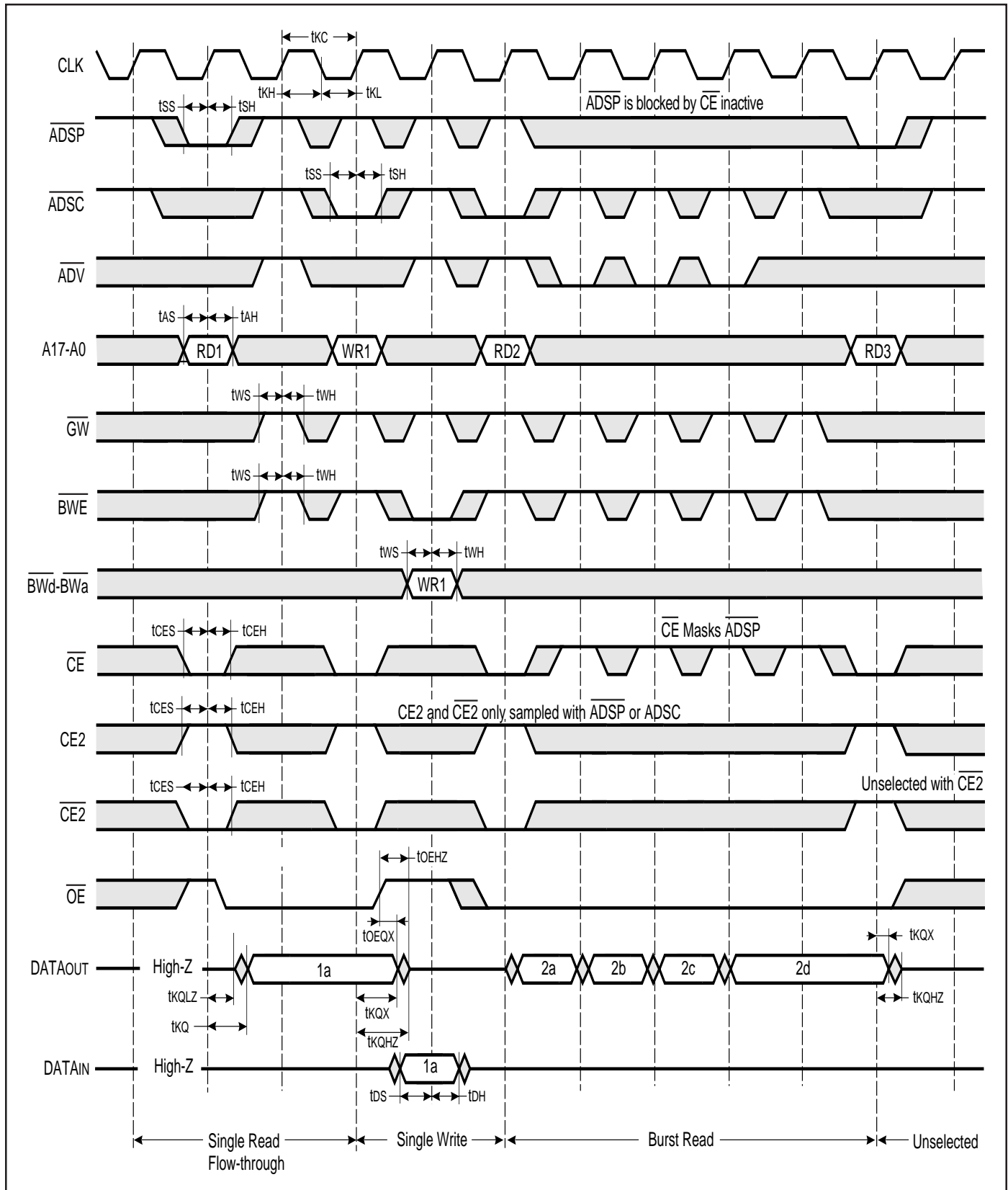
READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-8.5		-9		-10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}	Clock Frequency	—	90	—	66	—	66	MHz
t _{KC}	Cycle Time	10	—	15	—	15	—	ns
t _{KH}	Clock High Pulse Width	3.0	—	4.0	—	4.0	—	ns
t _{KL}	Clock Low Pulse Width	3.0	—	4.0	—	4.0	—	ns
t _{KQ}	Clock Access Time	—	8.5	—	9	—	10	ns
t _{KQX} ⁽¹⁾	Clock High to Output Invalid	2	—	2	—	2	—	ns
t _{KQLZ} ^(1,2)	Clock High to Output Low-Z	0	—	0	—	0	—	ns
t _{KQHZ} ^(1,2)	Clock High to Output High-Z	2	3.8	2	4	1.5	4.2	ns
t _{OEQ}	Output Enable to Output Valid	—	3.8	—	4	—	5	ns
t _{OELZ} ^(1,2)	Output Enable to Output Low-Z	0	—	0	—	0	—	ns
t _{OEHZ} ^(1,2)	Output Enable to Output High-Z	—	3.8	—	4	—	5	ns
t _{AS}	Address Setup Time	1.8	—	2	—	2	—	ns
t _{SS}	Address Status Setup Time	1.8	—	2	—	2	—	ns
t _{WS}	Write Setup Time	1.8	—	2	—	2	—	ns
t _{CES}	Chip Enable Setup Time	1.8	—	2	—	2	—	ns
t _{AVS}	Address Advance Setup Time	1.8	—	2	—	2	—	ns
t _{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{AVH}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	ns

Note:

1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.

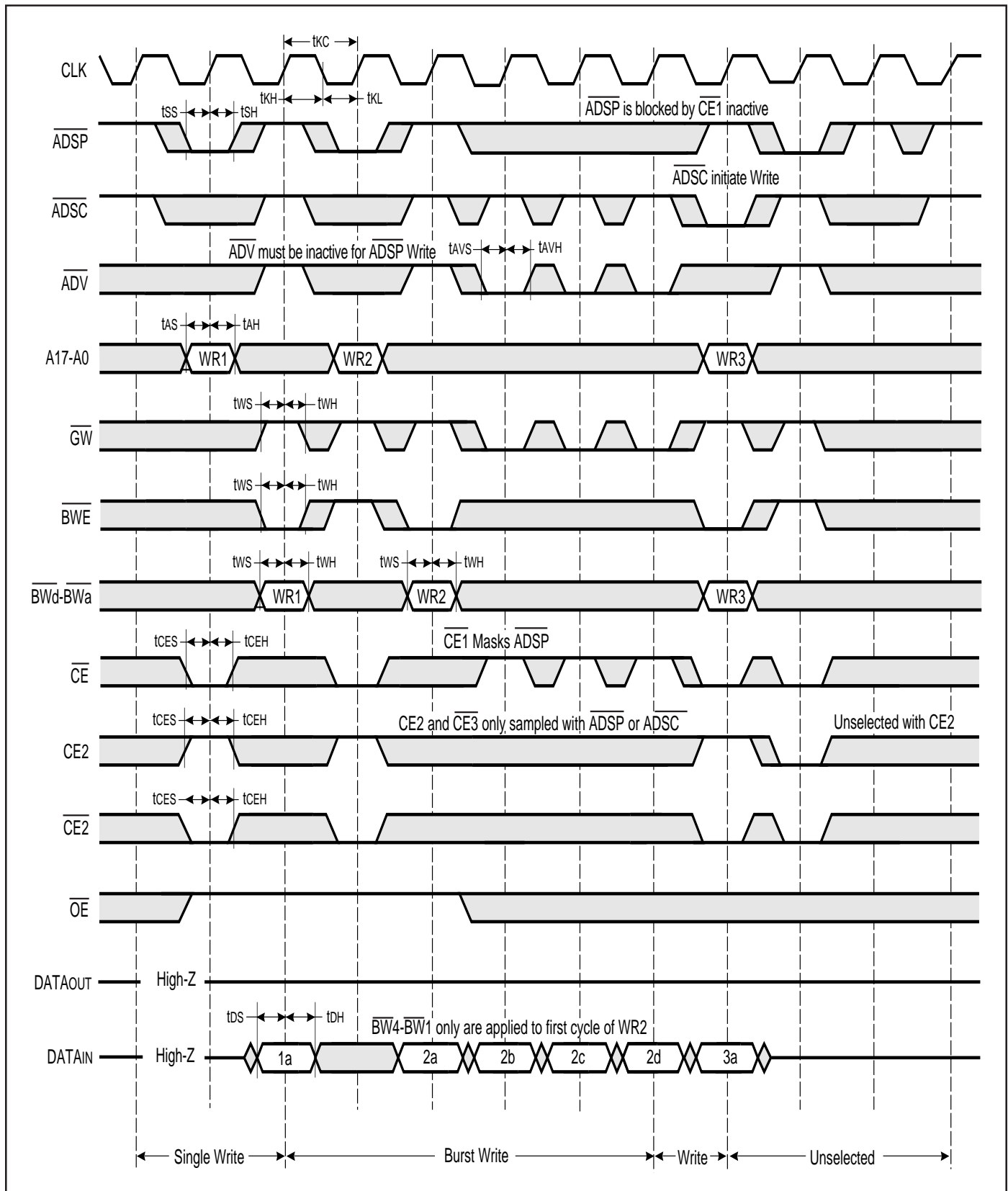
READ/WRITE CYCLE TIMING



WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-8.5		-9		-10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{KC}	Cycle Time	10	—	15	—	15	—	ns
t _{KH}	Clock High Pulse Width	3.0	—	4.0	—	4.0	—	ns
t _{KL}	Clock Low Pulse Width	3.0	—	4.0	—	4.0	—	ns
t _{AS}	Address Setup Time	1.8	—	2	—	2	—	ns
t _{SS}	Address Status Setup Time	1.8	—	2	—	2	—	ns
t _{WS}	Write Setup Time	1.8	—	2	—	2	—	ns
t _{DS}	Data In Setup Time	1.8	—	2	—	2	—	ns
t _{CES}	Chip Enable Setup Time	1.8	—	2	—	2	—	ns
t _{AVS}	Address Advance Setup Time	1.8	—	2	—	2	—	ns
t _{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{DH}	Data In Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{AVH}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	ns

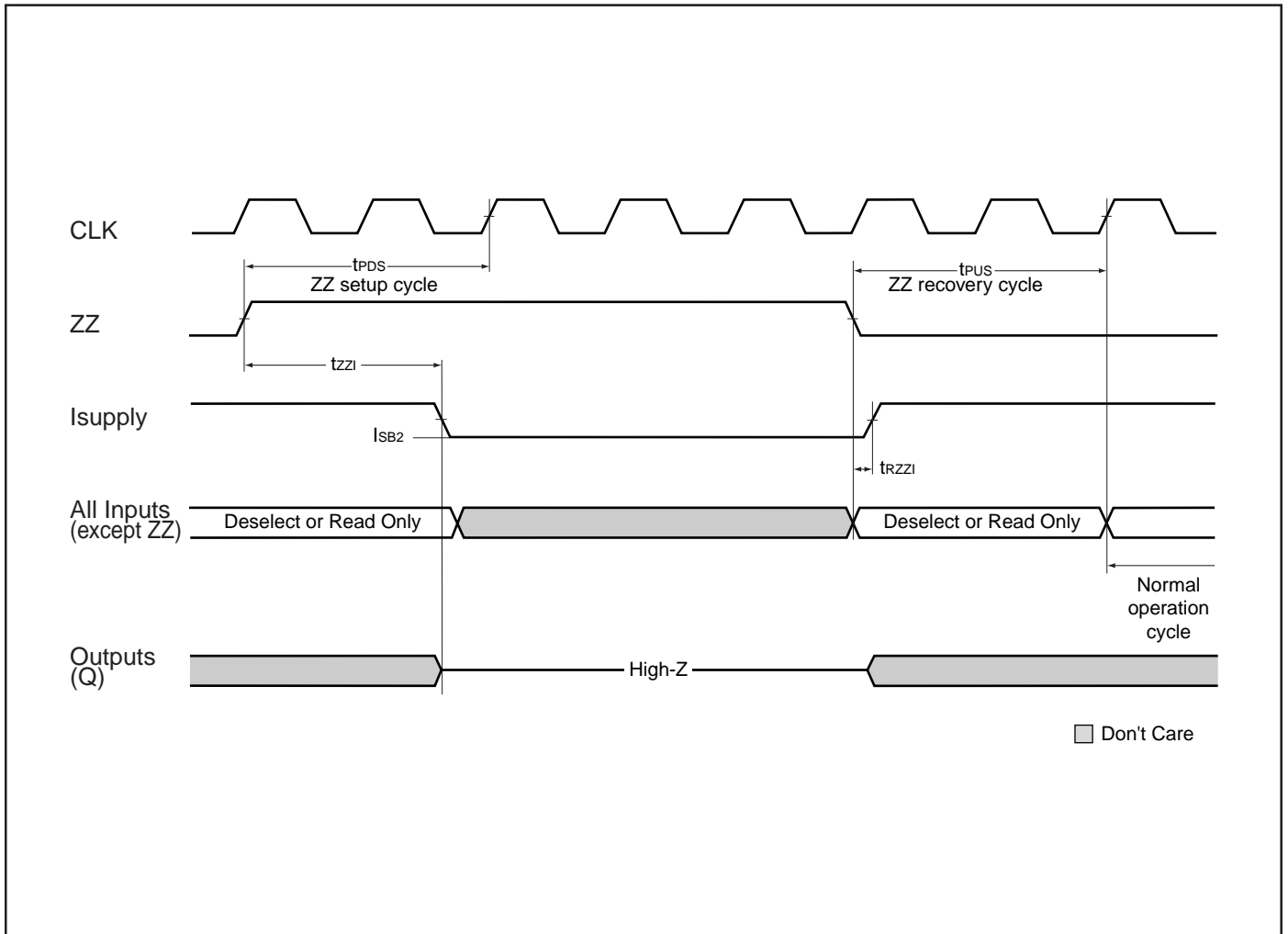
WRITE CYCLE TIMING



SLEEP MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
ISB2	Current during SLEEP MODE	ZZ ≥ Vih	—	15	mA
tpDS	ZZ active to input ignored		2	—	cycle
tpUS	ZZ inactive to input sampled		2	—	cycle
tzZI	ZZ active to SLEEP current		2	—	cycle
trZZI	ZZ inactive to exit SLEEP current		0	—	ns

SLEEP MODE TIMING



IS61SF25632T/D IS61LF25632T/D
 IS61SF25636T/D IS61LF25636T/D
 IS61SF51218T/D IS61LF51218T/D



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
9 ns	IS61SF25632T-9TQ	TQFP
	IS61SF25632D-9TQ	TQFP
	IS61SF25632D-9B	PBGA
10 ns	IS61SF25632T-10TQ	TQFP
	IS61SF25632D-10TQ	TQFP
	IS61SF25632D-10B	PBGA

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
9 ns	IS61SF25636T-9TQ	TQFP
	IS61SF25636D-9TQ	TQFP
	IS61SF25636D-9B	PBGA
10 ns	IS61SF25636T-10TQ	TQFP
	IS61SF25636D-10TQ	TQFP
	IS61SF25636D-10B	PBGA

Industrial Range: -40°C to +85°C

Speed	Order Part Number	Package
9 ns	IS61SF25632T-9TQI	TQFP
	IS61SF25632D-9TQI	TQFP
10 ns	IS61SF25632T-10TQI	TQFP
	IS61SF25632D-10TQI	TQFP

Industrial Range: -40°C to +85°C

Speed	Order Part Number	Package
9 ns	IS61SF25636T-9TQI	TQFP
	IS61SF25636D-9TQI	TQFP
10 ns	IS61SF25636T-10TQI	TQFP
	IS61SF25636D-10TQI	TQFP

IS61SF25632T/D IS61LF25632T/D
IS61SF25636T/D IS61LF25636T/D
IS61SF51218T/D IS61LF51218T/D



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
8.5 ns	IS61SF51218T-8.5TQ	TQFP
	IS61SF51218D-8.5TQ	TQFP
	IS61SF51218D-8.5B	PBGA
9 ns	IS61SF51218T-9TQ	TQFP
	IS61SF51218D-9TQ	TQFP
	IS61SF51218D-9B	PBGA
10 ns	IS61SF51218T-10TQ	TQFP
	IS61SF51218D-10TQ	TQFP
	IS61SF51218D-10B	PBGA

Industrial Range: -40°C to +85°C

Speed	Order Part Number	Package
9 ns	IS61SF51218T-9TQI	TQFP
	IS61SF51218D-9TQI	TQFP
10 ns	IS61SF51218T-10TQI	TQFP
	IS61SF51218D-10TQI	TQFP

IS61SF25632T/D IS61LF25632T/D
 IS61SF25636T/D IS61LF25636T/D
 IS61SF51218T/D IS61LF51218T/D



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
9 ns	IS61LF25632T-9TQ	TQFP
	IS61LF25632D-9TQ	TQFP
	IS61LF25632D-9B	PBGA
10 ns	IS61LF25632T-10TQ	TQFP
	IS61LF25632D-10TQ	TQFP
	IS61LF25632D-10B	PBGA

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
9 ns	IS61LF25636T-9TQ	TQFP
	IS61LF25636D-9TQ	TQFP
	IS61LF25636D-9B	PBGA
10 ns	IS61LF25636T-10TQ	TQFP
	IS61LF25636D-10TQ	TQFP
	IS61LF25636D-10B	PBGA

Industrial Range: -40°C to +85°C

Speed	Order Part Number	Package
9 ns	IS61LF25632T-9TQI	TQFP
	IS61LF25632D-9TQI	TQFP
10 ns	IS61LF25632T-10TQI	TQFP
	IS61LF25632D-10TQI	TQFP

Industrial Range: -40°C to +85°C

Speed	Order Part Number	Package
9 ns	IS61LF25636T-9TQI	TQFP
	IS61LF25636D-9TQI	TQFP
10 ns	IS61LF25636T-10TQI	TQFP
	IS61LF25636D-10TQI	TQFP

IS61SF25632T/D IS61LF25632T/D
IS61SF25636T/D IS61LF25636T/D
IS61SF51218T/D IS61LF51218T/D



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
9 ns	IS61LF51218T-9TQ	TQFP
	IS61LF51218D-9TQ	TQFP
	IS61LF51218D-9B	PBGA
10 ns	IS61LF51218T-10TQ	TQFP
	IS61LF51218D-10TQ	TQFP
	IS61LF51218D-10B	PBGA

Industrial Range: -40°C to +85°C

Speed	Order Part Number	Package
9 ns	IS61LF51218T-9TQI	TQFP
	IS61LF51218D-9TQI	TQFP
10 ns	IS61LF51218T-10TQI	TQFP
	IS61LF51218D-10TQI	TQFP



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