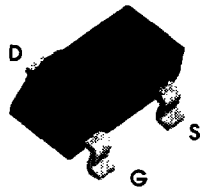# NDS336P
P-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

These P-Channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management, portable electronics, and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- -1.2 A, -20V. $R_{DS(ON)} = 0.27\Omega$ @ $V_{GS}=-2.7V$
  $R_{DS(ON)} = 0.20\Omega$ @ $V_{GS}=-4.5V$.

- Industry standard outline SOT-23 surface mount package using poprietary SuperSOT™-3 design for superior thermal and electrical capabilities.

- High density cell design for extremely low $R_{DS(ON)}$.

- Exceptional on-resistance and maximum DC current capability.

SuperSOT™-3 (SOT-23)
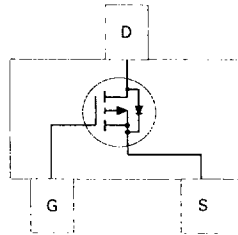
Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS336P	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage - Continuous		-8	V
I_D	Maximum Drain Current - Continuous (Note 1a)		-1.2	A
	- Pulsed		-10	
P_D	Maximum Power Dissipation (Note 1a)		0.5	W
	(Note 1b)		0.46	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
			300	
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)		250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)		75	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = -250$ µA		-20			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16$ V, $V_{GS} = 0$ V				-1	µA
			$T_J = 55$°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 8$ V, $V_{DS} = 0$ V				100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -8$ V, $V_{DS} = 0$ V				-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -250$ µA		-0.5	-0.78	-1	V
			$T_J = 125$°C	-0.3	-0.58	-0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = -2.7$ V, $I_D = -1.2$ A			0.22	0.27	Ω
			$T_J = 125$°C		0.34	0.49	
		$V_{GS} = -4.5$ V, $I_D = -1.3$ A			0.16	0.2	
$I_{D(ON)}$	On-State Drain Current	$V_{GS} = -2.7$ V, $V_{DS} = -5$ V		-2			A
g_{FS}	Forward Transconductance	$V_{DS} = -5$ V, $I_D = -1.2$ A			3		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	$V_{DS} = -10$ V, $V_{GS} = 0$ V, f = 1.0 MHz			360		pF
C_{oss}	Output Capacitance				170		pF
C_{rss}	Reverse Transfer Capacitance				60		pF
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = -5$ V, $I_D = -1$ A, $V_{GS} = -4.5$ V, $R_{GEN} = 6$ Ω			8	15	ns
t_r	Turn - On Rise Time				29	50	ns
$t_{D(off)}$	Turn - Off Delay Time				33	60	ns
t_f	Turn - Off Fall Time				23	45	ns
Q_g	Total Gate Charge	$V_{DS} = -10$ V, $I_D = -1.2$ A, $V_{GS} = -4.5$ V			5.7	8.5	nC
Q_{gs}	Gate-Source Charge				0.7		nC
Q_{gd}	Gate-Drain Charge				1.8		nC

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Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Source Current				-0.42	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				-10	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.42 (Note 2)		-0.65	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

   a. 250°C/W when mounted on a 0.02 in² pad of 2oz copper.

   b. 270°C/W when mounted on a 0.001 in² pad of 2oz copper.
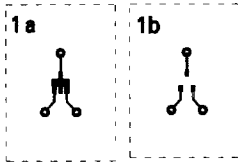
Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics
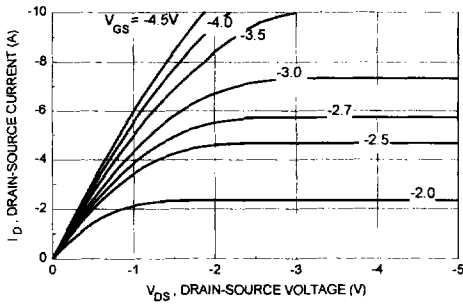
Figure 1. On-Region Characteristics
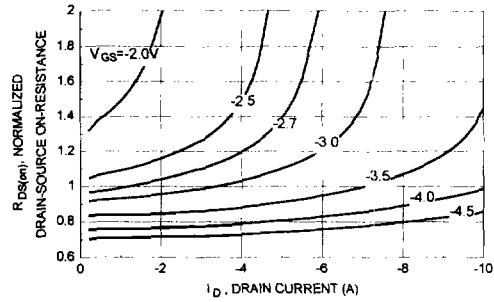
Figure 2. On-Resistance Variation
with Drain Current and Gate Voltage
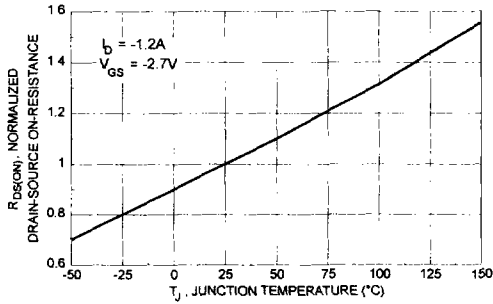
Figure 3. On-Resistance Variation
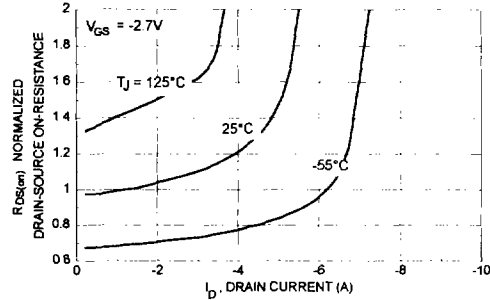with Temperature

Figure 4. On-Resistance Variation
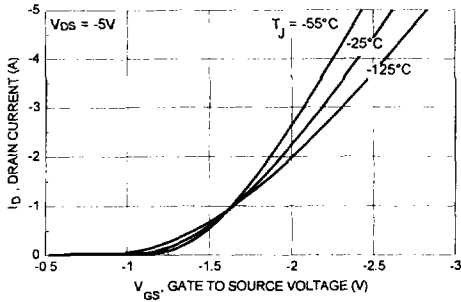with Drain Current and Temperature
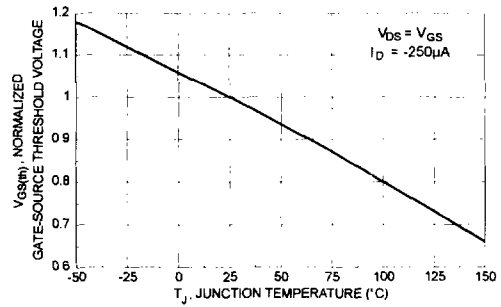

Figure 5. Transfer Characteristics

Figure 6. Gate Threshold Variation
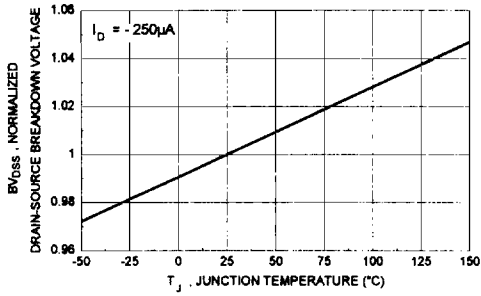with Temperature

Typical Electrical Characteristics (continued)
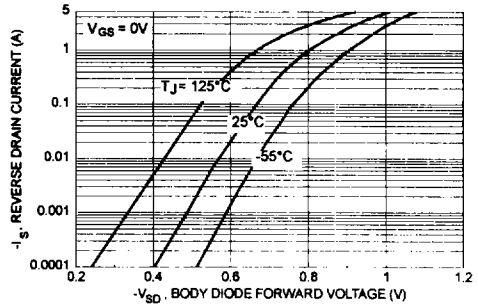

Figure 7. Breakdown Voltage Variation
with Temperature

Figure 8. Body Diode Forward Voltage
Variation with Source Current
and Temperature
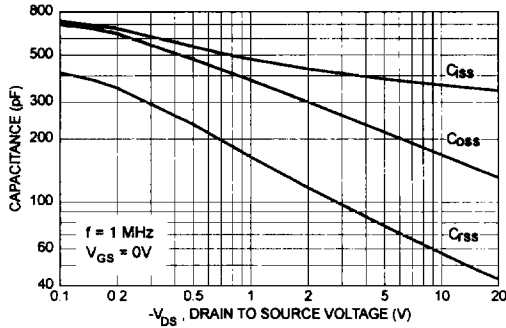
Figure 9. Capacitance Characteristics
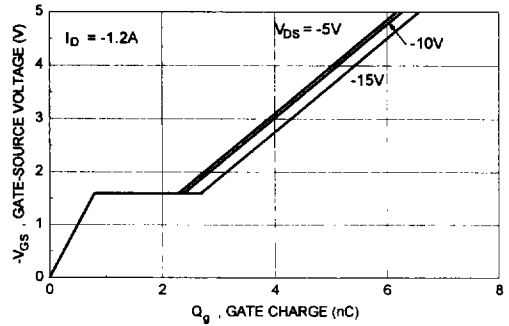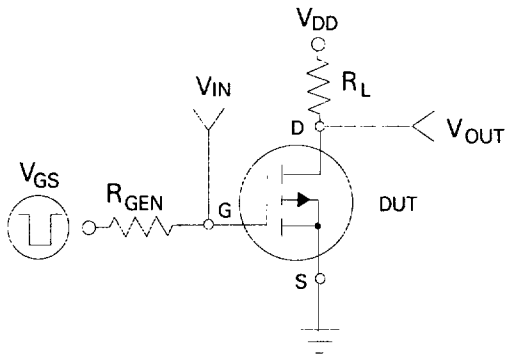

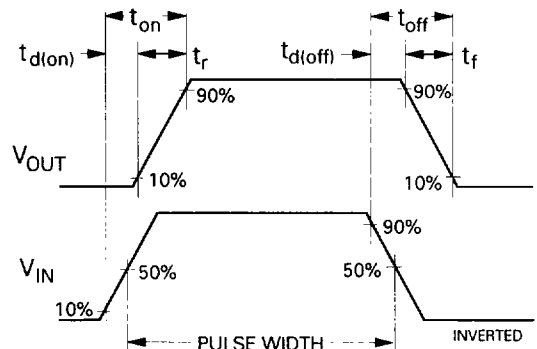Figure 10. Gate Charge Characteristics

Figure 11. Switching Test Circuit

Figure 12. Switching Waveforms
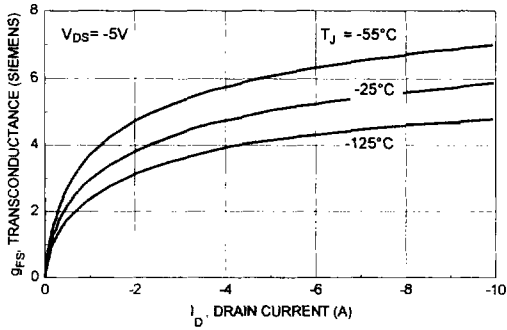
Typical Electrical Characteristics (continued)

Figure 13. Transconductance Variation with Drain Current and Temperature
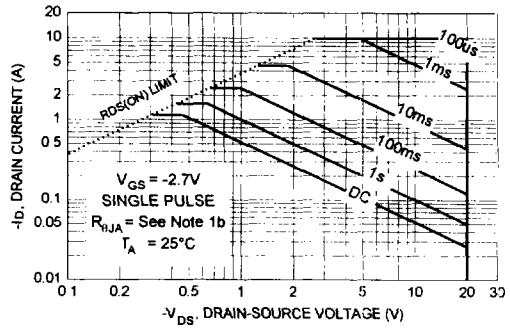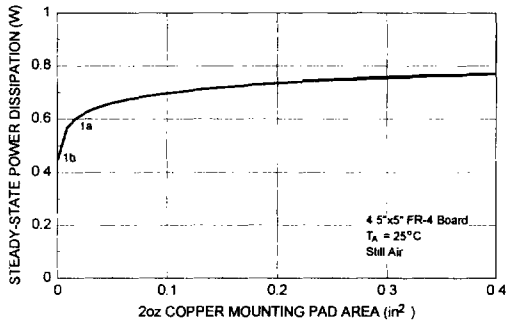

Figure 14. Maximum Safe Operating Area

Figure 15. SuperSOT™-3 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.
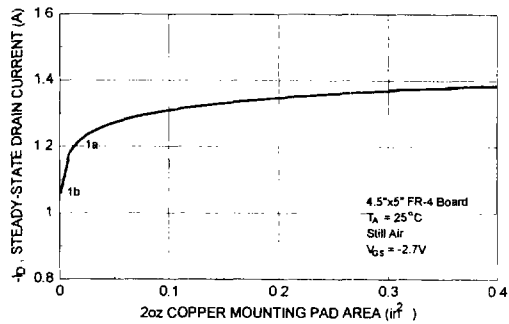

Figure 16. Maximum Steady-State Drain Current versus Copper Mounting Pad Area
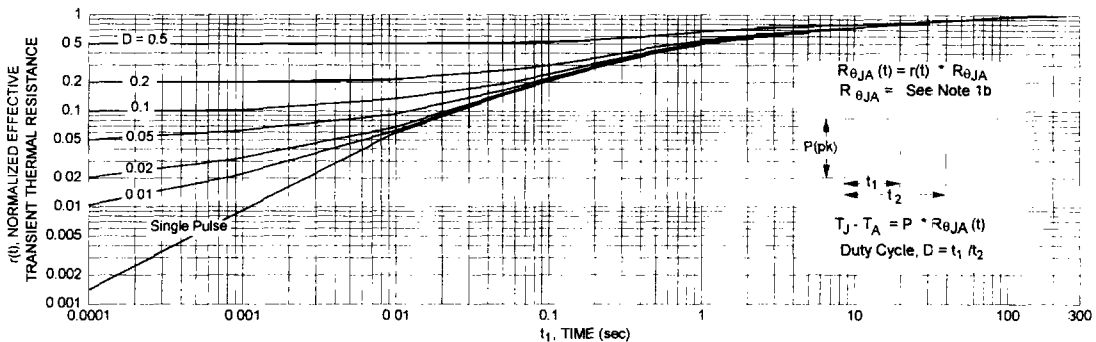
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Figure 17. Transient Thermal Response Curve

Note : Characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.