Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (16K x 4-BIT)

IDT6198S
IDT6198L

FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- Output Enable ($\overline{OE}$) pin available for added system flexibility
- High-speed (equal access and cycle times)
  - — Military: 20/25/35/45/55/70/85ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low-power consumption
  - — IDT6198S
    Active: 350mW (typ.)
    Standby 100µW (typ.)
  - — IDT6198L
    Active: 300mW (typ.)
    Standby: 30µW (typ.)
- JEDEC compatible pinout
- Battery back-up operation—2V data retention (L version only)
- 24-pin CERDIP, 24-pin plastic DIP, high-density 28-pin leadless chip carrier and 24-pin SOIC (gull-wing and J-bend)
- Produced with advanced CEMOS™ technology
- Bidirectional data inputs and outputs
- Military product compliant to MIL-STD-883, Class B

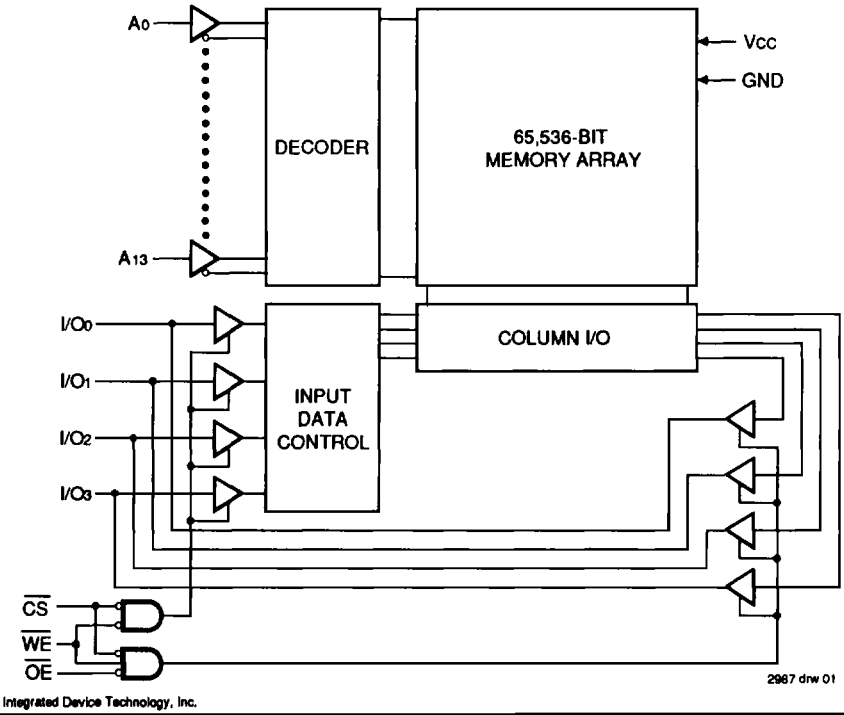
DESCRIPTION:

The IDT6198 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for memory intensive applications. Timing parameters have been specified to meet the speed demands of the IDT79R3000 RISC processors.

The IDT6198 features two memory control functions: chip select ($\overline{CS}$) and output enable ($\overline{OE}$). These two functions greatly enhance the IDT6198's overall flexibility in high-speed memory applications.

Access times as fast as 15ns are available, with typical power consumption of only 300mW. The IDT6198 offers a reduced power standby mode, I_{SB1}, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and

FUNCTIONAL BLOCK DIAGRAM



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DESCRIPTION (Continued)

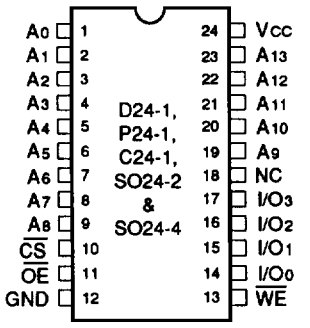
cooling levels, while greatly enhancing system reliability. The low-power version (L) also offers a battery backup data retention capability where the circuit typically consumes only 30µW when operating from a 2 volt battery.

All inputs and outputs are TTL-compatible and operate from a single 5 volt supply.

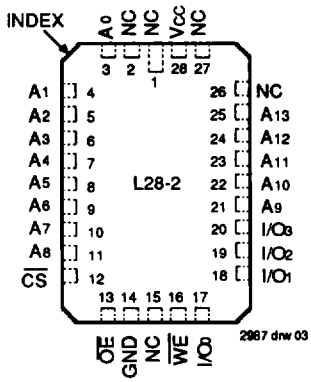
The IDT6198 is packaged in either a 24-pin 300 mil CERDIP or plastic DIP, 28-pin leadless chip carrier or 24-pin gull-wing or J-bend small outline IC.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A_0–A_{13}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_0–I/O_3	Data Input/Output
V_{CC}	Power
GND	Ground

2987 tbl 01

TRUTH TABLE[1]

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Standby	H	X	X	High Z	Standby
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active
Read	L	H	H	High Z	Active

NOTE: 2987 tbl 02
1. H = V_{IH}, L = V_{IL}, X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2987 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2987 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2987 tbl 05

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2987 tbl 06

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT6198S Min.	IDT6198S Max.	IDT6198L Min.	IDT6198L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2967 tbl 07

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6198S15 6198L15 Com'l.	6198S15 6198L15 Mil.	6198S20 6198L20 Com'l.	6198S20 6198L20 Mil.	6198S25 6198L25 Com'l.	6198S25 6198L25 Mil.	6198S35 6198L35 Com'l.	6198S35 6198L35 Mil.	6198S45 6198L45 Com'l.	6198S45 6198L45 Mil.	6198S55/70/85 6198L55/70/85 Com'l.	6198S55/70/85 6198L55/70/85 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0[2]	S	110	—	100	110	100	110	100	110	—	110	—	110	mA
		L	75	—	70	80	70	80	85	95	—	95	—	95	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	S	135	—	130	160	135	155	125	140	—	140	—	140	mA
		L	125	—	115	130	105	120	105	115	—	110	—	110	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}[2]	S	60	—	55	70	55	60	45	500	—	50	—	50	mA
		L	45	—	40	50	35	40	35	40	—	35	—	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC}=Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0[2]	S	20	—	15	25	15	20	15	20	—	20	—	20	mA
		L	1.5	—	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	—	1.5	

NOTES: 2987 tbl 08

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

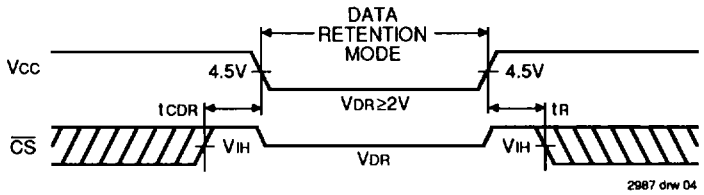
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1] Vcc @ 2.0v	Typ.[1] Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\|I_{LI}\|$[3]	Input Leakage Current			—	—	—	2	2	µA

2987 tbl 09

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2987 tbl 10

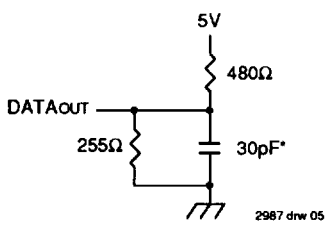


Figure 1. Output Load

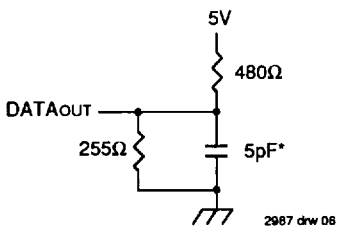


Figure 2. Output Load
(for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ} and t_{OW})

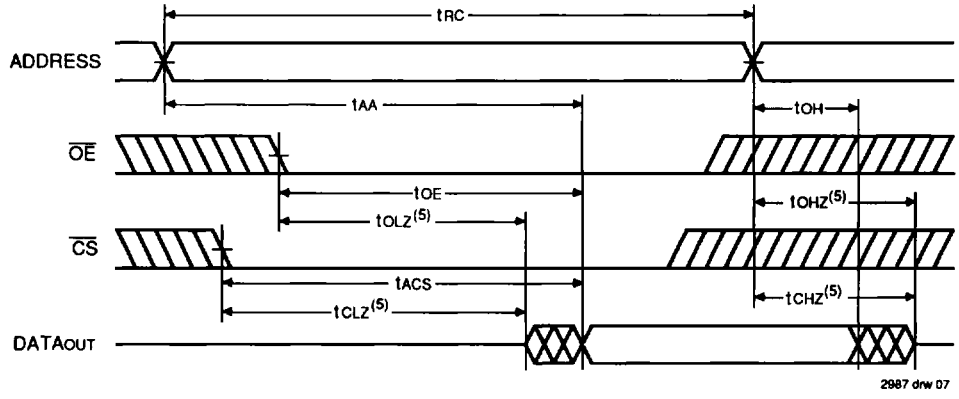
*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6198S15[1] 6198L15[1] Min.	Max.	6198S20 6198L20 Min.	Max.	6198S25 6198L25 Min.	Max.	6198S35 6198L35 Min.	Max.	6198S45/55[2] 6198L45/55[2] Min.	Max.	6198S70/85[2] 6198L70/85[2] Min.	Max.	Unit
Read Cycle														
tRC	Read Cycle Time	15	—	20	—	25	—	35	—	45/55	—	70/85	—	ns
tAA	Address Access Time	—	15	—	19	—	25	—	35	—	45/55	—	70/85	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	—	35	—	45/55	—	70/85	ns
tCLZ	Chip Select to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	8	—	9	—	11	—	18	—	25/35	—	45/55	ns
tOLZ	Output Enable to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tCHZ	Chip Select to Output in High Z[3]	2	7	2	8	2	10	2	14	—	15/20	—	25/30	ns
tOHZ	Output Disable to Output in High Z[3]	2	7	2	8	2	9	2	15	—	15/20	—	25/30	ns
tOH	Output Hold from Address Change	5	—	5	—	2	—	5	—	5	—	5	—	ns
tPU	Chip Select to Power Up Time[3]	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power Down Time[3]	—	15	—	20	—	25	—	35	—	45/55	—	70/85	ns

NOTES:
2987 tbl 11
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

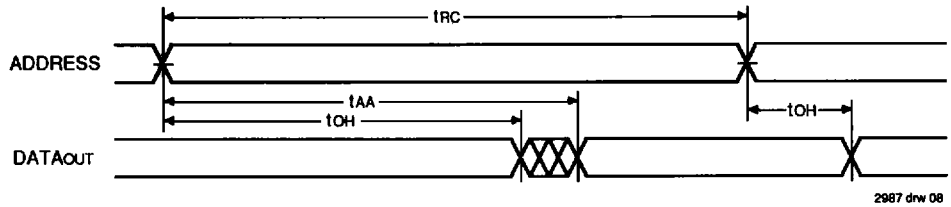
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



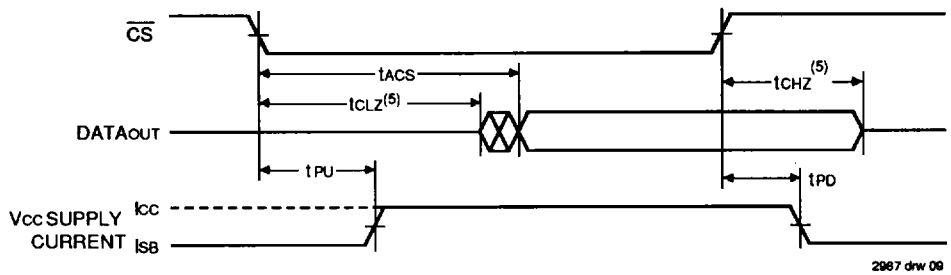
2987 drw 07

NOTES:
1. WE is high for Read cycle.
2. Device is continuously selected, CS = VIL.
3. Address valid prior to or coincident with CS transition low.
4. OE = VIL.
5. Transition is measured ±200mV from steady state voltage.

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



5

NOTES:
1. $\overline{WE}$ is high for Read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state voltage.

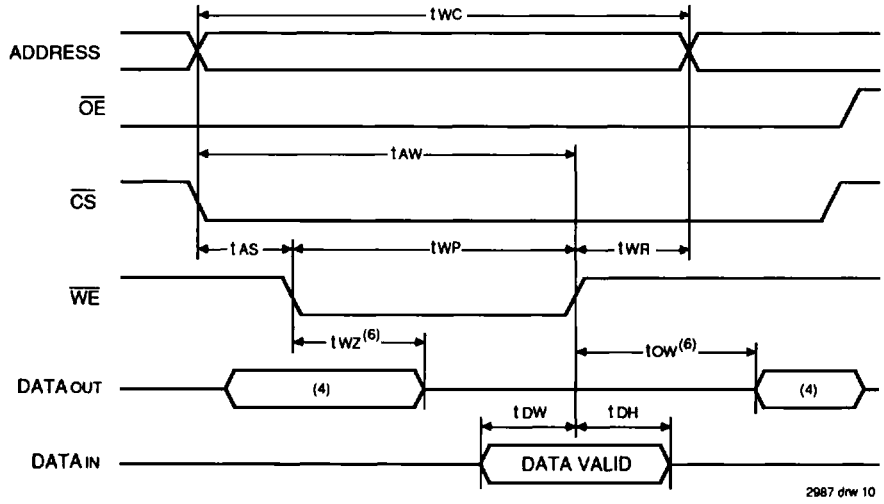
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6198S15[1] 6198L15[1] Min.	Max.	6198S20 6198L20 Min.	Max.	6198S25 6198L25 Min.	Max.	6198S35 6198L35 Min.	Max.	6198S45/55[2] 6198L45/55[2] Min.	Max.	6198S70/85[2] 6198L70/85[2] Min.	Max.	Unit
Write Cycle														
tWC	Write Cycle Time	14	—	17	—	20	—	30	—	40/50	—	60/75	—	ns
tCW	Chip Select to End of Write	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
tAW	Address Valid to End of Write	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High Z[3]	—	5	—	6	—	7	—	10	—	15/25	—	30/40	ns
tDW	Data Valid to End of Write	10	—	10	—	13	—	15	—	20/25	—	30/35	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End of Write[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns

2987 tbl 12

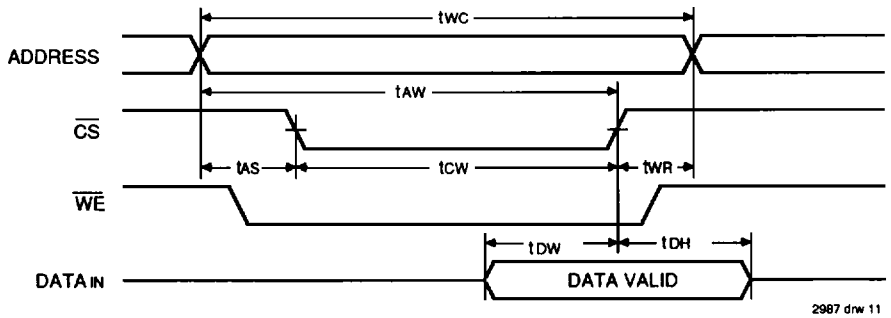
NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
8. $\overline{OE}$ = VIH.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5, 8)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
8. $\overline{OE}$ = VIH.

ORDERING INFORMATION