

Features

- **Medium-voltage and Standard-voltage Operation**
 - 5.0 ($V_{CC} = 4.5V$ to $5.5V$)
 - 2.7 ($V_{CC} = 2.7V$ to $5.5V$)
- **User-selectable Internal Organization**
 - 2K: 256 x 8 or 128 x 16
 - 4K: 512 x 8 or 256 x 16
- **Three-wire Serial Interface**
- **Sequential Read Operation**
- **2 MHz Clock Rate (5V)**
- **Self-timed Write Cycle (10 ms max)**
- **High Reliability**
 - **Endurance: 1 Million Write Cycles**
 - **Data Retention: 100 Years**
- **8-lead PDIP and 8-lead JEDEC SOIC Packages**

Description

The AT93C56A/66A provides 2048/4096 bits of serial electrically erasable programmable read-only memory (EEPROM). The EEPROM is organized as 128/256 words of 16 bits each (when the ORG pin is connected to VCC) and 256/512 words of 8 bits each (when the ORG pin is tied to ground.) The device is optimized for use in many automotive applications where low-power and low-voltage operations are essential. The AT93C56A/66A is available in space-saving 8-lead PDIP and 8-lead JEDEC SOIC packages.

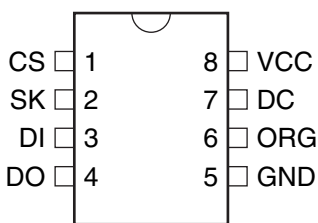
The AT93C56A/66A is enabled through the Chip Select (CS) pin and accessed via a three-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The write cycle is completely self-timed, and no separate erase cycle is required before write. The write cycle is only enabled when the part is in the Erase/Write Enable state. When CS is brought high following the initiation of a write cycle, the DO pin outputs the Ready/Busy status of the part.

The AT93C56A/66A is available in 4.5V to 5.5V and 2.7V to 5.5V versions.

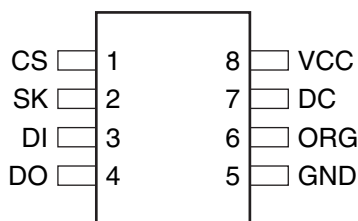
Table 1. Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
VCC	Power Supply
ORG	Internal Organization
DC	Don't Connect

8-lead PDIP



8-lead SOIC



Three-wire Serial Automotive EEPROMs

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

AT93C56A

AT93C66A

Preliminary

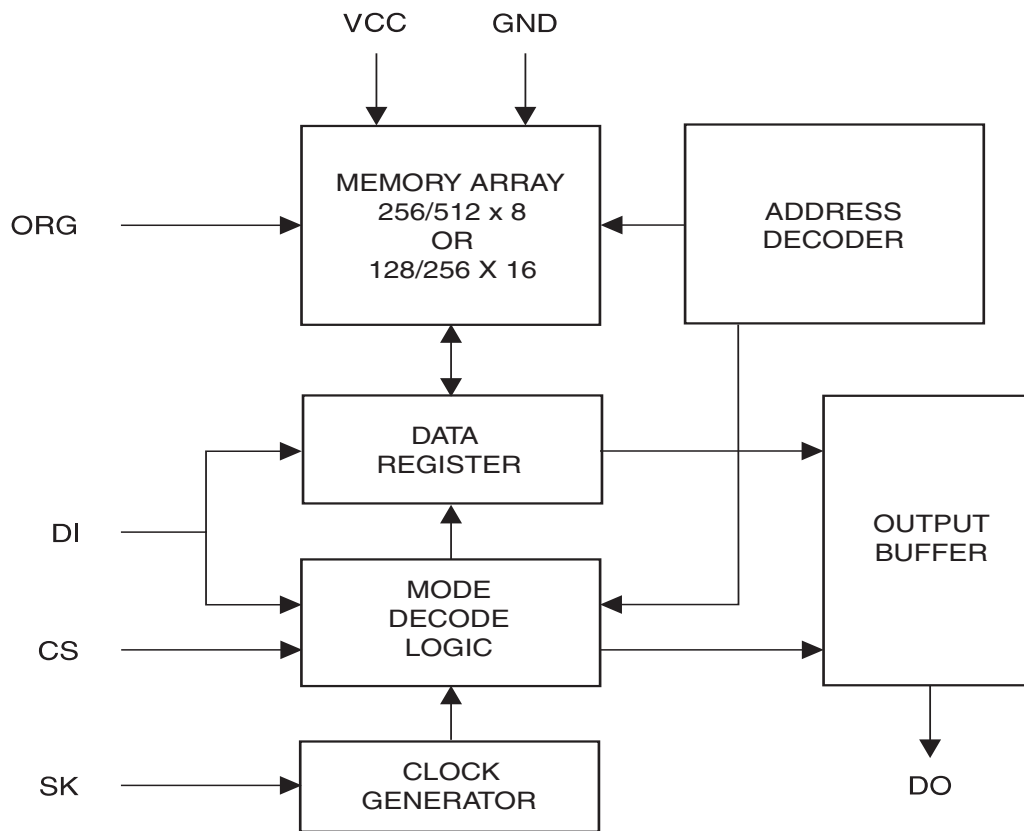


Absolute Maximum Ratings*

Operating Temperature.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground.....	-1.0V to +7.0V
Maximum Operating Voltage.....	6.25V
DC Output Current.....	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Figure 1. Block Diagram



Note: When the ORG pin is connected to VCC, the “x 16” organization is selected. When it is connected to ground, the “x 8” organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1 Meg ohm pullup, then the “x 16” organization is selected.

Table 1. Pin Capacitance⁽¹⁾

Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$, $V_{CC} = +5.0\text{V}$ (unless otherwise noted)

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	$V_{OUT} = 0\text{V}$
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

Table 2. DC Characteristics

Applicable over recommended operating range from: $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = +2.7\text{V}$ to $+5.5\text{V}$ (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC1}	Supply Voltage		2.7		5.5	V
V_{CC2}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current	$V_{CC} = 5.0\text{V}$	READ at 1.0 MHz	0.5	2.0	mA
			WRITE at 1.0 MHz	0.5	2.0	mA
I_{SB1}	Standby Current	$V_{CC} = 2.7\text{V}$	CS = 0V	6.0	10.0	μA
I_{SB2}	Standby Current	$V_{CC} = 5.0\text{V}$	CS = 0V	17	30	μA
I_{IL}	Input Leakage	$V_{IN} = 0\text{V}$ to V_{CC}		0.1	3.0	μA
I_{OL}	Output Leakage	$V_{IN} = 0\text{V}$ to V_{CC}		0.1	3.0	μA
$V_{IL1}^{(1)}$ $V_{IH1}^{(1)}$	Input Low Voltage Input High Voltage	$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$		-0.6 2.0	0.8 $V_{CC} + 1$	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	$I_{OL} = 2.1\text{ mA}$		0.4	V
			$I_{OH} = -0.4\text{ mA}$	2.4		V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 3. AC Characteristics

Applicable over recommended operating range from $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = \text{As Specified}$, $C_L = 1 \text{ TTL Gate and } 100 \text{ pF}$ (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	0 0		2 1	MHz
t_{SKH}	SK High Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	250 250			ns
t_{SKL}	SK Low Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	250 250			ns
t_{CS}	Minimum CS Low Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	250 250			ns
t_{CSS}	CS Setup Time	Relative to SK $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	50 50			ns
t_{DIS}	DI Setup Time	Relative to SK $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	100 100			ns
t_{CSH}	CS Hold Time	Relative to SK	0			ns
t_{DIH}	DI Hold Time	Relative to SK $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	100 100			ns
t_{PD1}	Output Delay to '1'	AC Test $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$			250 500	ns
t_{PDO}	Output Delay to '0'	AC Test $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$			250 500	ns
t_{SV}	CS to Status Valid	AC Test $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$			250 250	ns
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL} $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$			100 150	ns
t_{WP}	Write Cycle Time	$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	0.1	3	10	ms
Endurance ⁽¹⁾	5.0V, 25°C		1M			Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

Table 4. Instruction Set for the AT93C56A and AT93C66A

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	$A_8 - A_0$	$A_7 - A_0$			Reads data stored in memory, at specified address
EWEN	1	00	11XXXXXXXX	11XXXXXXXX			Write enable must precede all programming modes
ERASE	1	11	$A_8 - A_0$	$A_7 - A_0$			Erases memory location $A_n - A_0$
WRITE	1	01	$A_8 - A_0$	$A_7 - A_0$	$D_7 - D_0$	$D_{15} - D_0$	Writes memory location $A_n - A_0$
ERAL	1	00	10XXXXXXXX	10XXXXXXXX			Erases all memory locations. Valid only at $V_{CC} = 4.5V$ to $5.5V$.
WRAL	1	00	01XXXXXXXX	01XXXXXXXX	$D_7 - D_0$	$D_{15} - D_0$	Writes all memory locations. Valid only at $V_{CC} = 5.0V \pm 10\%$ and Disable Register cleared.
EWDS	1	00	00XXXXXXXX	00XXXXXXXX			Disables all programming instructions.

Note: The Xs in the address field represent *don't care* values and must be clocked.

Functional Description

The AT93C56A/66A is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A *valid instruction starts with a rising edge of CS* and consists of a Start Bit (logic “1”) followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic “0”) precedes the 8- or 16-bit data output string. The AT93C56A/66A supports sequential read operations. The device will automatically increment the internal address pointer and clock out the next memory location as long as Chip Select (CS) is held high. In this case, the dummy bit (logic “0”) will not be clocked out between memory locations, thus allowing for a continuous stream of data to be read.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

ERASE (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical “1” state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic “1” at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP} , starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic “0” at DO indicates that programming is still in progress. A logic “1” indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. *A Ready/Busy status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, t_{WP} .*

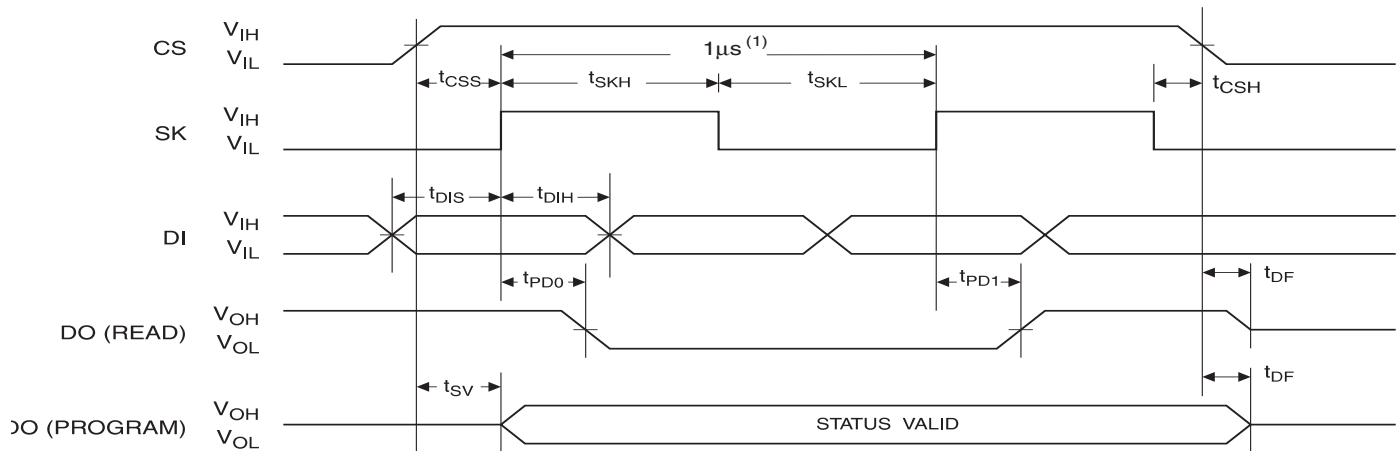
ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic “1” state and is primarily used for testing purposes. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at $V_{CC} = 5.0V \pm 10\%$.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at $V_{CC} = 5.0V \pm 10\%$.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Timing Diagrams

Figure 2. Synchronous Data Timing



Note: This is the minimum SK period.

Table 5. Organization Key for Timing Diagrams

I/O	AT93C56A (2K)		AT93C66A (4K)	
	x 8	x 16	x 8	x 16
A_N	$A_8^{(1)}$	$A_7^{(2)}$	A_8	A_7
D_N	D_7	D_{15}	D_7	D_{15}

Notes: 1. A_8 is a *don't care* value, but the extra clock is required.
2. A_7 is a *don't care* value, but the extra clock is required.

Figure 3. READ Timing

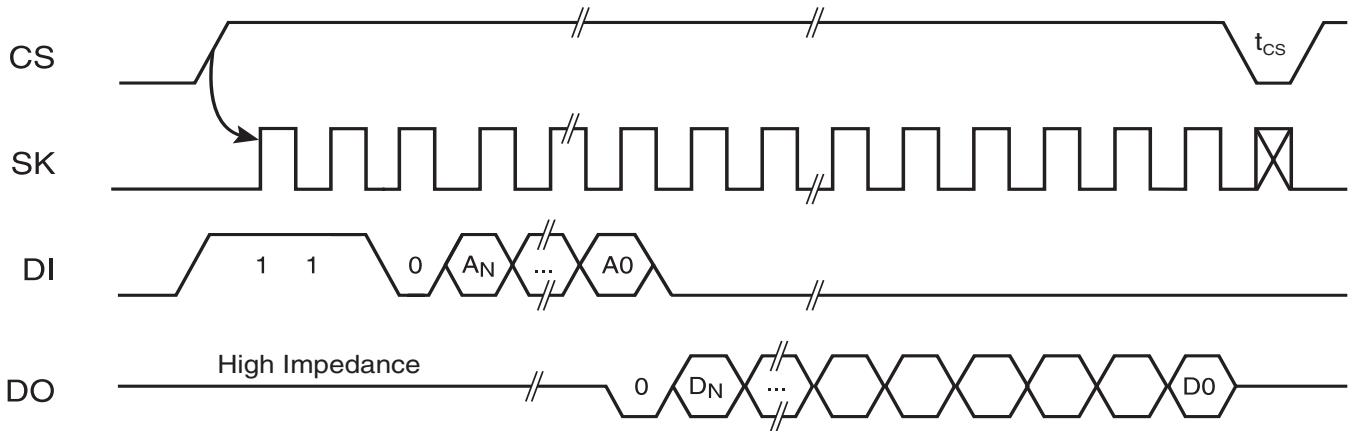


Figure 4. EWEN Timing

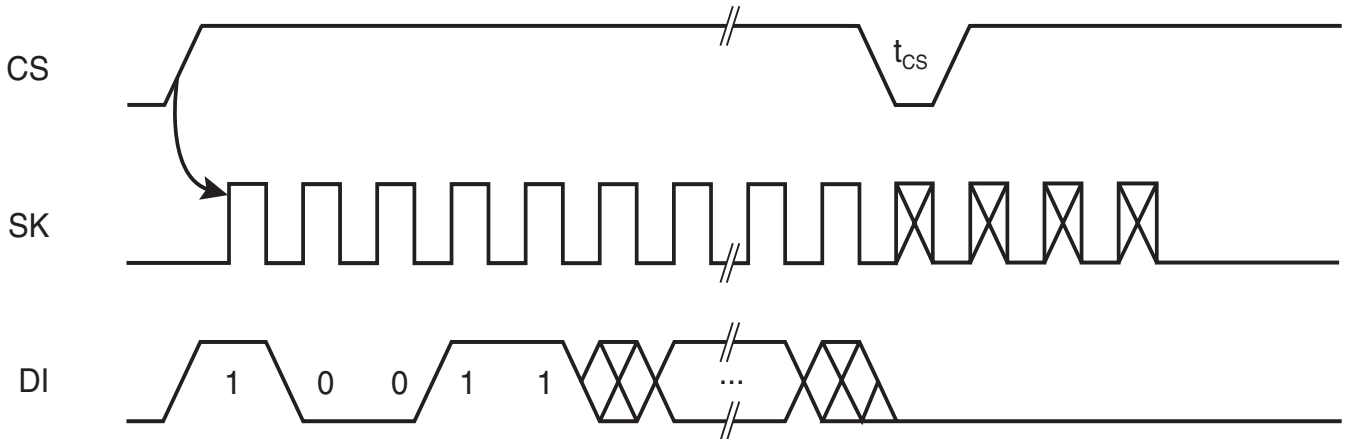


Figure 5. EWDS Timing

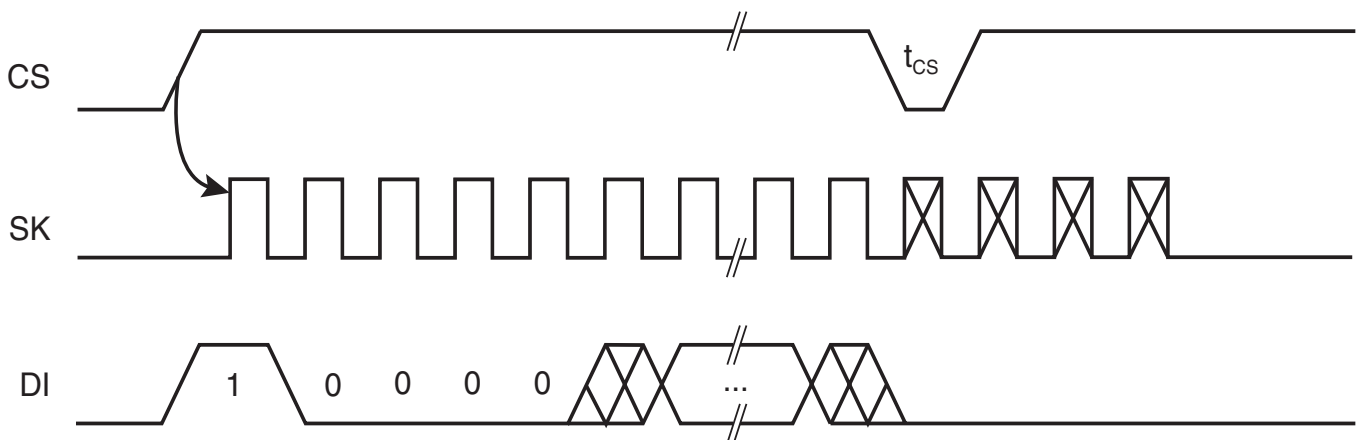


Figure 6. WRITE Timing

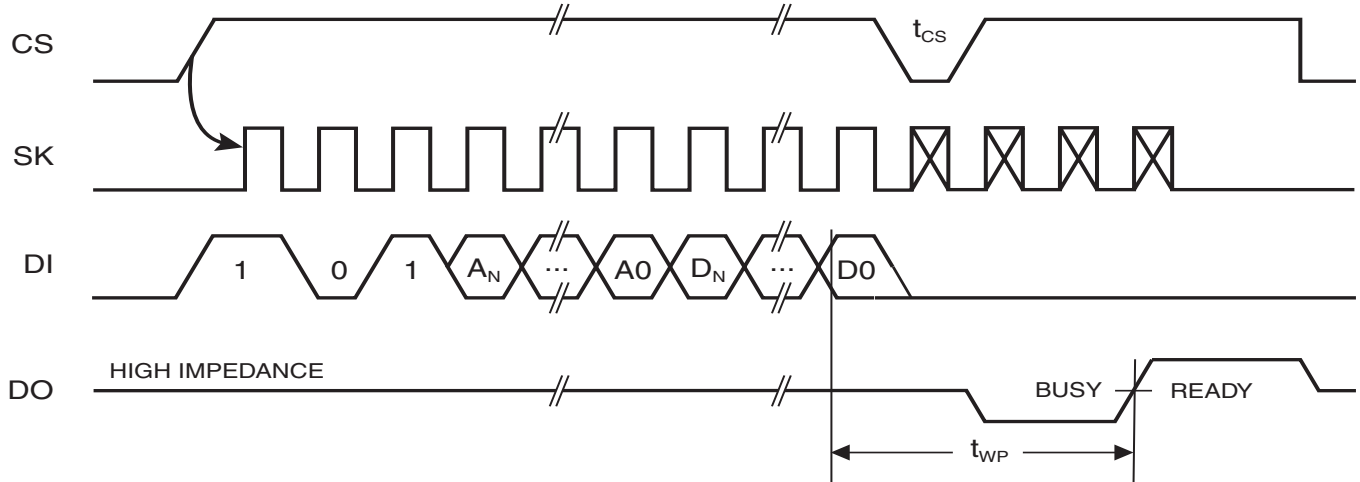
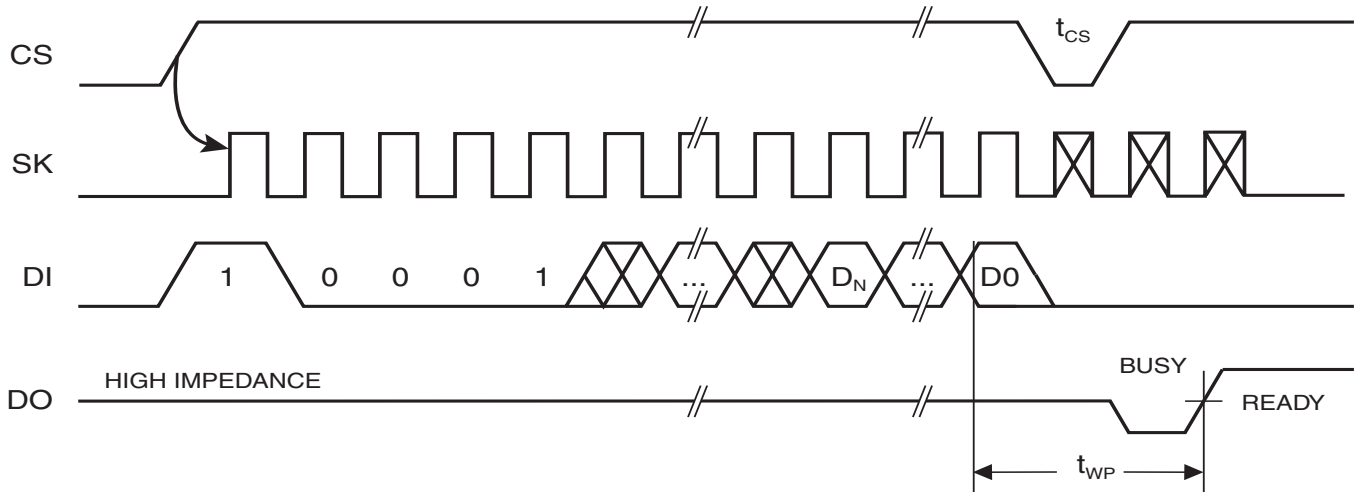


Figure 7. WRAL Timing



Note: 1. Valid only at $V_{CC} = 4.5V$ to $5.5V$.

Figure 8. ERASE Timing

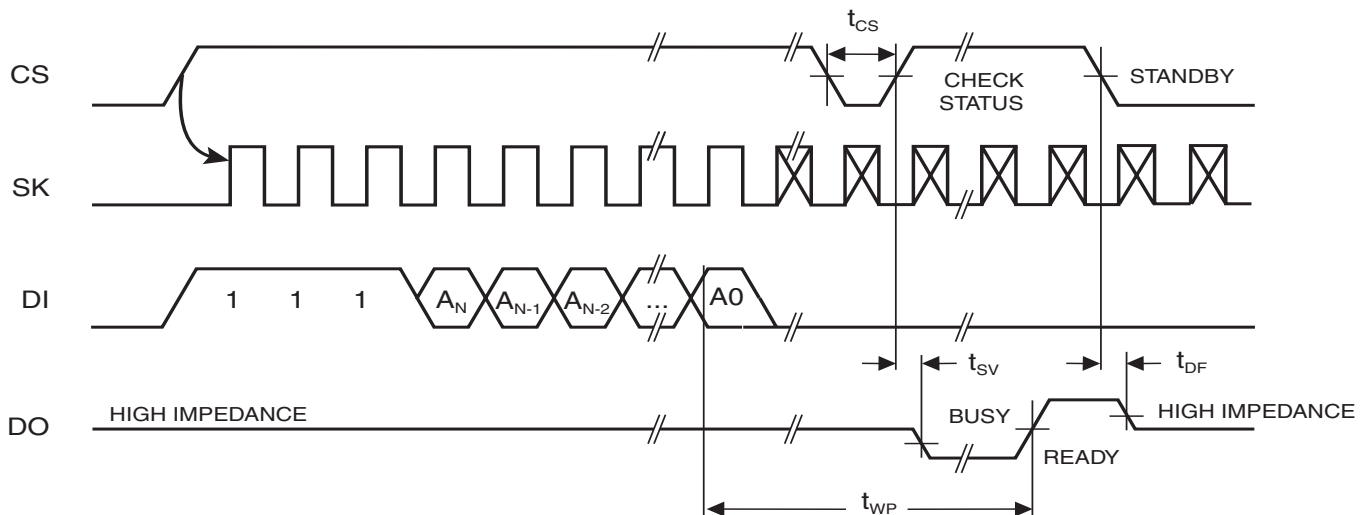
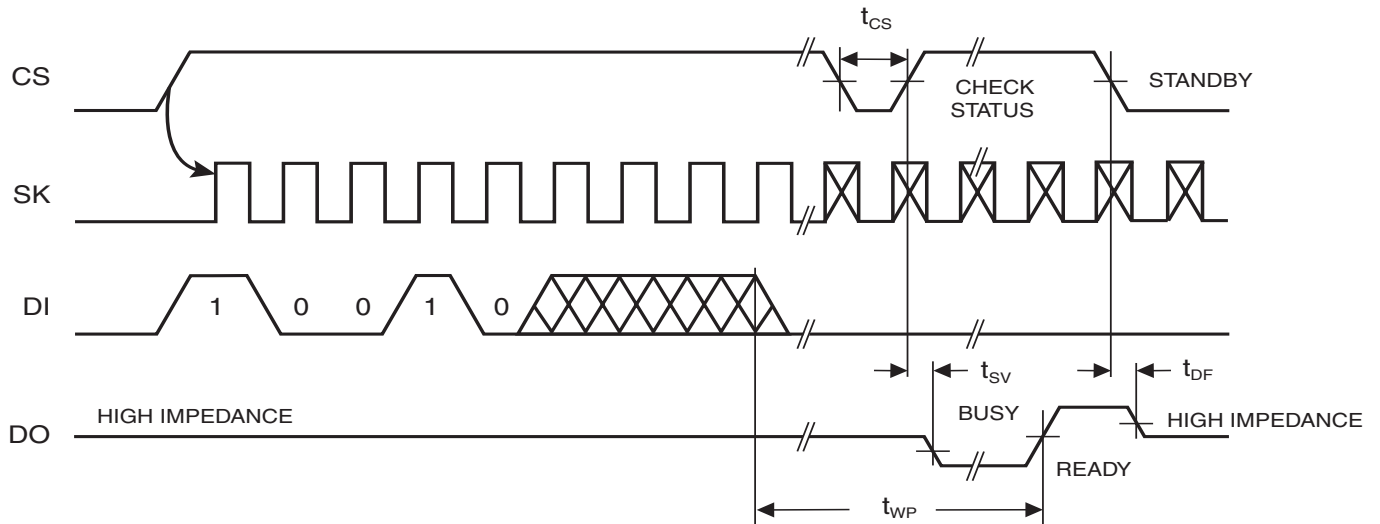


Figure 9. ERAL Timing



Note: Valid only at $V_{CC} = 4.5V$ to $5.5V$.



AT93C56A Ordering Information

Ordering Code	Package	Operation Range
AT93C56A-10PA-5.0C	8P3	Automotive
AT93C56A-10SA-5.0C	8S1	(-40°C to 125°C)
AT93C56A-10PA-2.7C	8P3	Automotive
AT93C56A-10SA-2.7C	8S1	(-40°C to 125°C)

Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
-5.0	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)

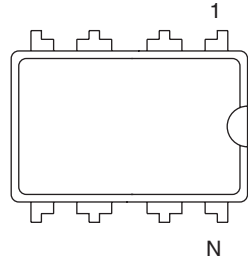
AT93C66A Ordering Information

Ordering Code	Package	Operation Range
AT93C66A-10PA-5.0C	8P3	Automotive
AT93C66A-10SA-5.0C	8S1	(-40°C to 125°C)
AT93C66A-10PA-2.7C	8P3	Automotive
AT93C66A-10SA-2.7C	8S1	(-40°C to 125°C)

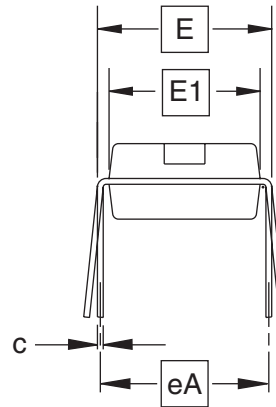
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8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
-5.0	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)

Packaging Information

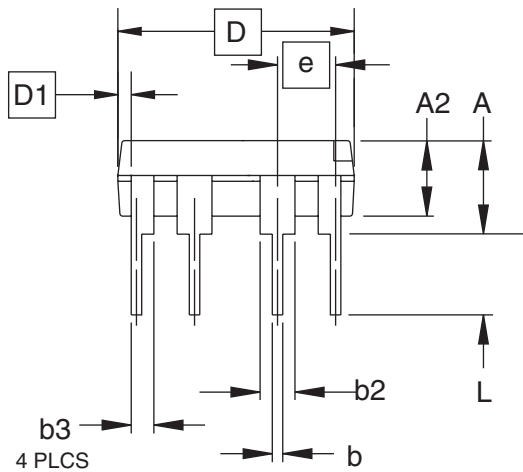
8P3 – PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005	–	–	3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

- Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA, for additional information.
 2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
 3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
 4. E and eA measured with the leads constrained to be perpendicular to datum.
 5. Pointed or rounded lead tips are preferred to ease insertion.
 6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

01/09/02



2325 Orchard Parkway
San Jose, CA 95131

TITLE

**8P3, 8-lead, 0.300" Wide Body, Plastic Dual
In-line Package (PDIP)**

DRAWING NO.

8P3

REV.

B



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