

August 1996

## Fast CMOS Octal Bidirectional Transceivers

### Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible With Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption
- 25Ω Series Resistor on All Outputs (CD74FCT2245T, CD74FCT2645T Only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs

### Description

These devices are 8-bit wide octal buffer bidirectional transceivers designed for asynchronous two-way communication between data buses. The transmit/receive ( $T/\bar{R}$ ) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports, and receive (active LOW) from B ports to A ports. The output enable ( $\overline{OE}$ ) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition

All CD74FCT2645T and CD74FCT2245T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT245ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT245ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT245CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT245CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT245DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT245DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT245TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT245TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT640ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT640ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT640CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT640CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT640DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT640DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT640TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT640TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT645ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT645ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT645CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT645CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT645DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT645DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT645TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT645TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2245ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2245ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2245CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2245CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2245TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2245TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2645ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2645ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2645CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2645CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2645TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2645TQM	-40 to 85	20 Ld QSOP	M20.15-P

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

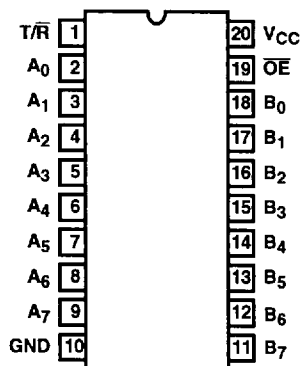
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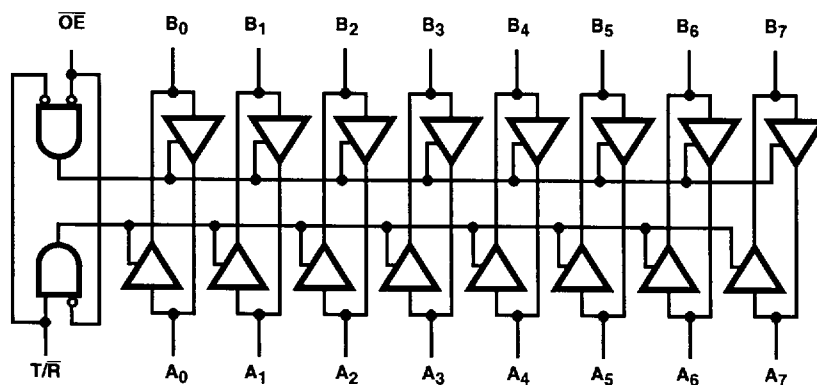
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**Pinout**

CD74FCT245T, CD74FCT640T, CD74FCT645T, CD74FCT2245, CD74FCT2645  
(QSOP, SOIC)  
TOP VIEW



**Functional Block Diagram**



NOTE: CD74FCT245T, CD74FCT2245T, CD74FCT645T, CD74FCT2645T are non-inverting options. CD74FCT640T is the inverting option.

TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
OE	T/R	
L	L	Bus B Data to Bus A (NOTE 2)
L	H	Bus A Data to Bus B (NOTE 2)
H	X	High Z State

NOTES:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High Impedance
- CD74FCT640T is inverting from input to output.

**Pin Descriptions**

PIN NAME	DESCRIPTION
OE	Three-State Output Enable Inputs (Active LOW)
T/R	Transmit/Receive Input
A <sub>0</sub> -A <sub>7</sub>	Side A Inputs or three-State Outputs
B <sub>0</sub> -B <sub>7</sub>	Side B Inputs or three-State Outputs
GND	Ground
V <sub>CC</sub>	Power

# CD74FCT245T, CD74FCT640T, CD74FCT645T, CD74FCT2245T, CD74FCT2645T

## Absolute Maximum Ratings

DC Input Voltage .....	-0.5V to 7.0V
DC Output Current .....	120mA

## Operating Conditions

Operating Temperature Range .....	-40°C to 85°C
Supply Voltage to Ground Potential	
Inputs and V <sub>CC</sub> Only .....	-0.5V to 7.0V
Supply Voltage to Ground Potential	
Outputs and D/O Only .....	-0.5V to 7.0V

## Thermal Information

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ (°C/W)
SOIC Package .....	87
QSOP Package .....	110
Maximum Junction Temperature .....	150°C
Maximum Storage Temperature Range .....	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(Lead Tips Only)	

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## NOTES:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications

PARAMETERS	SYMBOL	(NOTE 4) TEST CONDITIONS	MIN	(NOTE 5) TYP	MAX	UNITS
<b>DC ELECTRICAL SPECIFICATIONS</b> Over the Operating Range, $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , $V_{CC} = 5.0\text{V} \pm 5\%$						
Output HIGH Voltage	$V_{OH}$	$V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -15.0\text{mA}$	2.4	3.0	- V
Output LOW Voltage	$V_{OL}$	$V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 64\text{mA}$	-	0.3	0.50 V
Output LOW Voltage	$V_{OL}$	$V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 12\text{mA}$ (25 $\Omega$ Series)	-	0.3	0.50 V
Input HIGH Voltage	$V_{IH}$	Guaranteed Logic HIGH Level		2.0	-	- V
Input LOW Voltage	$V_{IL}$	Guaranteed Logic LOW Level		-	-	0.8 V
Input HIGH Current	$I_{IH}$	(Except I/O pins) $V_{CC} = \text{Max}$	$V_{IN} = V_{CC}$	-	-	1 $\mu\text{A}$
Input LOW Current	$I_{IL}$	(Except I/O pins) $V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$	-	-	-1 $\mu\text{A}$
Input HIGH Current	$I_{IH}$	(I/O pins only) $V_{CC} = \text{Max}$	$V_{IN} = V_{CC}$	-	-	1 $\mu\text{A}$
Input LOW Current	$I_{IL}$	(I/O pins only) $V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$	-	-	-1 $\mu\text{A}$
HIGH Impedance Output Current	$I_{OZH}$	$V_{CC} = \text{Max}$	$V_{OUT} = 2.7\text{V}$	-	-	1 $\mu\text{A}$
	$I_{OZL}$		$V_{OUT} = 0.5\text{V}$	-	-	-1 $\mu\text{A}$
Clamp Diode Voltage	$V_{IK}$	$V_{CC} = \text{Min}$ , $I_{IN} = -18\text{mA}$		-	-0.7	-1.2 V
Short Circuit Current	$I_{OS}$	$V_{CC} = \text{Max}$ (Note 6), $V_{OUT} = \text{GND}$		-60	-120	- mA
Power Down Disable	$I_{OFF}$	$V_{CC} = \text{GND}$ , $V_{OUT} = 4.5\text{V}$		-	-	100 $\mu\text{A}$
Input Hysteresis	$V_H$			-	200	- mV
<b>CAPACITANCE</b> $T_A = 25^\circ\text{C}$ , $f = 1\text{MHz}$						
Input Capacitance (Note 7)	$C_{IN}$	$V_{IN} = 0\text{V}$		-	6	10 pF
Output Capacitance (Note 7)	$C_{OUT}$	$V_{OUT} = 0\text{V}$		-	8	12 pF
<b>POWER SUPPLY SPECIFICATIONS</b>						
Quiescent Power Supply Current	$I_{CC}$	$V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$ or $V_{CC}$	-	0.1	500 $\mu\text{A}$

**CD74FCT245T, CD74FCT640T, CD74FCT645T, CD74FCT2245T, CD74FCT2645T**

**Electrical Specifications (Continued)**

PARAMETERS	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5)	MAX	UNITS
					TYP		
Supply Current per Input at TTL HIGH	$I_{CC}$	$V_{CC} = \text{Max}$	$V_{IN} = 3.4V$ (Note 8)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 9)	$I_{CCD}$	$V_{CC} = \text{Max}$ , Outputs Open $\overline{OE} = \text{GND}$ $T/\overline{R} = \text{GND}$ or $V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 11)	$I_C$	$V_{CC} = \text{Max}$ , Outputs Open $f_T = 10\text{MHz}$ , 50% Duty Cycle $T/\overline{R} = \overline{OE} = \text{GND}$ One Bit toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	1.5	3.5 (Note 10)	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	-	1.8	4.5 (Note 10)	mA
		$V_{CC} = \text{Max}$ , Outputs Open $f_T = 2.5\text{MHz}$ , 50% Duty Cycle $T/\overline{R} = \overline{OE} = \text{GND}$ Eight Bits toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	3.0	6.0 (Note 10)	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	-	5.0	14.0 (Note 10)	mA

**Switching Specifications Over Operating Range**

PARAMETER	SYMBOL	(NOTE 12) TEST CONDITIONS	T		AT		CT		DT		UNITS
			(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	
			<b>CD74FCT245T, CD74FCT2245T</b>								
Propagation Delay A to B, B to A	$t_{PLH}$ , $t_{PHL}$	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	7.0	1.5	4.6	1.5	4.1	1.5	3.8	ns
Output Enable Time $\overline{OE}$ to A or B	$t_{PZH}$ , $t_{PZL}$		1.5	9.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
Output Disable Time $\overline{OE}$ to A or B (Note 14)	$t_{PHZ}$ , $t_{PLZ}$		1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	ns
Output Enable Time $T/\overline{R}$ to A or B	$t_{PZH}$ , $t_{PZL}$		1.5	9.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
Output Disable Time $T/\overline{R}$ to A or B (Note 14)	$t_{PHZ}$ , $t_{PLZ}$		1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	ns
<b>CD74FCT640T</b>											
Propagation Delay A to B, B to A	$t_{PLH}$ , $t_{PHL}$	$C_L = 50\text{pF}$ $R_L = 500\Omega$	2	7.0	1.5	5.0	1.5	4.4	1.5	3.7	ns
Output Enable Time $\overline{OE}$ to A or B	$t_{PZH}$ , $t_{PZL}$		2	13.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
Output Disable Time $\overline{OE}$ to A or B (Note 14)	$t_{PHZ}$ , $t_{PLZ}$		2	10.0	1.5	5.0	1.5	4.8	1.5	4.3	ns
Output Enable Time $T/\overline{R}$ to A or B	$t_{PZH}$ , $t_{PZL}$		2	13.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
Output Disable Time $T/\overline{R}$ to A or B (Note 14)	$t_{PHZ}$ , $t_{PLZ}$		2	10.0	1.5	5.0	1.5	4.8	1.5	4.3	ns

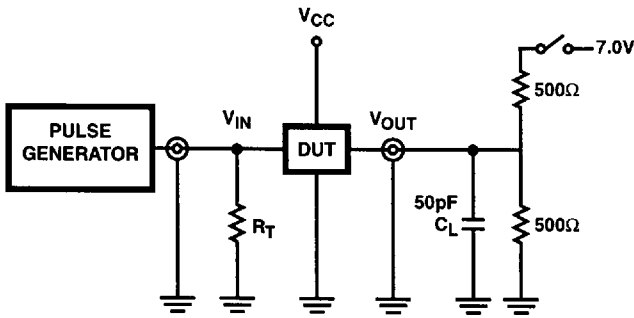
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 12) TEST CONDITIONS	T		AT		CT		DT		UNITS
			(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	
CD74FCT645T, CD74FCT2645T											
Propagation Delay A to B, B to A	$t_{PLH}$ , $t_{PHL}$	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	9.5	1.5	4.6	1.5	4.1	1.5	3.8	ns
Output Enable Time $\overline{OE}$ to A or B	$t_{PZH}$ , $t_{PZL}$		1.5	11.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
Output Disable Time $\overline{OE}$ to A or B (Note 14)	$t_{PHZ}$ , $t_{PLZ}$		1.5	12.0	1.5	5.0	1.5	4.8	1.5	4.3	ns
Output Enable Time T/R to A or B	$t_{PZH}$ , $t_{PZL}$		1.5	11.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
Output Disable Time T/R to A or B (Note 14)	$t_{PHZ}$ , $t_{PLZ}$		1.5	12.0	1.5	5.0	1.5	4.8	1.5	4.3	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Characteristics for the applicable device type.
5. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $25^\circ\text{C}$  ambient and maximum loading.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. This parameter is determined by device characterization but is not production tested.
8. Per TTL driven input ( $V_{IN} = 3.4\text{V}$ ); all other inputs at  $V_{CC}$  or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
10. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
11.  $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$   
 $I_{CC}$  = Quiescent Current  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4\text{V}$ )  
 $D_H$  = Duty Cycle for TTL Inputs High  
 $N_T$  = Number of TTL Inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 $f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 $f_I$  = Input Frequency  
 $N_I$  = Number of Inputs at  $f_I$   
 All currents are in milliamps and all frequencies are in megahertz.
12. See test circuit and wave forms.
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION	
TEST	SWITCH
$t_{PLZ}$ , $t_{PZL}$	Closed
$t_{PHZ}$ , $t_{PZH}$ , $t_{PLH}$ , $t_{PHL}$	Open

DEFINITIONS:

$C_L$  = Load capacitance, includes jig and probe capacitance.  
 $R_T$  = Termination resistance, should be equal to  $Z_{OUT}$  of the Pulse Generator.

NOTE:

15. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $Z_{OUT} \leq 50\Omega$ ;  
 $t_f$ ,  $t_r \leq 2.5\text{ns}$ .

FIGURE 1. TEST CIRCUIT

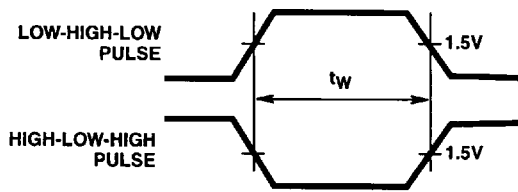


FIGURE 2. PULSE WIDTH

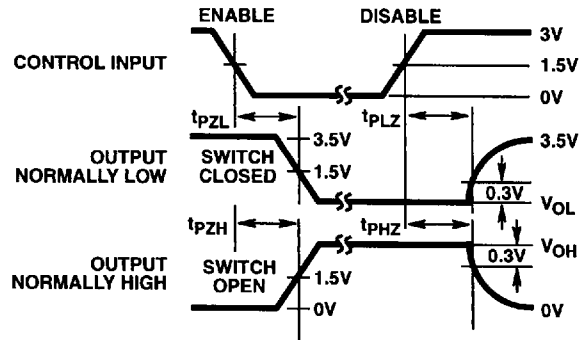


FIGURE 3. ENABLE AND DISABLE TIMING

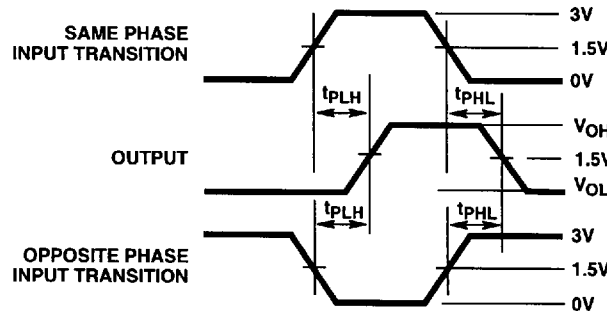
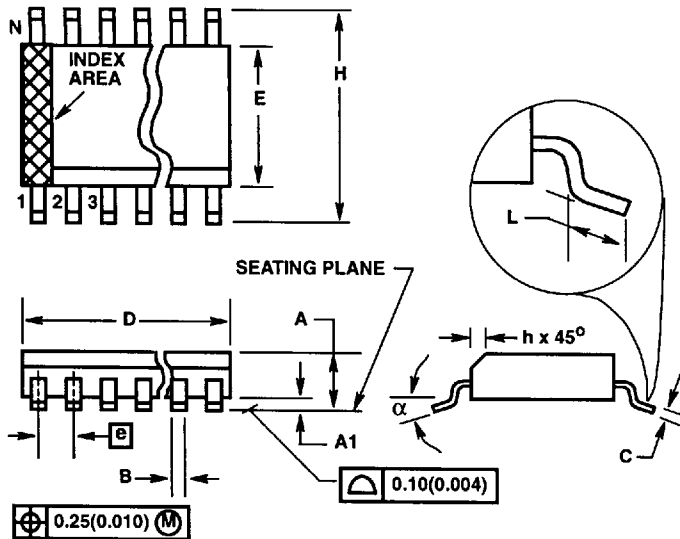


FIGURE 4. PROPAGATION DELAY

Small Outline Plastic Packages (SOIC)



M20.3-P  
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

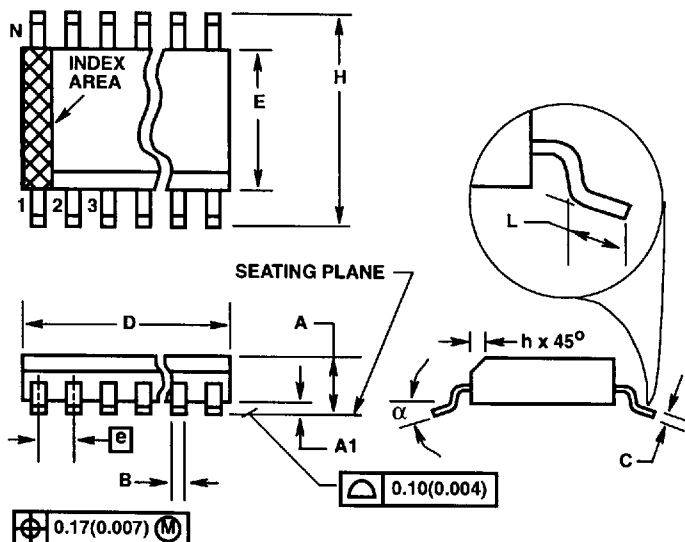
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.092	0.105	2.34	2.67	-
A1	0.004	0.012	0.102	0.302	-
B	0.013	0.020	0.330	0.508	-
C	0.009	0.011	0.229	0.279	-
D	0.496	0.512	12.60	13.00	1
E	0.291	0.299	7.39	7.59	2
e	0.050 BSC		1.27 BSC		-
H	0.401	0.411	10.18	10.44	-
h	0.010	0.029	0.254	0.737	-
L	0.016	0.050	0.41	1.27	3
N	20		20		4
α	0°	8°	0°	8°	-

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NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

### Shrink Small Outline Plastic Packages (SSOP/QSOP)



**M20.15-P**  
20 LEAD SHRINK NARROW BODY SMALL OUTLINE  
PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.007	0.011	0.178	0.279	-
B	0.008	0.012	0.203	0.305	-
C	0.007	0.010	0.178	0.254	-
D	0.337	0.344	8.56	8.74	1
E	0.149	0.157	3.78	3.99	2
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.79	6.20	-
h	0.015		0.38		-
L	0.016	0.050	0.41	1.27	3
N	20		20		4
$\alpha$	0°	8°	0°	8°	-

Rev. 1 7/96

**NOTES:**

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

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