FemtoClock® Crystal/LVCMOS-to-LVDS/LVCMOS Frequency Synthesizer

ICS8440259I-45

DATA SHEET

General Description

The ICS8440259I-45 is a nine output synthesizer optimized to generate Gigabit and 10 Gigabit Ethernet clocks. Using a 25MHz, 18pF parallel resonant crystal, the device will generate 156.25MHz, 125MHz and 3.90625MHz clocks with mixed LVDS and LVCMOS/LVTTL output levels. The ICS8440259I-45 uses IDT's 3RD generation low phase noise VCO technology and can achieve <1ps typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS8440259I-45 is packaged in a small, 5mm x 5mm VFQFN package that is optimum for applications with space limitations.

Features

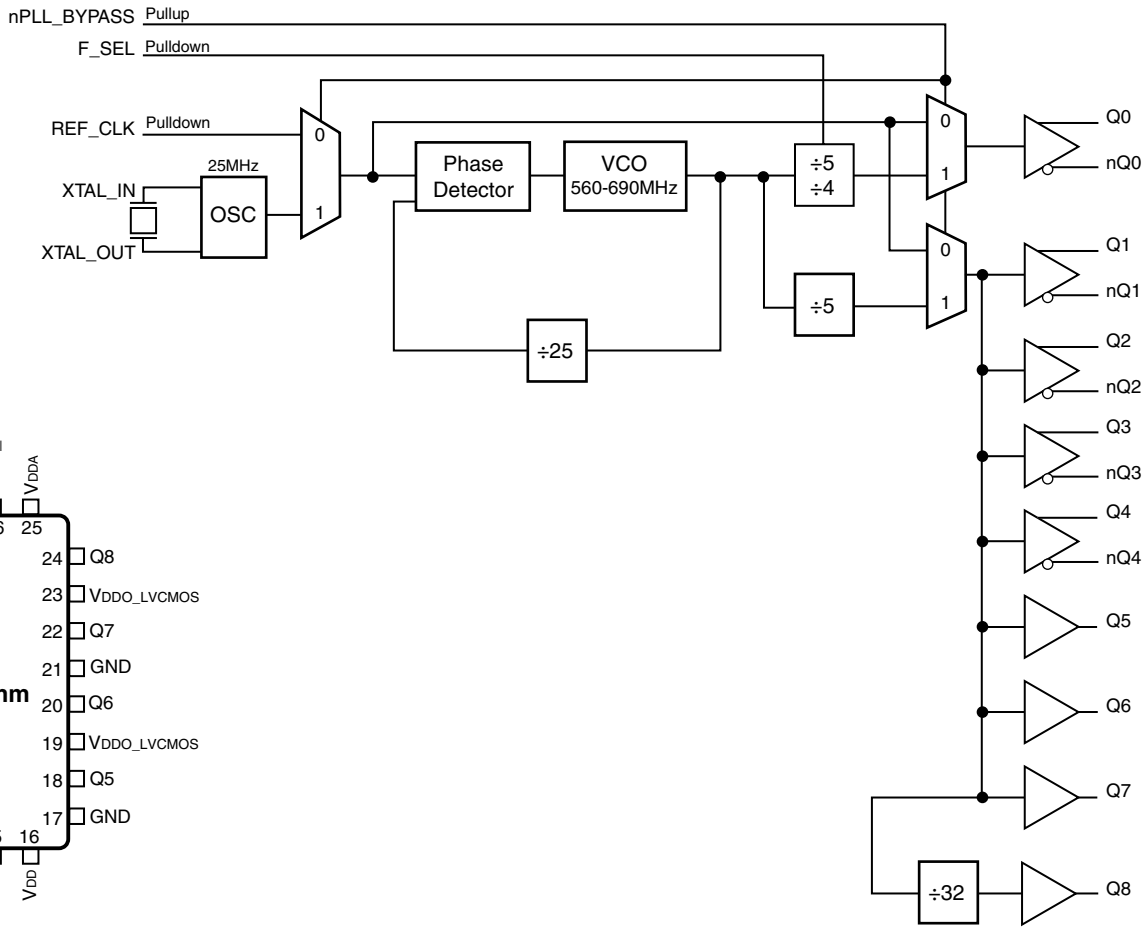
- One differential LVDS output at 156.25MHz or 125MHz

  Four differential LVDS outputs at 125MHz

  Three LVCMOS/LVTTL single-ended outputs at 125MHz

  One LVCMOS/LVTTL single-ended output at 3.90625MHz
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input and PLL bypass from a single select pin
- VCO range: 560MHz - 690MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.45ps (typical), LVDS outputs
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.45ps (typical), Q0, nQ0 output
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment

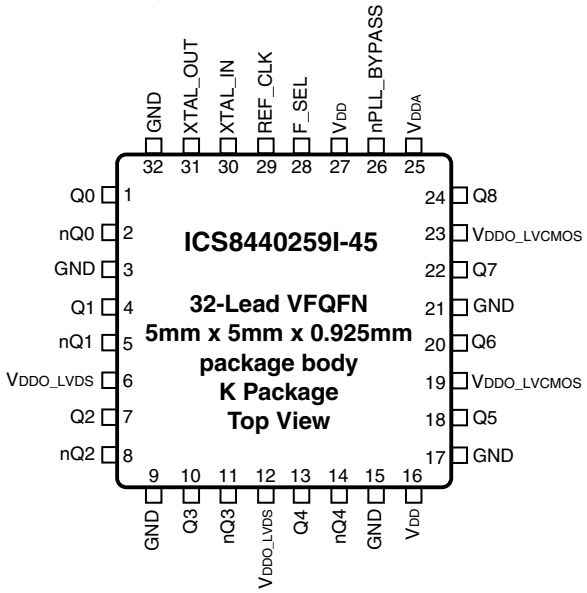


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential clock outputs. LVDS interface levels.
3, 9, 15, 17, 21, 32	GND	Power		Power supply ground.
4, 5	Q1, nQ1	Output		Differential clock outputs. LVDS interface levels.
6, 12	V_{DDO_LVDS}	Power		Output supply pins for Q[0:4], nQ[0:4] LVDS outputs.
7, 8	Q2, nQ2	Output		Differential clock outputs. LVDS interface levels.
10, 11	Q3, nQ3	Output		Differential clock outputs. LVDS interface levels.
13, 14	Q4, nQ4	Output		Differential clock outputs. LVDS interface levels.
16, 27	V_{DD}	Power		Core supply pins.
18, 20, 22, 24	Q5, Q6, Q7, Q8	Output		Single-ended clock outputs.LVCMOS/LVTTL interface levels.
19, 23	V_{DDO_LVCMOS}	Power		Output supply pins for Q[5:8] LVCMOS outputs.
25	V_{DDA}	Power		Analog supply pin.
26	nPLL_BYPASS	Input	Pullup	Input select and PLL bypass control pin. See Table 3B. LVCMOS/LVTTL interface levels.
28	F_SEL	Input	Pulldown	Frequency select pin. See Table 3A. LVCMOS/LVTTL interface levels.
29	REF_CLK	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
30, 31	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_OUT is the output, XTAL_IN is the input.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
C_{PD}	Power Dissipation Capacitance (per output)	Q[5:8]	V_{DDO_LVCMOS} = 3.465V		8		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	Q[5:8]	V_{DDO_LVCMOS} = 3.3V		20		Ω

Function Tables

Table 3A. F_SEL Frequency Select Function Table

Input		Output Frequency
F_SEL	**Output Divider Value**	**Q0, nQ0 (MHz)**
0	÷5	125 (default)
1	÷4	156.25

Table 3B. PLL Bypass and Input Select Function Table

Inputs		
nPLL_BYPASS	**PLL BYPASS**	**Input Selected**
0	PLL Bypassed	REF_CLK
1	PLL Enabled	XTAL_IN, XTAL_OUT (default)

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, I_O (LVCMOS)	-0.5V to V_{DDO_LVCMOS} + 0.5V
Outputs, I_O (LVDS) Continuous Current Surge Current	 10mA 15mA
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO\_LVCMOS} = V_{DDO\_LVDS} = 3.3V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.35	3.3	V_{DD}	V
V_{DDO_LVCMOS}, V_{DDO_LVDS}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				105	mA
I_{DDA}	Analog Supply Current				35	mA
I_{DDO_LVCMOS}	LVCMOS Output Supply Current				4	mA
I_{DDO_LVDS}	LVDS Output Supply Current				77	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO\_LVCMOS} = 3.3V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	REF_CLK, F_SEL	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nPLL_BYPASS	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	REF_CLK, F_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nPLL_BYPASS	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage	Q[5:8]	I_{OH} = -12mA	2.6			V
V_{OL}	Output Low Voltage	Q[5:8]	I_{OL} = 12mA			0.5	V

Table 4C. LVDS DC Characteristics, $V_{DD} = V_{DDO\_LVDS} = 3.3V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		250		520	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.20		1.55	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

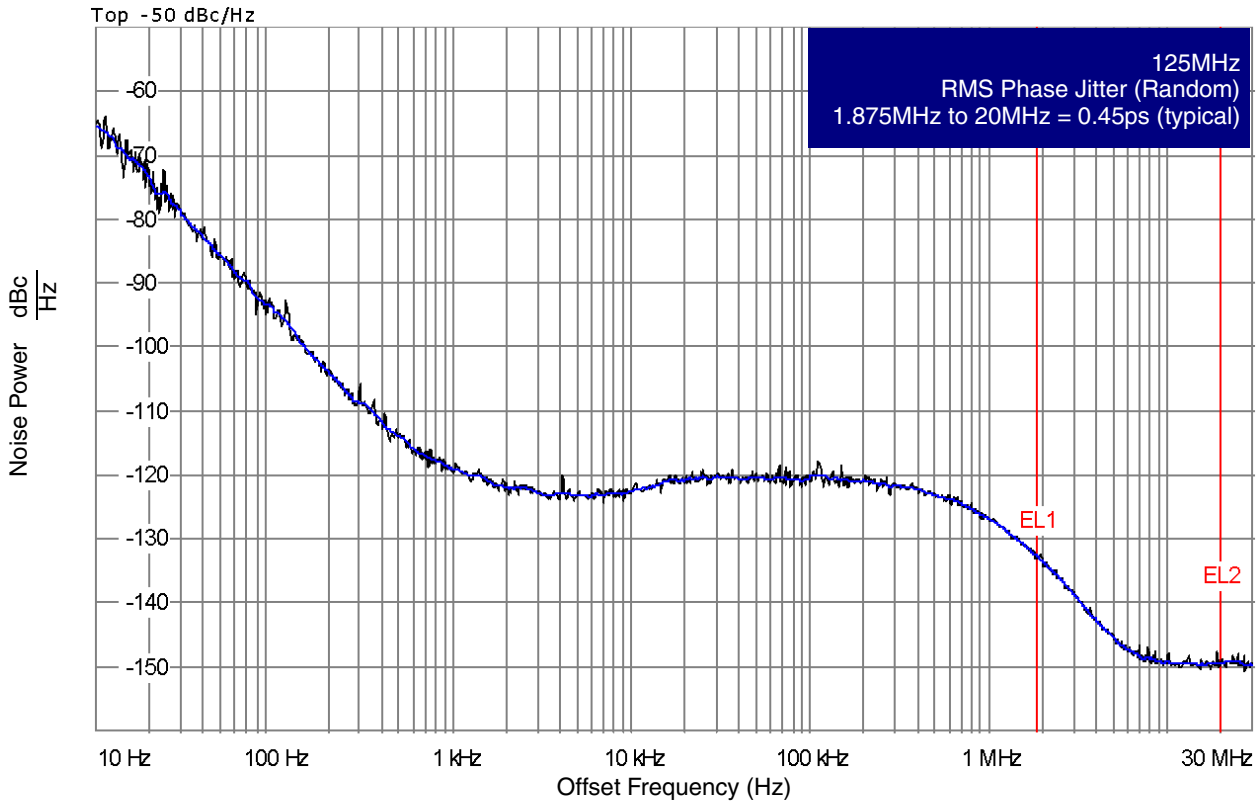
AC Electrical Characteristics

Table 6. AC Characteristics, $V_{DD} = V_{DDO\_LVCMOS} = V_{DDO\_LVDS} = 3.3V±5\%$, T_A = -40°C to 85°C

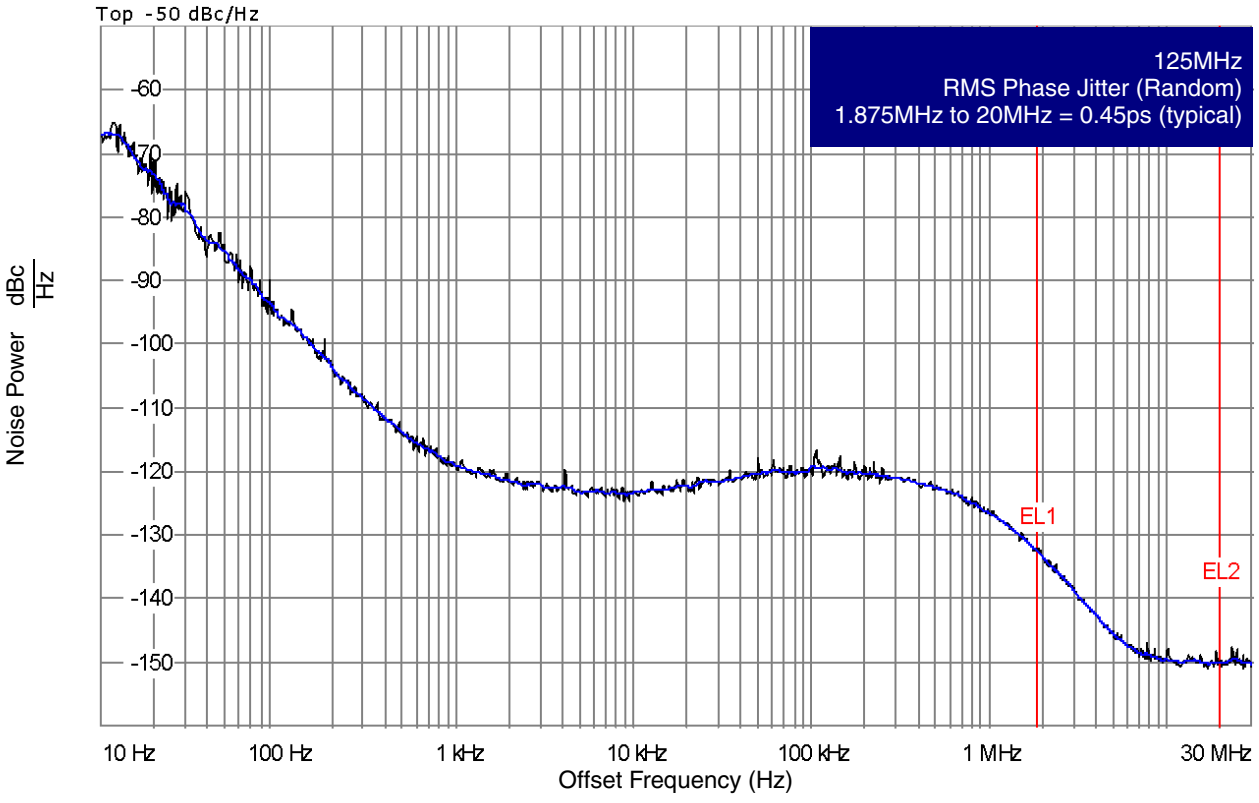
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{out}	Output Frequency	Q[0:4], nQ[0:4]	F_SEL = 0 (default)		125		MHz
		Q[5:7]	F_SEL = 0 (default)		125		MHz
		Q8	F_SEL = 0 (default)		3.90625		MHz
		Q0, nQ0	F_SEL = 1		156.25		MHz
		Q[1:4], nQ[1:4]			125		MHz
*t*jit(Ø)	RMS Phase Noise Jitter; NOTE 1 PLL Mode	Q[0:4], nQ[0:4]	125MHz, Integration Range: 1.875MHz - 20MHz		0.45		ps
		Q0, nQ0	156.25MHz, Integration Range: 1.875MHz - 20MHz		0.45		ps
		Q[5:7]	125MHz, Integration Range: 1.875MHz - 20MHz		0.45		ps
t_R / t_F	Output Rise/Fall Time	Q[0:4], nQ[0:4]; NOTE 2	PLL Mode, 125MHz, 30% to 70%	130		665	ps
		Q[0:4], nQ[0:4]	PLL Mode, 125MHz, 20% to 80%	155		700	ps
		Q0, nQ0	PLL Mode, 156.25MHz, 20% to 80%	115		565	ps
		Q[5:7]	PLL Mode, 125MHz, 20% to 80%	400		1000	ps
		Q8	3.90625MHz, 20% to 80%	475		1250	ps
odc	Output Duty Cycle, PLL Mode	Q[0:4], nQ[0:4]	125MHz	45		55	%
		Q0, nQ0	156.25MHz	48		52	%
		Q[5:7]	125MHz	45		55	%
		Q8	3.90625MHz	49		51	%
odc	Output Duty Cycle, Bypass Mode	Q[0:4], nQ[0:4]	125MHz	47		53	%
		Q0, nQ0	156.25MHz	46		54	%
		Q[5:7]	125MHz	47		53	%
		Q8	3.90625MHz	49		51	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Refer to Phase Noise Plots.
NOTE 2: Output loaded with 100Ω differential and 15pF loads.

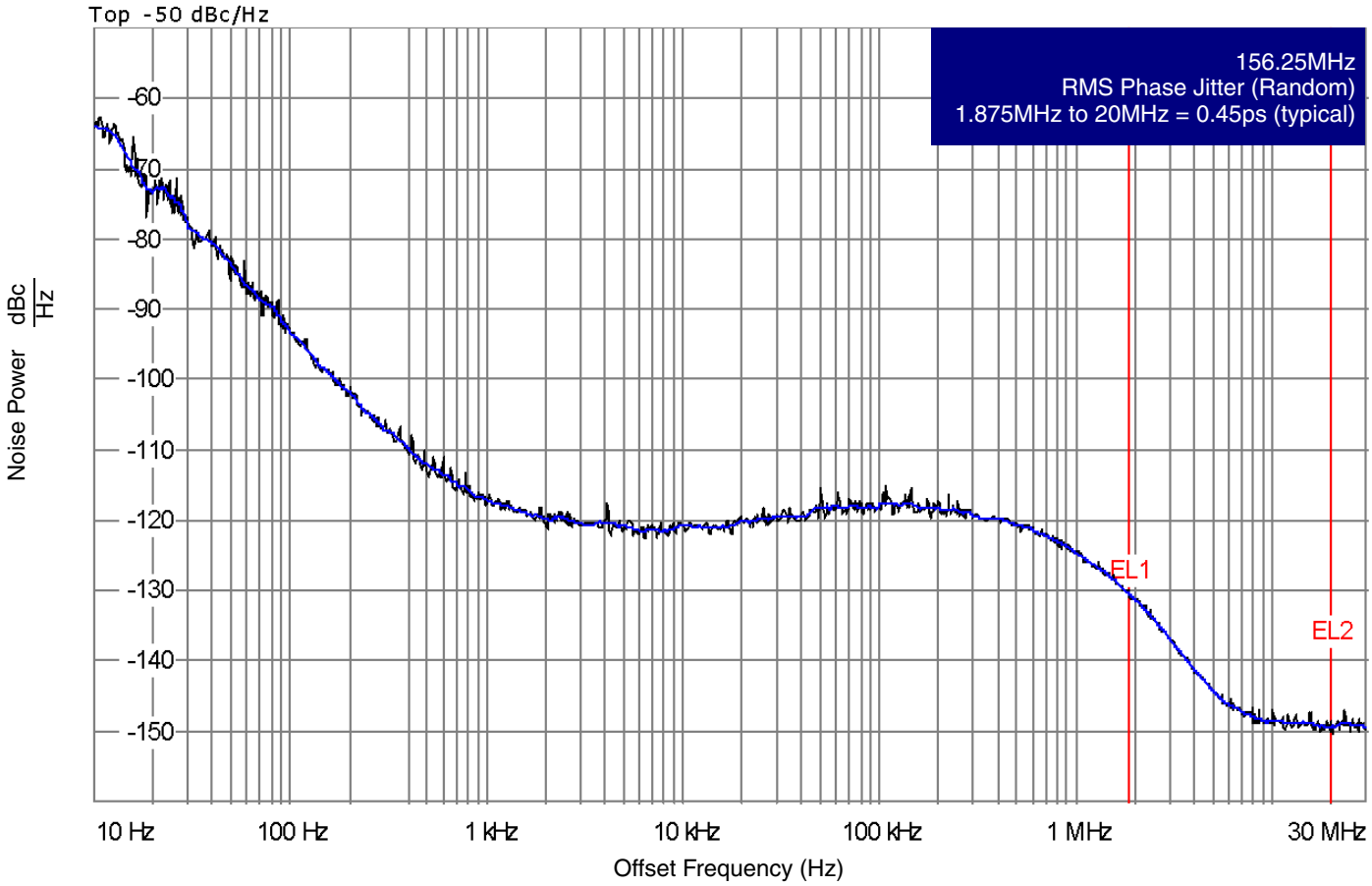
Typical Phase Noise at 125MHz (Q[0:4])



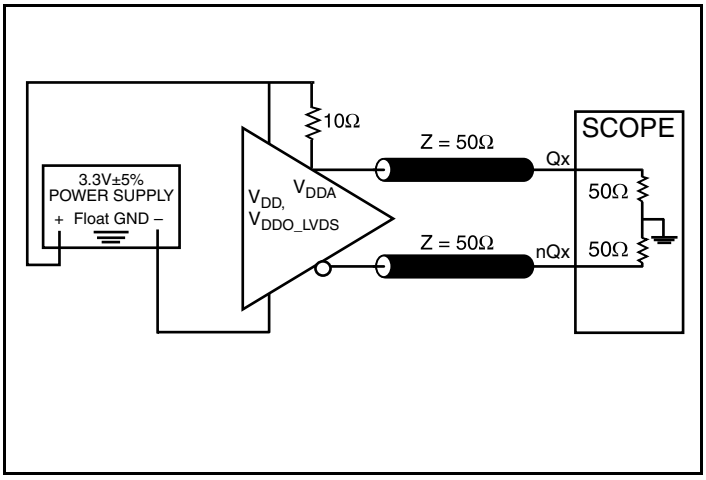
Typical Phase Noise at 125MHz (Q[5:7])



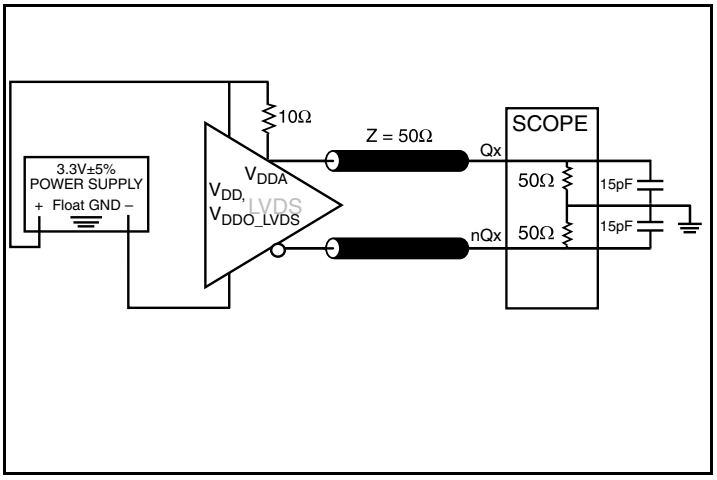
Typical Phase Noise at 156.25MHz (Q0)



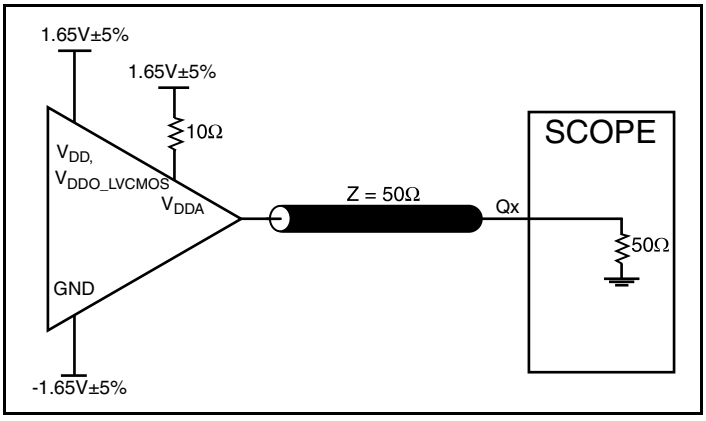
Parameter Measurement Information



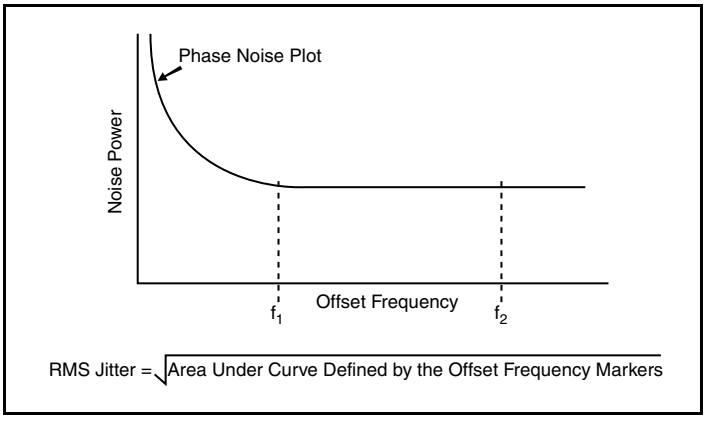
LVDS Output Load AC Test Circuit



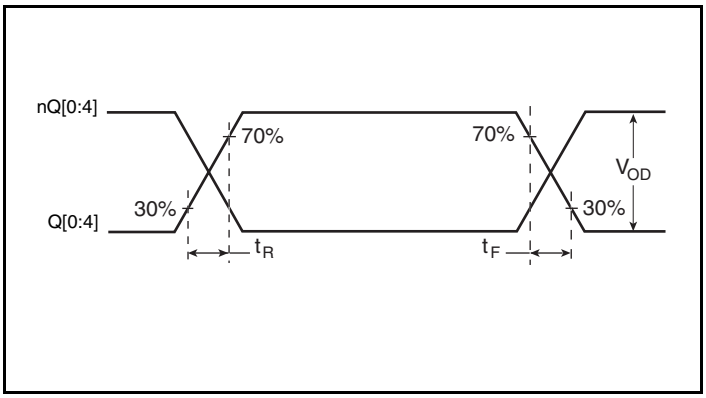
LVDS Output Load AC Test Circuit with 15pF



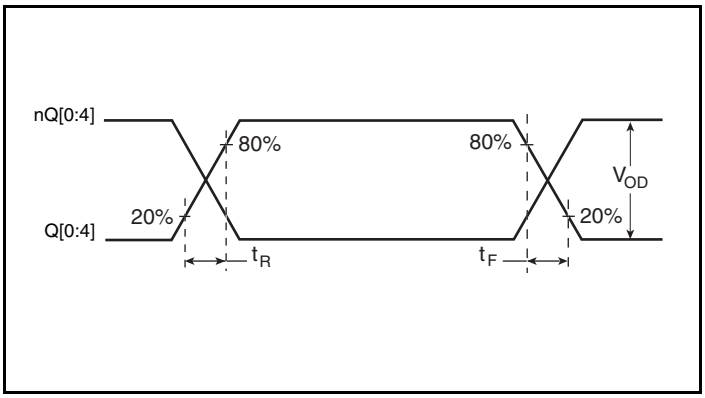
LVCMOS Output Load AC Test Circuit



RMS Phase Jitter

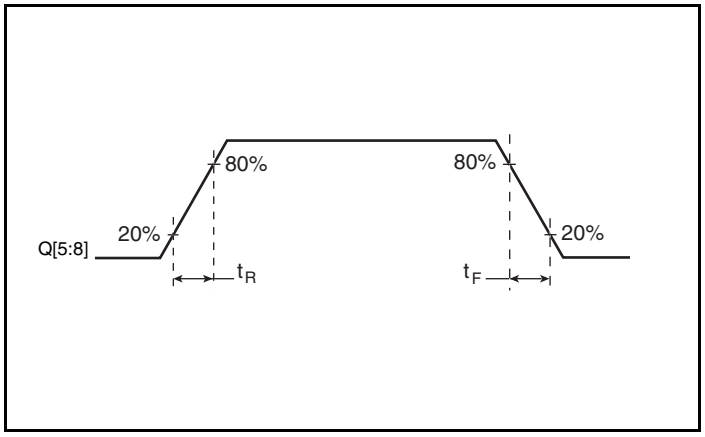


LVDS Output Rise/Fall Time

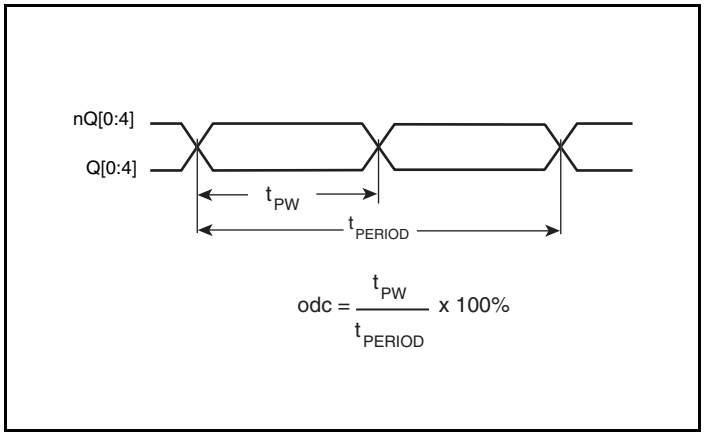


LVDS Output Rise/Fall Time

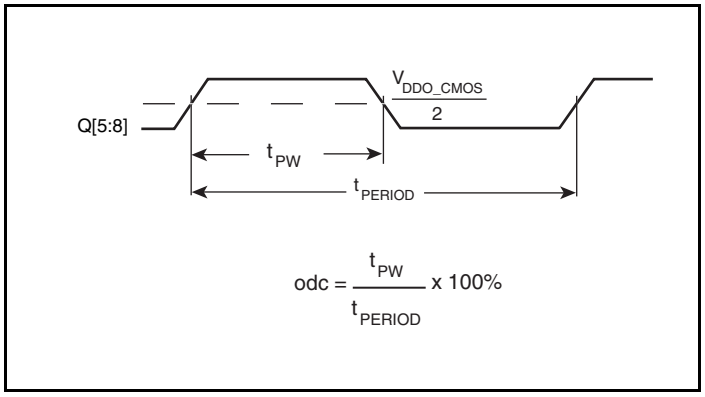
Parameter Measurement Information, continued



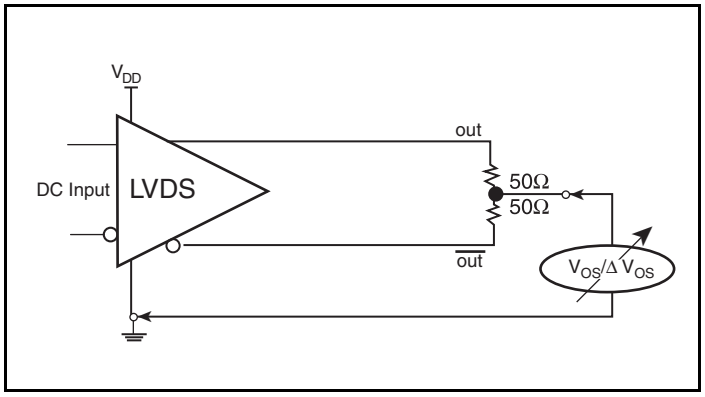
LVCMOS Output Rise/Fall Time



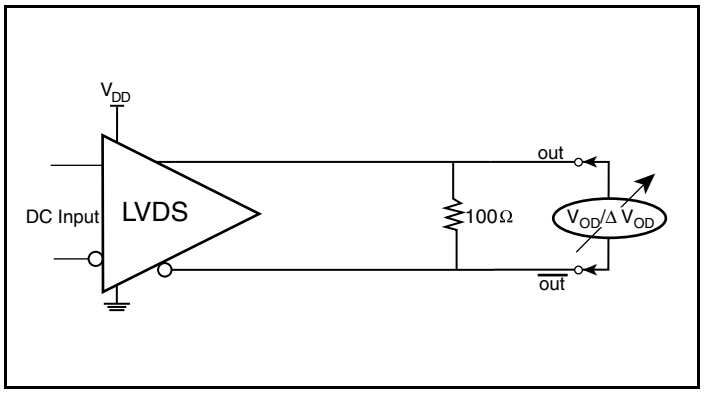
Differential Output Duty Cycle/Pulse Width/Period



Single-Ended Output Duty Cycle/Pulse Width/Period



Offset Voltage Setup



Differential Output Voltage Setup

Applications Information

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 1A.* The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

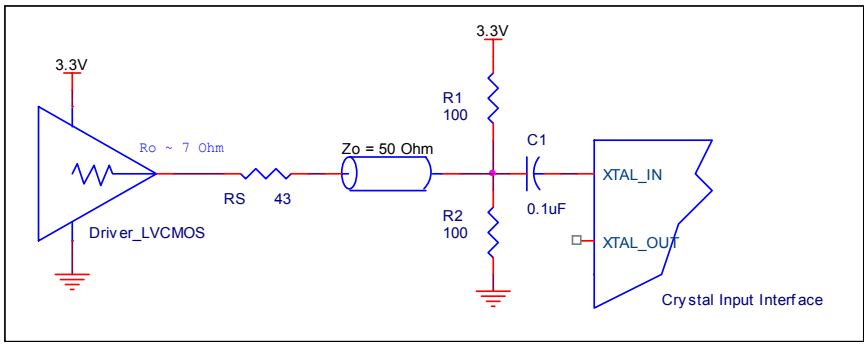


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

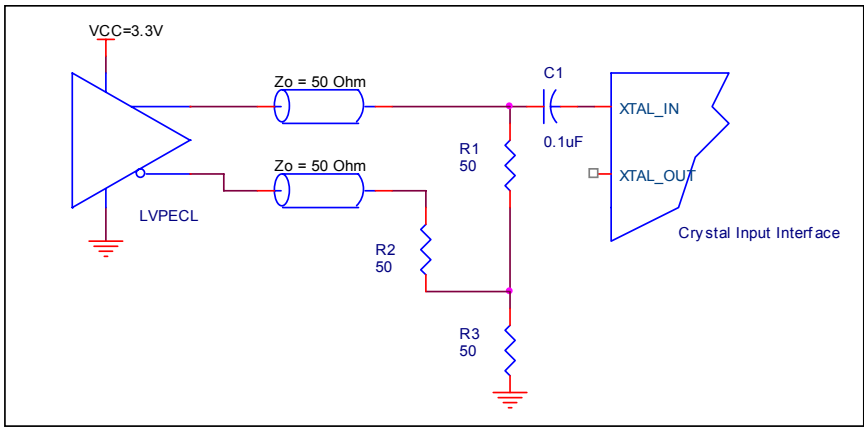


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

LVDS Driver Termination

A general LVDS interface is shown in *Figure 2.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 2 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the amplitude and common mode input range of the input receivers should be verified for compatibility with the output.

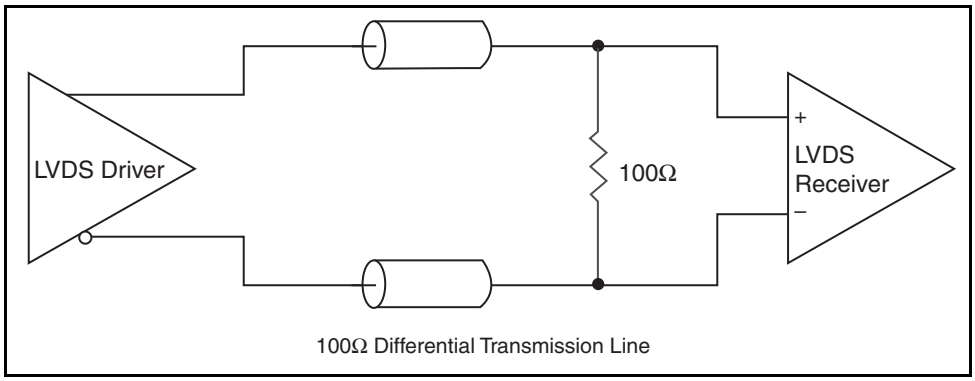


Figure 2. Typical LVDS Driver Termination

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

Outputs:

LVDS Outputs

All unused LVDS outputs should be terminated with 100Ω resistor between the differential pair.

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally Electrically Enhance Leadframe Base Package, Amkor Technology.

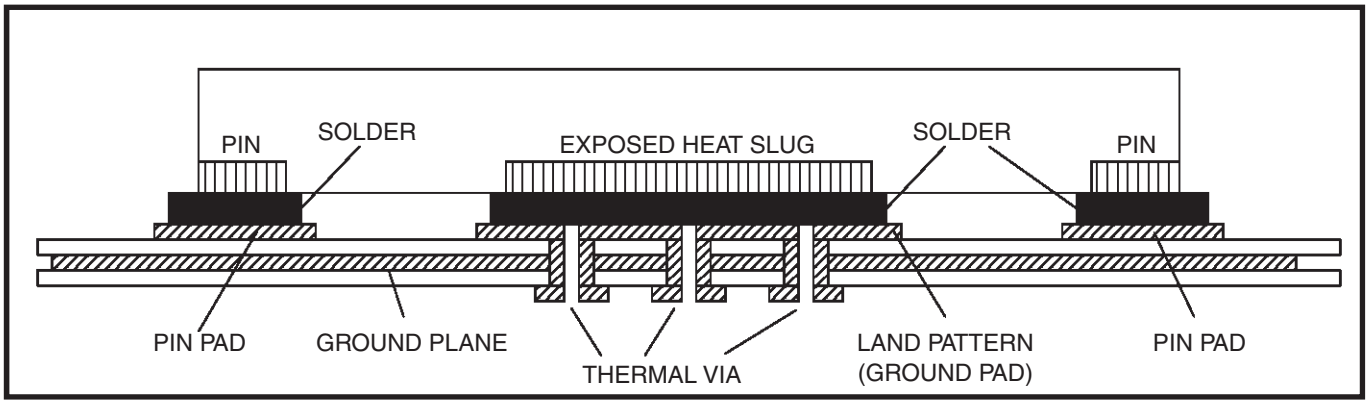


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Example

Figure 4 (on the next page) shows an example of ICS8440259I-45 application schematic. In this example, the device is operated at V_{DD} = V_{DDO_LVDS} = V_{DDO_LVCMOS} = 3.3V. An 18pF parallel resonant 25MHz crystal is used. The load capacitance C1 = 33pF and C2 = 27pF are recommended for frequency accuracy. Depending on the parasitics of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The ICS8440259I-45 provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

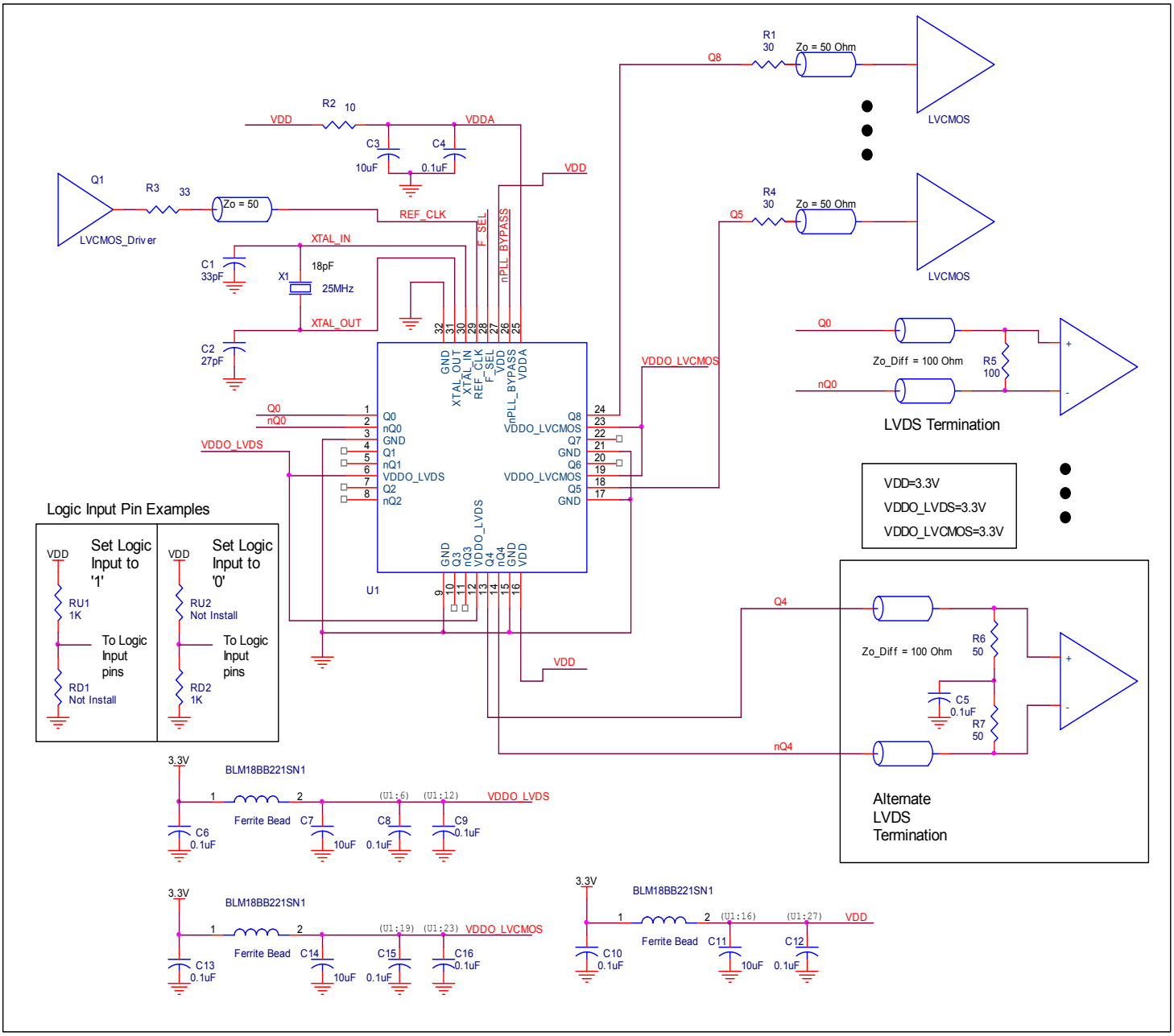


Figure 4. ICS8440259I-45 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8440259I-45.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8440259I-45 is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

Core and LVDS, LVCMOS Output Power Dissipation

- Power (core) = V_{DD_MAX} * (I_{DD} + I_{DDO_LVDS} + I_{DDO_LVCMOS} + I_{DDA}) = 3.465V * (105mA + 77mA + 4mA + 35mA) = **765.765mW**

LVCMOS Output Power Dissipation

- Dynamic Power Dissipation at 125MHz, (Q[5:7])
  Power (125MHz) = C_{PD} * Frequency * $(V_{DDO})^2$ = 8pF * 125MHz * $(3.465V)^2$ = **12mW per output**
  Total Power (125MHz) = **12mW * 3 = 36mW**

- Dynamic Power Dissipation at 3.9MHz, (Q8)
  Power (3.9MHz) = C_{PD} * Frequency * $(V_{DDO})^2$ = 8pF * 3.90625MHz * $(3.465V)^2$ = **0.4mW**

Total Power Dissipation

- **Total Power**
  = Power (core) + Total Power (125MHz) + Total Power (3.9MHz)
  = 765.765mW + 36mW + 0.4mW
  = 802.165mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.802W * 37°C/W = 114.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

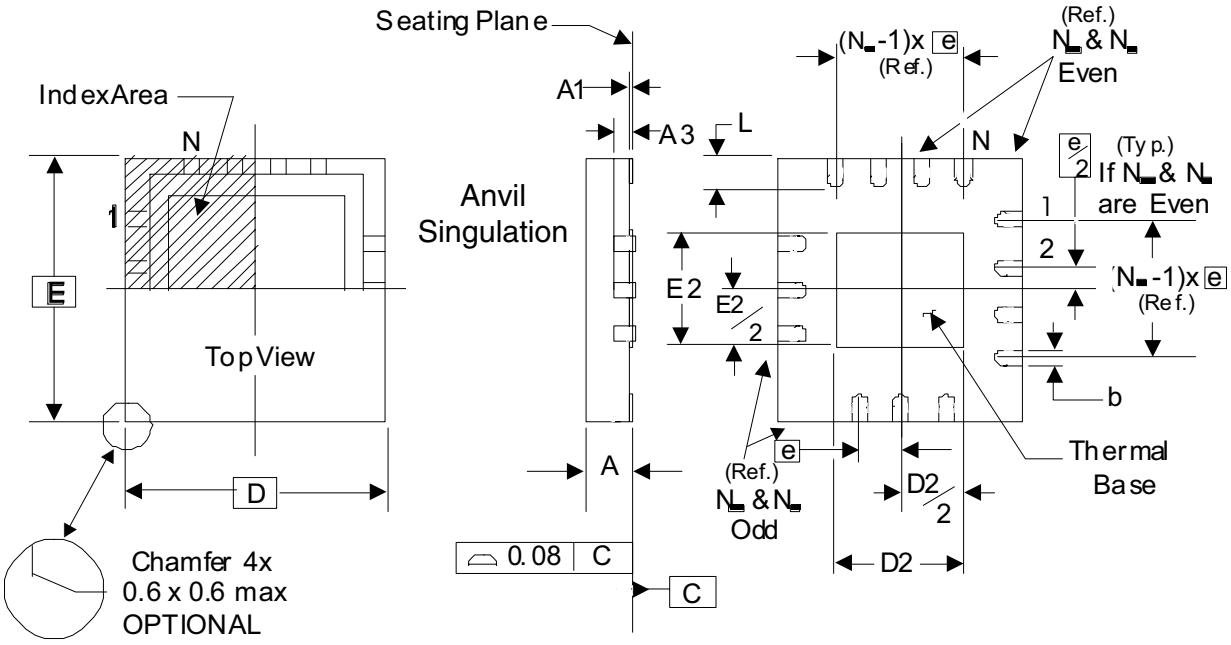
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

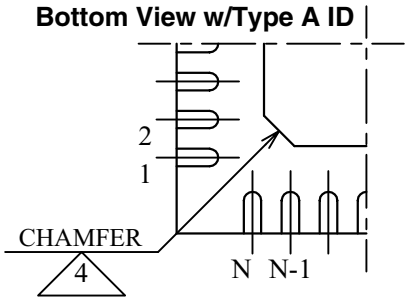
Transistor Count

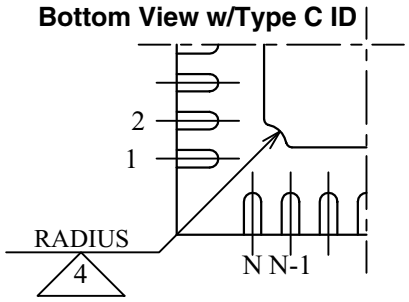
The transistor count for ICS8440259I-45 is: 3666

Package Outline and Package Dimensions

Package Outline - K Suffix for 32 Lead VFQFN







There are 2 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 9. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8440259EKI-45LF	ICS259EI45L	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
8440259EKI-45LFT	ICS259EI45L	“Lead-Free” 32 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.