MOTOROLA

MC74AC109
MC74ACT109

Product Preview

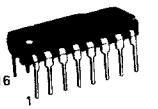
Dual $J\overline{K}$ Positive Edge-Triggered Flip-Flop

DUAL $J\overline{K}$ POSITIVE EDGE-TRIGGERED FLIP-FLOP

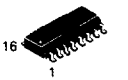
The MC74AC109/74ACT109 consists of two high-speed completely independent transition clocked $J\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $J\overline{K}$ design allows operation as a D flip-flop (refer to MC74AC74/74ACT74 data sheet) by connecting the J and $\overline{K}$ inputs together.

Asynchronous Inputs:
- LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
- LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

- Outputs Source/Sink 24 mA
- 'ACT109 Has TTL Compatible Inputs

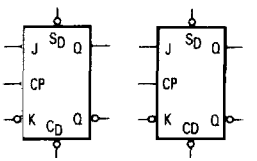


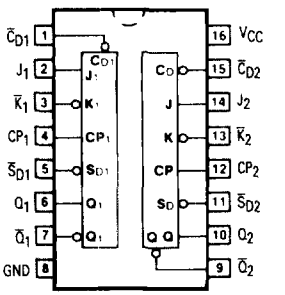
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

$J_1, J_2, \overline{K}_1, \overline{K}_2$	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}, \overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}, \overline{S}_{D2}$	Direct Set Inputs
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs

TRUTH TABLE

Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⎍	L	L	L	H
H	H	⎍	H	L	Toggle	
H	H	⎍	L	H	Q_0	$\overline{Q}_0$
H	H	⎍	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
⎍ = LOW-to-HIGH Clock Transition
X = Immaterial
$Q_0(\overline{Q}_0)$ = Previous $Q_0(\overline{Q}_0)$ before LOW-to-HIGH Transition of Clock

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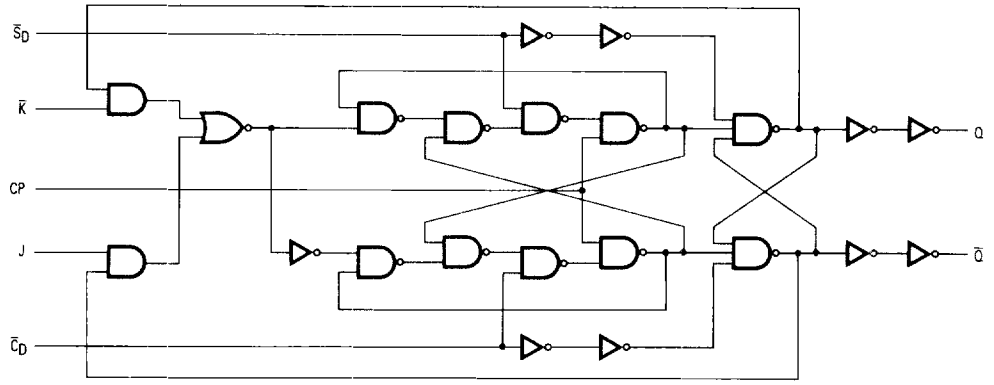
LOGIC DIAGRAM (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	40	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT109)	1.5	mA	V_{IN} = V_{CC} – 2.1 V, V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	125 150	150 175		100 125		MHz	3-3
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	8.0 6.0	13.5 10	1.0 1.0	16 10.5	ns	3-6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	8.0 6.0	14 10	1.0 1.0	14.5 10.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	8.0 6.0	12 9.0	1.0 1.0	13 10	ns	3-6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	10 7.5	12 9.5	1.0 1.0	13.5 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V + 0.5 V

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AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Set-up Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.3 5.0	3.5 2.0	6.5 4.5	7.5 5.0	ns	3-9
t_h	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.3 5.0	−1.5 −0.5	0 0.5	0 0.5	ns	3-9
t_w	Pulse Width CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	3.3 5.0	2.0 2.0	4.0 3.5	4.5 3.5	ns	3-6
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.3 5.0	−2.5 −1.5	0 0	0 0	ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	145	210		125		MHz	3-3
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	1.0	7.0	11	1.0	13	ns	3-6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	1.0	6.0	10	1.0	11.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	1.0	5.5	9.5	1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	1.0	6.0	10	1.0	11.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Set-up Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	0.5	2.0	2.5	ns	3-9
t_h	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	0	2.0	2.0	ns	3-9
t_w	Pulse Width CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	5.0	3.0	5.0	6.0	ns	3-6
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	−2.5	0	0	ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	35	pF	V_{CC} = 5.0 V