

LM5107 100V / 1.4A Peak Half Bridge Gate Driver

Check for Samples: [LM5107](#)

FEATURES

- Drives Both a High Side and Low Side N-Channel MOSFET
- High Peak Output Current (1.4A Sink / 1.3A Source)
- Independent TTL compatible inputs
- Integrated Bootstrap Diode
- Bootstrap Supply Voltage to 118V DC
- Fast Propagation Times (27 ns Typical)
- Drives 1000 pF Load with 15ns Rise and Fall Times
- Excellent Propagation Delay Matching (2 ns Typical)
- Supply Rail Under-Voltage Lockout
- Low Power Consumption
- Pin Compatible with ISL6700

TYPICAL APPLICATIONS

- Current Fed Push-Pull Converters
- Half and Full Bridge Power Converters
- Solid State Motor Drives
- Two Switch Forward Power Converters

DESCRIPTION

The LM5107 is a low cost high voltage gate driver, designed to drive both the high side and the low side N-Channel MOSFETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of working with rail voltages up to 100V. The outputs are independently controlled with TTL compatible input thresholds. An integrated on chip high voltage diode is provided to charge the high side gate drive bootstrap capacitor. A robust level shifter technology operates at high speed while consuming low power and providing clean level transitions from the control input logic to the high side gate driver. Under-voltage lockout is provided on both the low side and the high side power rails. The device is available in the SOIC and the thermally enhanced WSON packages.

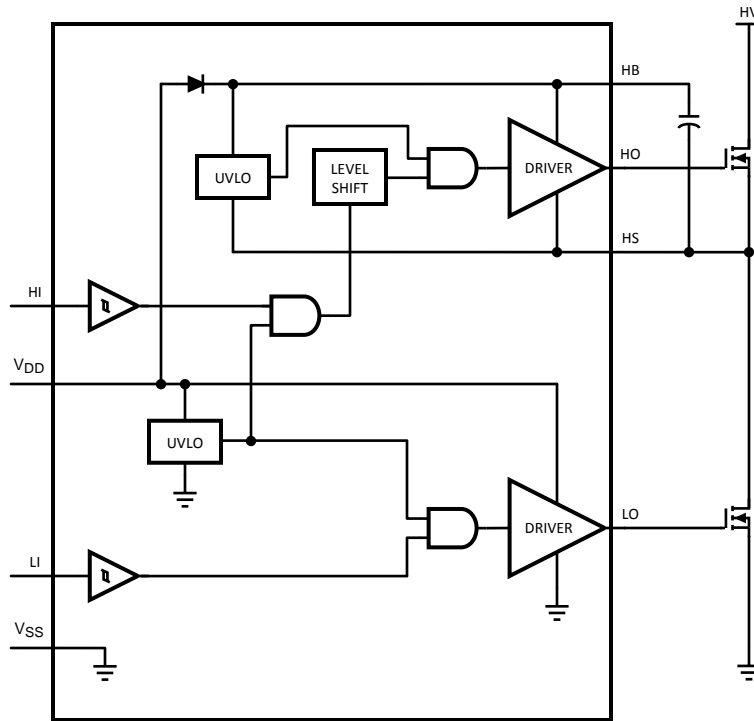
Package

- SOIC
- WSON (4 mm x 4 mm)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Simplified Block Diagram



Connection Diagrams

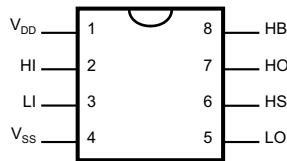


Figure 1. 8-Lead SOIC See D Package

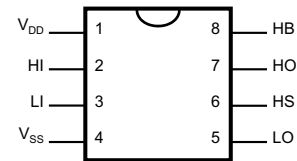


Figure 2. 8-Lead WSON See NGT0008A Package

PIN DESCRIPTIONS⁽¹⁾

Pin #		Name	Description	Application Information
SOIC	WSON			
1	1	V _{DD}	Positive gate drive supply	Locally decouple to V _{SS} using low ESR/ESL capacitor located as close to IC as possible.
2	2	HI	High side control input	The LM5107 HI input is compatible with TTL input thresholds. Unused HI input should be tied to ground and not left open
3	3	LI	Low side control input	The LM5107 LI input is compatible with TTL input thresholds. Unused LI input should be tied to ground and not left open.
4	4	V _{SS}	Ground reference	All signals are referenced to this ground.
5	5	LO	Low side gate driver output	Connect to the gate of the low side N-MOS device.
6	6	HS	High side source connection	Connect to the negative terminal of the bootstrap capacitor and to the source of the high side N-MOS device.
7	7	HO	High side gate driver output	Connect to the gate of the low side N-MOS device.
8	8	HB	High side gate driver positive supply rail	Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal of the bootstrap capacitor to HS. The bootstrap capacitor should be placed as close to IC as possible.

(1) For WSON package it is recommended that the exposed pad on the bottom of the LM5107 be soldered to ground plane on the PCB board and the ground plane should extend out from underneath the package to improve heat dissipation.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

V_{DD} to V_{SS}	-0.3V to 18V
HB to HS	-0.3V to 18V
LI or HI to V_{SS}	-0.3V to $V_{DD} + 0.3V$
LO to V_{SS}	-0.3V to $V_{DD} + 0.3V$
HO to V_{SS}	$V_{HS} - 0.3V$ to $V_{HB} + 0.3V$
HS to V_{SS} ⁽³⁾	-5V to 100V
HB to V_{SS}	118V
Junction Temperature	-40°C to +150°C
Storage Temperature Range	-55°C to +150°C
ESD Rating HBM ⁽⁴⁾	2 kV

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the [Electrical Characteristics](#).
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed -1V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than $V_{DD} - 15V$. For example, if $V_{DD} = 10V$, the negative transients at HS must not exceed -5V.
- (4) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. Pin 6, Pin 7 and Pin 8 are rated at 500V.

Recommended Operating Conditions

V_{DD}	8V to 14V
HS ⁽¹⁾	-1V to 100V
HB	$V_{HS} + 8V$ to $V_{HS} + 14V$
HS Slew Rate	< 50 V/ns
Junction Temperature	-40°C to +125°C

- (1) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed -1V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than $V_{DD} - 15V$. For example, if $V_{DD} = 10V$, the negative transients at HS must not exceed -5V.

Electrical Characteristics

Specifications in standard typeface are for $T_J = +25^\circ\text{C}$, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, $V_{DD} = V_{HB} = 12\text{V}$, $V_{SS} = V_{HS} = 0\text{V}$, No Load on LO or HO.

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Units
SUPPLY CURRENTS						
I_{DD}	V_{DD} Quiescent Current	LI = HI = 0V		0.3	0.6	mA
I_{DDO}	V_{DD} Operating Current	f = 500 kHz		2.1	3.4	mA
I_{HB}	Total HB Quiescent Current	LI = HI = 0V		0.06	0.2	mA
I_{HBO}	Total HB Operating Current	f = 500 kHz		1.6	3.0	mA
I_{HBS}	HB to V_{SS} Current, Quiescent	$V_{HS} = V_{HB} = 100\text{V}$		0.1	10	μA
I_{HBSO}	HB to V_{SS} Current, Operating	f = 500 kHz		0.5		mA
INPUT PINS LI and HI						
V_{IL}	Low Level Input Voltage Threshold		0.8	1.8		V
V_{IH}	High Level Input Voltage Threshold			1.8	2.2	V
R_I	Input Pulldown Resistance		100	180	500	k Ω
UNDER VOLTAGE PROTECTION						
V_{DDR}	V_{DD} Rising Threshold	$V_{DDR} = V_{DD} - V_{SS}$	6.0	6.9	7.4	V
V_{DDH}	V_{DD} Threshold Hysteresis			0.5		V
V_{HBR}	HB Rising Threshold	$V_{HBR} = V_{HB} - V_{HS}$	5.7	6.6	7.1	V
V_{HBH}	HB Threshold Hysteresis			0.4		V
BOOT STRAP DIODE						
V_{DL}	Low-Current Forward Voltage	$I_{VDD-HB} = 100\ \mu\text{A}$ $V_{DL} = V_{DD} - V_{HB}$		0.58	0.9	V
V_{DH}	High-Current Forward Voltage	$I_{VDD-HB} = 100\ \text{mA}$ $V_{DH} = V_{DD} - V_{HB}$		0.82	1.1	V
R_D	Dynamic Resistance	$I_{VDD-HB} = 100\ \text{mA}$		0.8	1.5	Ω
LO GATE DRIVER						
V_{OLL}	Low-Level Output Voltage	$I_{LO} = 100\ \text{mA}$ $V_{OHL} = V_{LO} - V_{SS}$		0.28	0.45	V
V_{OHL}	High-Level Output Voltage	$I_{LO} = -100\ \text{mA}$, $V_{OHL} = V_{DD} - V_{LO}$		0.45	0.75	V
I_{OHL}	Peak Pullup Current	$V_{LO} = 0\text{V}$		1.3		A
I_{OLL}	Peak Pulldown Current	$V_{LO} = 12\text{V}$		1.4		A
HO GATE DRIVER						
V_{OLH}	Low-Level Output Voltage	$I_{HO} = 100\ \text{mA}$ $V_{OLH} = V_{HO} - V_{HS}$		0.28	0.45	V
V_{OHH}	High-Level Output Voltage	$I_{HO} = -100\ \text{mA}$ $V_{OHH} = V_{HB} - V_{HO}$		0.45	0.75	V
I_{OHH}	Peak Pullup Current	$V_{HO} = 0\text{V}$		1.3		A
I_{OLH}	Peak Pulldown Current	$V_{HO} = 12\text{V}$		1.4		A
THERMAL RESISTANCE						
$\theta_{JA}^{(2)}$	Junction to Ambient	SOIC		160		$^\circ\text{C/W}$
		WSON ⁽³⁾		40		

(1) Min and Max limits are 100% production tested at 25°C . Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

(2) The θ_{JA} is not a constant for the package and depends on the printed circuit board design and the operating conditions.

(3) 4 layer board with Cu finished thickness 1.5/1/1/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50mm ground and power planes embedded in PCB. See Application Note AN-1187.

Switching Characteristics

Specifications in standard typeface are for $T_J = +25^\circ\text{C}$, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, $V_{DD} = V_{HB} = 12\text{V}$, $V_{SS} = V_{HS} = 0\text{V}$, No Load on LO or HO.

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Units
LM5100A						
t_{LPHL}	Lower Turn-Off Propagation Delay (LI Falling to LO Falling)			27	56	ns
t_{HPHL}	Upper Turn-Off Propagation Delay (HI Falling to HO Falling)			27	56	ns
t_{LPLH}	Lower Turn-On Propagation Delay (LI Rising to LO Rising)			29	56	ns
t_{HPLH}	Upper Turn-On Propagation Delay (HI Rising to HO Rising)			29	56	ns
t_{MON}	Delay Matching: Lower Turn-On and Upper Turn-Off			2	15	ns
t_{MOFF}	Delay Matching: Lower Turn-Off and Upper Turn-On			2	15	ns
t_{RC}, t_{FC}	Either Output Rise/Fall Time	$C_L = 1000\text{ pF}$		15	-	ns
t_{PW}	Minimum Input Pulse Width that Changes the Output			50		ns
t_{BS}	Bootstrap Diode Turn-Off Time	$I_F = 100\text{ mA}, I_R = 100\text{ mA}$		105		ns

- (1) Min and Max limits are 100% production tested at 25°C . Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

Typical Performance Characteristics

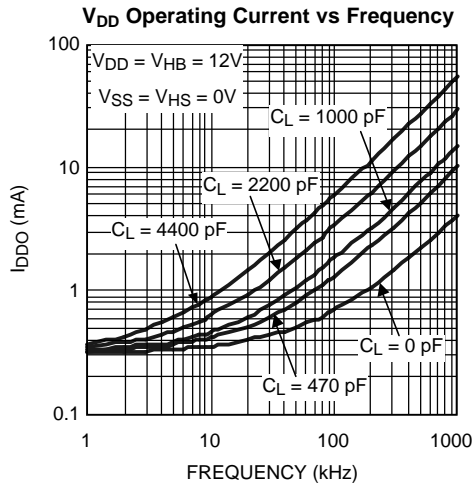


Figure 3.

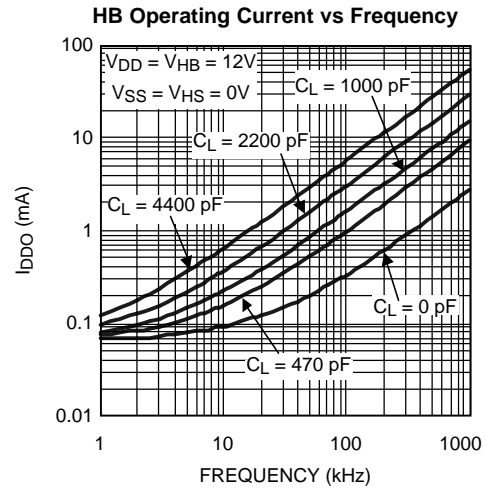


Figure 4.

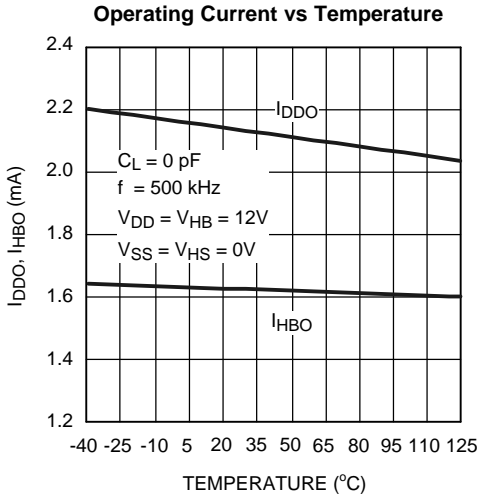


Figure 5.

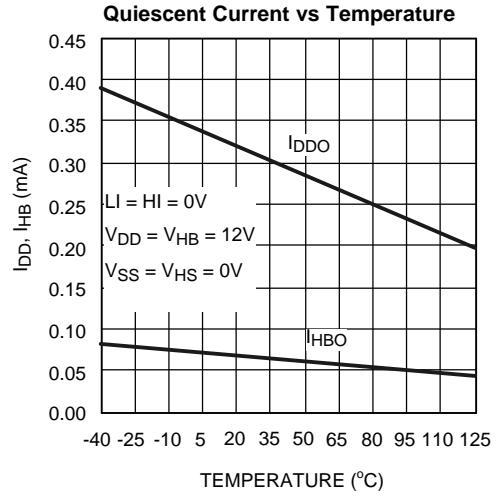


Figure 6.

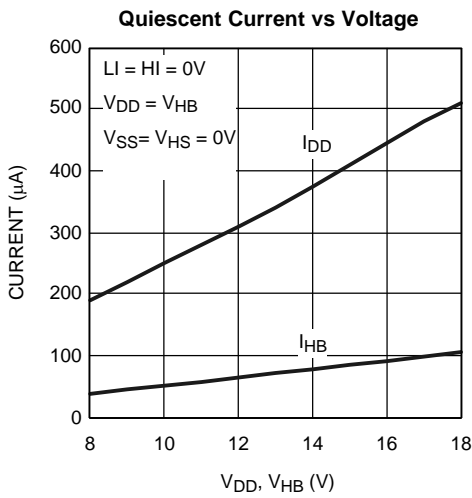


Figure 7.

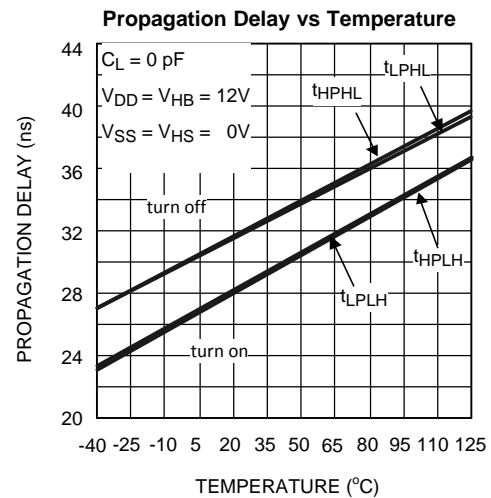


Figure 8.

Typical Performance Characteristics (continued)

LO and HO High Level Output Voltage vs Temperature

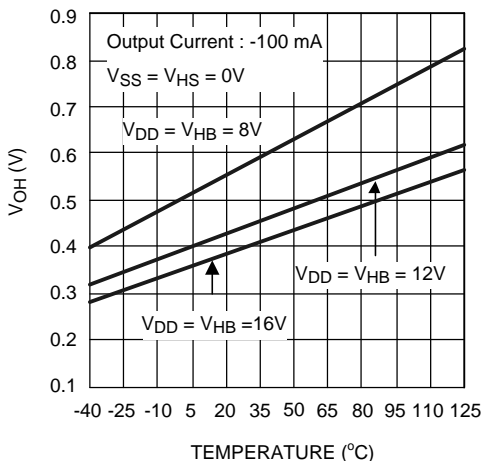


Figure 9.

LO and HO Low Level Output Voltage vs Temperature

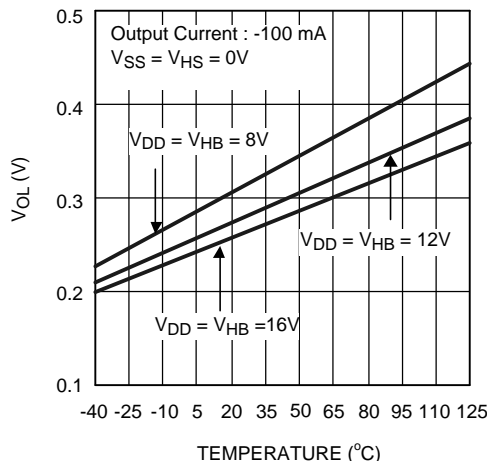


Figure 10.

HO and LO Peak Output Current vs Output Voltage

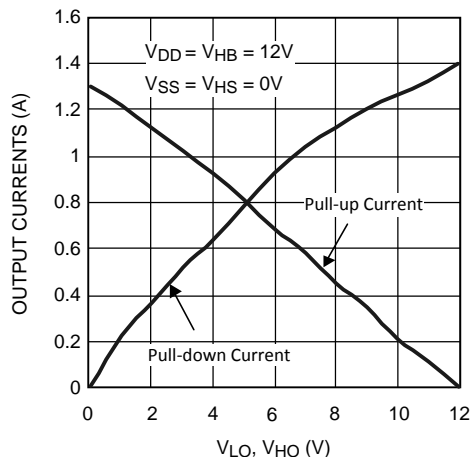


Figure 11.

Diode Forward Voltage

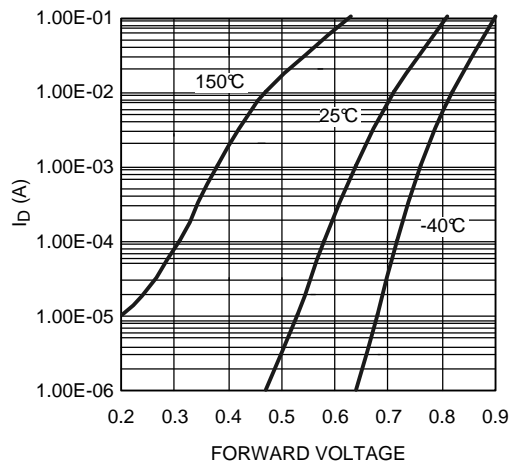


Figure 12.

Undervoltage Rising Thresholds vs Temperature

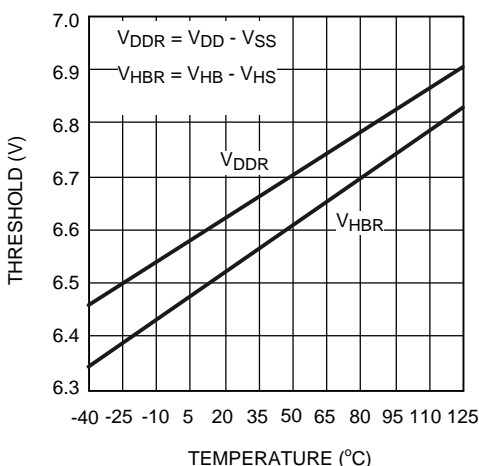


Figure 13.

Undervoltage Hysteresis vs Temperature

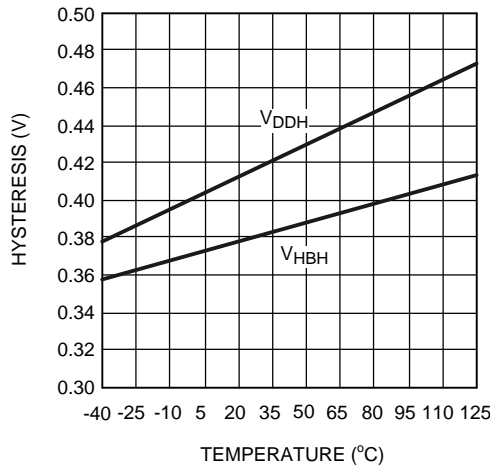
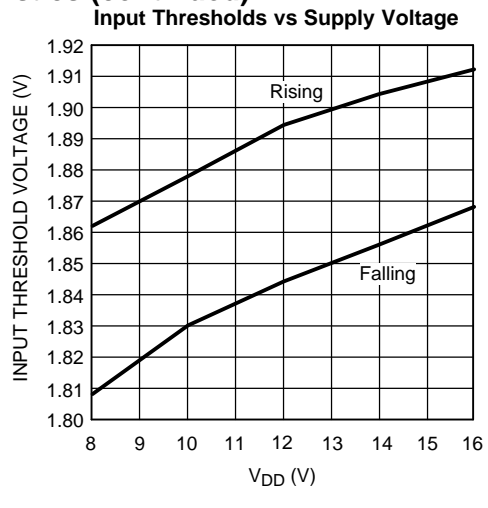
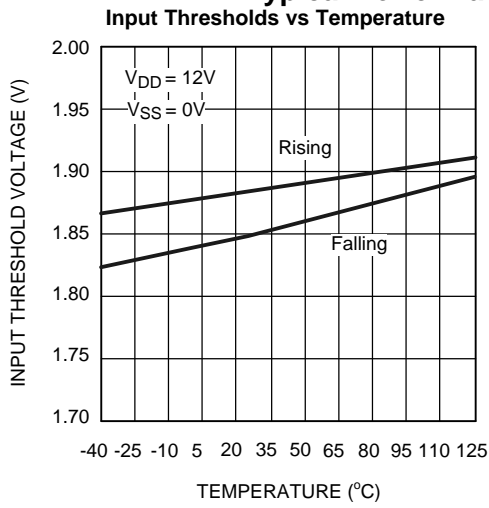


Figure 14.

Typical Performance Characteristics (continued)



Timing Diagram

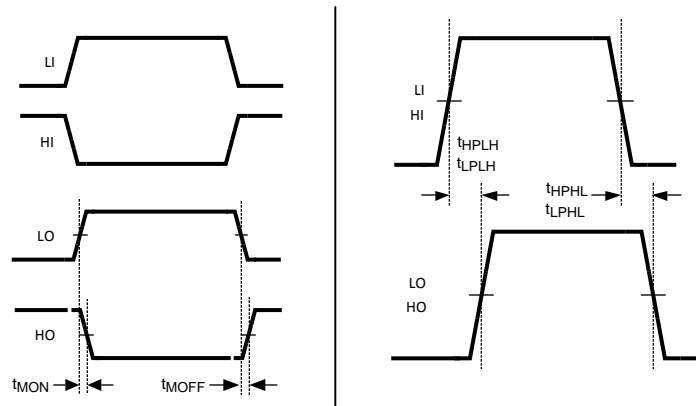


Figure 17.

Layout Considerations

The optimum performance of high and low side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. A low ESR / ESL capacitor must be connected close to the IC, and between V_{DD} and V_{SS} pins and between HB and HS pins to support high peak currents being drawn from VDD during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (V_{SS}).
3. In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding Considerations:
 - The first priority in designing grounding connections is to confine the high peak currents from charging and discharging the MOSFET gate in a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
 - The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low side MOSFET body diode. The bootstrap capacitor is recharged on the cycle-by-cycle basis through the bootstrap diode from the ground referenced V_{DD} bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

HS Transient Voltages Below Ground

The HS node will always be clamped by the body diode of the lower external FET. In some situations, board resistances and inductances can cause the HS node to transiently swing several volts below ground. The HS node can swing below ground provided:

1. HS must always be at a lower potential than HO. Pulling HO more than -0.3V below HS can activate parasitic transistors resulting in excessive current to flow from the HB supply possibly resulting in damage to the IC. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed externally between HO and HS or LO and GND to protect the IC from this type of transient. The diode must be placed as close to the IC pins as possible in order to be effective.
2. HB to HS operating voltage should be 15V or less . Hence, if the HS pin transient voltage is -5V, VDD should be ideally limited to 10V to keep HB to HS below 15V.
3. A low ESR bypass capacitor between HB to HS as well as VDD to VSS is essential for proper operation. The

capacitor should be located at the leads of the IC to minimize series inductance. The peak currents from LO and HO can be quite large. Any series inductances with the bypass capacitor will cause voltage ringing at the leads of the IC which must be avoided for reliable operation.

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
<hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format	<hr/> 9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5107MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5107 MA	Samples
LM5107MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5107 MA	Samples
LM5107SD/NOPB	ACTIVE	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5107SD	Samples
LM5107SDX/NOPB	ACTIVE	WSON	NGT	8		TBD	Call TI	Call TI	-40 to 125	L5107SD	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5107MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5107SD/NOPB	WSO	NGT	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

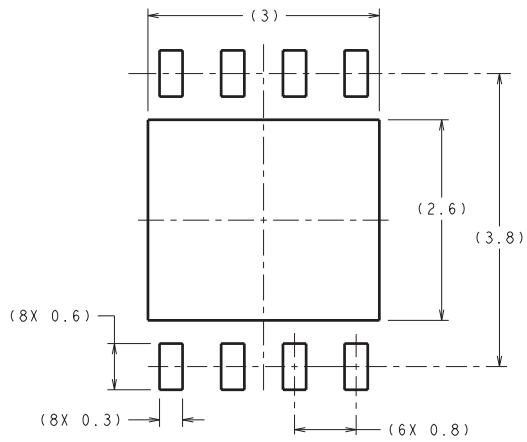
TAPE AND REEL BOX DIMENSIONS



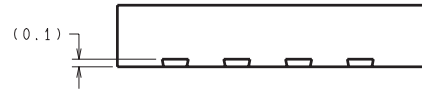
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5107MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5107SD/NOPB	WSON	NGT	8	1000	210.0	185.0	35.0

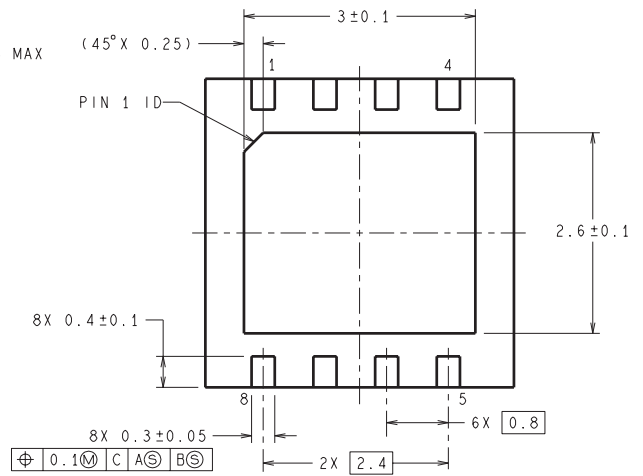
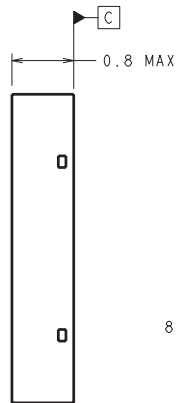
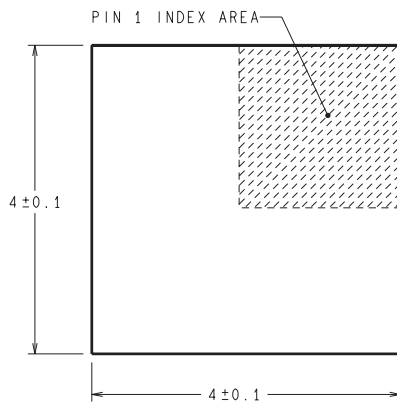
NGT0008A



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



RECOMMENDED LAND PATTERN



SDC08A (Rev A)

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com