262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This M5M5256DFP, VP, RV is a 262144-bit CMOS static RAMs organized as 32768-words by 8-bits which is fabricated using high-performance 3 polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. They are low stand-by current and low voltage operation (3V) and ideal for the battery operation application.

Especially the M5M5256DVP, RV are packaged in a 28-pin thin small outline package. Two types of devices are available, M5M5256DVP (normal lead bend type package) and M5M5256DRV (reverse lead bend type package). Using both type of devices, it becomes very easy to design a printed circuit board.

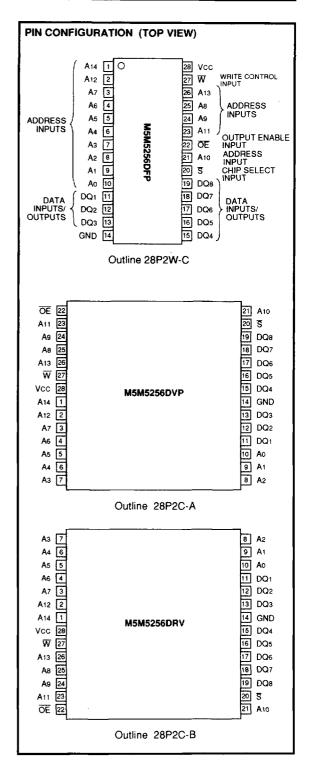
FEATURES

	Access	Power supply current			
Type name	time (max)	Active (max)	stand-by (max)		
M5M5256DFP, VP, RV-10VLL M5M5256DFP, VP, RV-12VLL M5M5256DFP, VP, RV-15VLL	100ns 120ns 150ns	20mA	12μA (Vcc=3.6V)		
M5M5256DFP, VP, RV-10VXL M5M5256DFP, VP, RV-12VXL M5M5256DFP, VP, RV-15VXL	100ns 120ns 150ns	(Vcc=3.6V)	2.4μA (Vcc=3.6V) 0.05μA (Vcc=3V, Typical)		

- ●Single +2.7V~3.6V power supply
- No clocks, No refresh
- Data-hold on +2V power supply
- Directly TTL compatible: All inputs and outputs
- Three-state outputs: OR-tie capability
- Simple memory expansion by S
- OE prevents data contention in the I/O bus
- Common data I/O
- ●Low stand-by current 0.05μA (typ)
- Package M5M5256DVP, RV28pin 8 X 13.4mm² TSOP

APPLICATION

Small capacity memory units





262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

FUNCTION

The operation mode of the M5M5256DFP, VP, RV is determined by a combination of the device control inputs \overline{S} , \overline{W} and \overline{OE} . Each mode is summariezed in the function table.

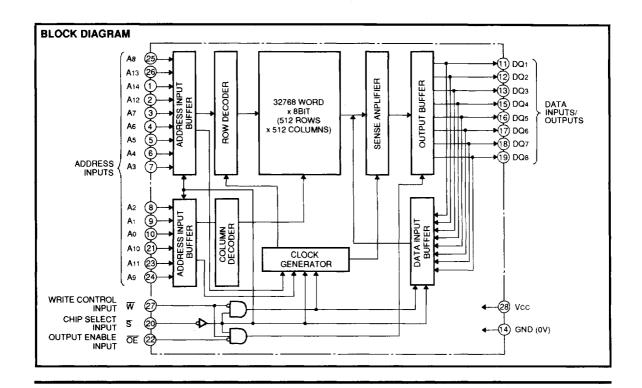
A write cycle is executed whenever the low level \overline{W} overlaps with the low level \overline{S} . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of \overline{W} , \overline{S} , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable \overline{OE} directly controls the output stage. Setting the \overline{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting \overline{W} at a high level and \overline{OE} at a low level while \overline{S} are in an active state.

When setting \overline{S} at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by \overline{S} . The power supply current is reduced as low as the stand-by current which is specified as locs or loc4, and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

S	W	ŌΕ	Mode	DQ	lcc
Τ	X	Х	Non selection	High-impedance	Stand-by
L	L	X	Write	Din	Active
٦	Н	L	Read	Dout	Active
L	Н	Н		High-impedance	Active





262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.3~4.6	V
Vi	Input voltage	With respect to GND	-0.3*~Vcc+0.3 (max. 4.6)	V
Vo	Output voltage		0~Vcc	
Pd	Power dissipation	Ta=25℃	700	mW
Topr	Operating temperature		0~70	·C
Tstg	Storage temperature		-65~150	.c

^{* -3.0}V in case of AC (Pulse width ≤30ns)

DC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=2.7~3.6V, unless otherwise noted)

O	Davameter	Test conditions			Limits		l lmia
Symbol	Parameter	l est condition	S	Min	Тур	Max	Unit
ViH	High-level input voltage					VCC+0.3	٧
VIL	Low-level input voltage			-0.3*		0.6	V
1/	1 tink land a standard	Iон=-0.5mA		2.4			V
Vон	High-level output voltage	rel output voltage		VCC-0.5			V
Vol	Low-level output voltage	IoL=1mA				0.4	٧
lı	Input leakage current	Vi=0~Vcc				±1	μА
lo	Output leakage current	S=ViH or OE=ViH, Vi/0=0~	S=ViH or OE=ViH, Vi/0=0~Vcc			±1	μA
	Active supply current	S≦0.2V Other inputs≦0.2V	Min. cycle		11	20	mA
ICC1	(AC, MOS level) or≧Vcc-0.2V Output open	1MHz		1.5	3		
	Active supply current	S=VIL	Min. cycle		11	20	
ICC2	(AC, TTL level)	Other inputs=VIн or VIL Output open	1MHz		1.5	3	mA
	0	S≧Vcc-0.2V	-VLL			12	μA
ICC3	Stand-by supply current Other inputs=0~Vcc	-VXL		0.05	2.4	μ,	
ICC4	Stand-by supply current	S=VIH, Other inputs=0~Vc	S=VIH, Other inputs=0~Vcc			0.33	mA
Cı	Input capacitance (Ta=25°C)	Vi=GND, Vi=25mVrms, f=	Vi=GND, Vi=25mVrms, f=1MHz			6	pF
Co	Output capacitance (Ta=25°C)	Vo=GND, Vo=25mVrms,	Vo=GND, Vo=25mVrms, f=1MHz			8	pF

* -3.0V in case of AC (Pulse width≤30ns)
Note1: Direction for current flowing into IC is indicated as positive. (no mark)



^{2:} Typical value is 3V, Ta=25°C.

^{3:} Ci, Co are periodically sampled and are not 100% tested.

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

AC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=2.7~3.6V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ViH=2.2V, ViL=0.4V

Input rise and fall time 5ns

Reference level VoH=VoL=1.5V

Transition is measured $\pm 500 mV$ from steady state voltage. (for ten, tdis)

Output loads Fig.1. CL=100pF (-15VLL, -15VXL)

CL=50pF(-12VLL, -12VXL) CL=30pF(-10VLL, -10VXL)

CL=5pF(for ten, tdis)

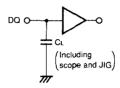


Fig.1 Output load

(2) READ CYCLE

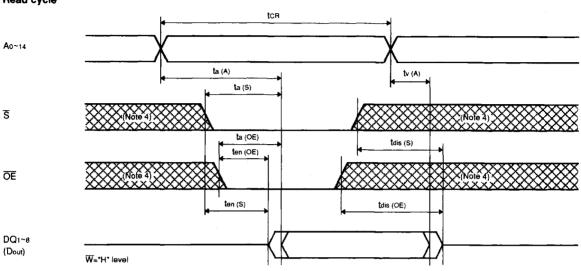
Symbol			Limits						
	Parameter		M5M5256D-10VLL M5M5256D-12VLI M5M5256D-10VXL M5M5256D-12VX				Unit		
		Min	Max	Min	Max	Min	Max		
tcn	Read cycle time	100		120		150		ns	
ta (A)	Address access time		100		120		150	ns	
ta (S)	Chip select access time		100		120		150	ns	
ta (OE)	Output enable access time	,	50		60		75	ns	
tdis (S)	Output disable time after \$\overline{S}\$ high		30		35		40	ns	
tdis (OE)	Output disable time after OE high		30		35		40	ns	
ten (S)	Output enable time after S low	10		10		10		ns	
ten (OE)	Output enable time after OE low	10		10		10		ns	
tv (A)	Data valid time after address	10		10		10		ns	

(3) WRITE CYCLE

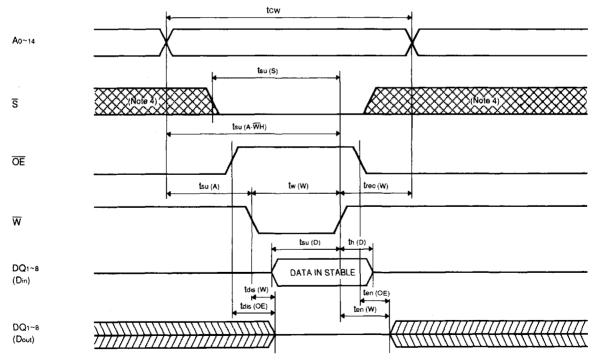
-	Parameter		Limits						
Symbol							M5M5256D-15VLL M5M5256D-15VXL		
		Min	Max	Min	Max	Min	Max	-'	
tcw	Write cycle time	100		120		150		ns	
tw (W)	Write pulse width	70		80		90		ns	
Īsu (A)	Address setup time	0		0		0		ns	
tsu (A-WH)	Address setup time with respect to W high	80		90		100		ns	
tsu (S)	Chip select setup time	80		90	<u> </u>	100		ns	
tsu (D)	Data setup time	40		45		50		ns	
th (D)	Data hold time	0		0	.,	0		ns	
trec (W)	Write recovery time	0		0		0		ns	
tdis (W)	Output disable time after W low		30		35		40	ns	
tdis (OE)	Output disable time after OE high		30		35		40	ns	
ten (W)	Output enable time after W high	10	1	10		10		ns	
ten (OE)	Output enable time after OE low	10		10		10		ns	

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

(4) TIMING DIAGRAMS Read cycle



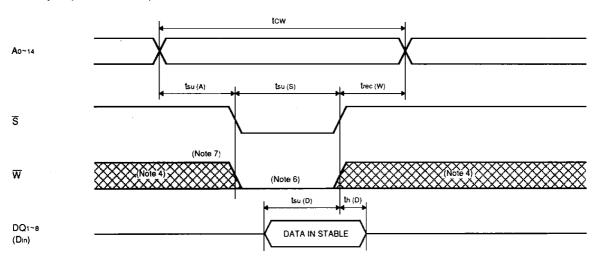
Write cycle (W control mode)





262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

Write cycle (\$\overline{S}\$ control mode)



Note 4: Hatching indicates the state is don't care.

- 5: Writing is executed in overlap of \overline{S} and \overline{W} low.
- 6: If W goes low simultaneously with or prior to S, the output remains in the high-impedance state.
- 7: Don't apply inverted phase signal externally when DQ pin is in output mode.
- 8: ten, this are periodically sampled and are not 100% tested.

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			L Amile	
Symbol	ratameter	Test conditions	Min	Тур	Max	Unit	
VCC (PD)	Power down supply voltage			2			٧
Vı (Š)	Chip select input S		_	2			٧
loo (no)	Development and the second	Vcc=3V	-VLL			10*	μА
ICC (PD)	Power down supply current	Other inputs=3V	-VXL		0.05	2**	μА

* Ta=25°C, loc (PD)=1µA

* * Ta=25°C, Icc (PD)=0.2μA

(2) TIMING REQUIREMENTS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions		11.		
			Min	Тур	Max	Unit
tsu (PD)	Power down set up time		0			ns
trec (PD)	Power down recovery time		tcr			ns

(3) POWER DOWN CHARACTERISTICS

Vcc tsu (PD) 2.7V trec (PD) 2.2V S≥Vcc-0.2V