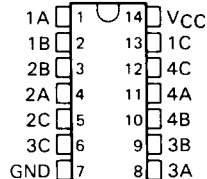


TLC4066M, TLC4066I SILICON-GATE CMOS QUADRUPLE BILATERAL ANALOG SWITCH

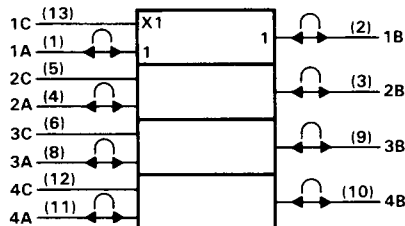
D2922, JANUARY 1986—REVISED OCTOBER 1988

- High Degree of Linearity
- High On-Off Output Voltage Ratio
- Low Crosstalk Between Switches
- Low On-State Impedance . . . 30 Ω Typ at $V_{CC} = 12\text{ V}$
- Individual Switch Controls
- Extremely Low Input Current
- Functionally Interchangeable with National Semiconductor MM54/74HC4066, Motorola MC54/74HC4066, and RCA CD4066A

TLC4066M . . . J OR N PACKAGE
TLC4066I . . . D OR N PACKAGE
(TOP VIEW)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

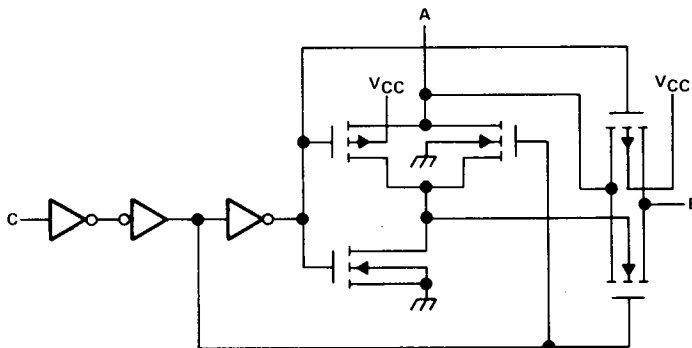
The TLC4066 is a silicon-gate CMOS quadruple analog switch designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 12 V peak to be transmitted in either direction.

Each switch section has its own enable input control. A high-level voltage applied to this control terminal turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

The TLC4066M is characterized for operation from -55°C to 125°C . The TLC4066I is characterized from -40°C to 85°C .

logic diagram (positive logic)



PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

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TLC4066M, TLC4066I

SILICON-GATE CMOS QUADRUPLE BILATERAL ANALOG SWITCH

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range (see Note 1)	-0.5 V to 15 V
Control-input diode current ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
I/O port diode current ($V_I < 0$ or $V_{I/O} > V_{CC}$)	± 20 mA
On-state switch current ($V_{I/O} = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Continuous total dissipation	see Dissipation Rating Table
Operating free-air temperature: TLC4066M	-55°C to 125°C
TLC4066I	-40°C to 85°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

NOTE 1: All voltages are with respect to ground unless otherwise specified.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	N/A
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		2 [†]	5	12	V
I/O port voltage, $V_{I/O}$		0		V_{CC}	V
High-level input voltage, V_{IH}	$V_{CC} = 2$ V	1.5		V_{CC}	V
	$V_{CC} = 4.5$ V	3.15		V_{CC}	
	$V_{CC} = 9$ V	6.3		V_{CC}	
	$V_{CC} = 12$ V	8.4		V_{CC}	
Low-level input voltage, V_{IL}	$V_{CC} = 2$ V	0		0.3	V
	$V_{CC} = 4.5$ V	0		0.9	
	$V_{CC} = 9$ V	0		1.8	
	$V_{CC} = 12$ V	0		2.4	
Input rise time, t_r	$V_{CC} = 2$ V			1000	ns
	$V_{CC} = 4.5$ V			500	
	$V_{CC} = 9$ V			400	
Input fall time, t_f	$V_{CC} = 2$ V			1000	ns
	$V_{CC} = 4.5$ V			500	
	$V_{CC} = 9$ V			400	
Operating free-air temperature, T_A	TLC4066M	-55		125	°C
	TLC4066I	-40		85	

[†]With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.



TLC4066M, TLC4066I SILICON-GATE CMOS QUADRUPLE BILATERAL ANALOG SWITCH

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	TLC4066M			TLC4066I			UNIT
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
r _{son} On-state switch resistance	I _S = 1 mA, V _A = 0 to V _{CC} , See Figure 1	4.5 V		100	220		100	200	Ω
		9 V		50	110		50	105	
		12 V		30	90		30	85	
	I _S = 1 mA, V _A = 0 or V _{CC} , See Figure 1	2 V		120	240		120	215	
		4.5 V		50	120		50	100	
		9 V		35	80		35	75	
On-state switch resistance matching	V _A = 0 to V _{CC} , See Figure 1	12 V		20	70		20	60	
		4.5 V		10	20		10	20	
		9 V		5	15		5	15	
I _I Control input current	V _I = 0 or V _{CC}	2 V						μA	
		or			± 1		± 1		
		6 V							
I _{soff} Off-state switch leakage current	V _S = ±V _{CC} , See Figure 2	5.5 V		± 10	± 600		± 10	± 600	nA
		9 V		± 15	± 800		± 15	± 800	
		12 V		± 20	± 1000		± 20	± 1000	
I _{son} On-state switch leakage current	V _A = 0 or V _{CC} , See Figure 3	5.5 V		± 10	± 150		± 10	± 150	nA
		9 V		± 15	± 200		± 15	± 200	
		12 V		± 20	± 300		± 20	± 300	
I _{CC} Supply current	V _I = 0 or V _{CC} , I _O = 0	5.5 V		2	40		2	20	μA
		9 V		8	160		8	80	
		12 V		16	320		16	160	
C _i Input capacitance	A or B	2 V to 12 V		15			15		pF
	C			5 10			5 10		
C _f Feedthrough capacitance	A to B	2 V to 12 V		5			5		pF

[†]All typical values are at T_A = 25°C.

TLC4066M, TLC4066I

SILICON-GATE CMOS QUADRUPLE BILATERAL ANALOG SWITCH

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	TLC4066M			TLC4066I			UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX		
t_{pd}	Propagation delay time, A to B or B to A See Figure 4	2 V	25 75			15 30			ns	
			4.5 V	5 15			5 13			
				9 V			4 12			
				12 V			3 13			
t_{on}	Switch turn-on time $R_L = 1$ k Ω , See Figures 5 and 6	2 V	32 150			32 125			ns	
			4.5 V	8 30			8 25			
				9 V			6 18			
				12 V			5 15			
t_{off}	Switch turn-off time $R_L = 1$ k Ω , See Figures 5 and 6	2 V	45 252			45 210			ns	
			4.5 V	15 54			15 45			
				9 V			10 48			
				12 V			8 45			
f_{co}	Switch cutoff frequency (channel loss = 3 dB)	4.5 V	100			100			MHz	
			9 V			120				
$V_{OCF(PP)}$	Control feedthrough voltage to any switch, peak to peak See Figure 7	4.5 V	350			350			mV	
	Frequency at which crosstalk attenuation between any two switches equals 50 dB See Figure 8	4.5 V	1			1			MHz	

†All typical values are at $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

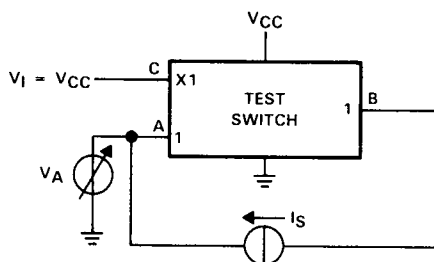
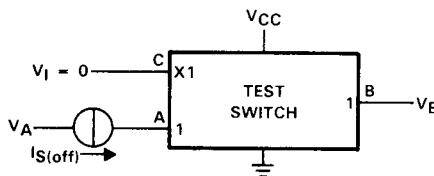


FIGURE 1. TEST CIRCUIT FOR ON-STATE RESISTANCE



$V_S = V_A - V_B$
 CONDITION 1: $V_A = 0, V_B = V_{CC}$
 CONDITION 2: $V_A = V_{CC}, V_B = 0$

FIGURE 2. TEST CIRCUIT FOR OFF-STATE SWITCH LEAKAGE CURRENT

PARAMETER MEASUREMENT INFORMATION

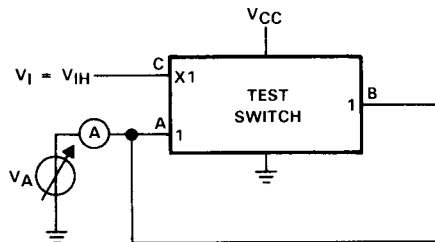
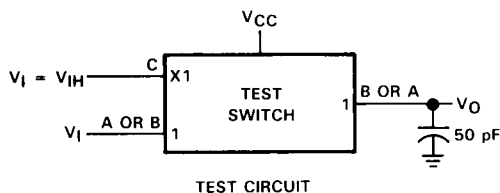
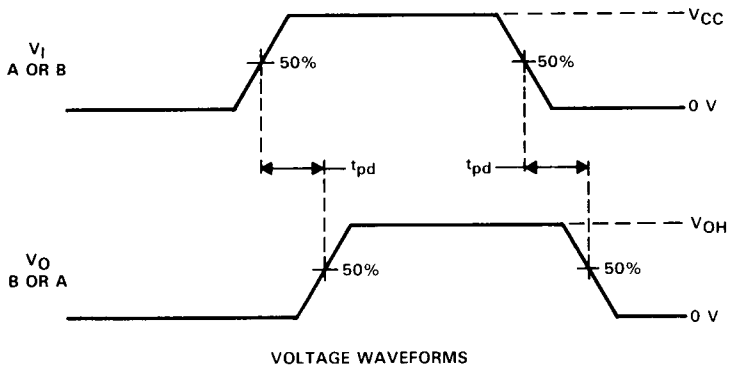


FIGURE 3. TEST CIRCUIT FOR ON-STATE SWITCH LEAKAGE CURRENT



TEST CIRCUIT

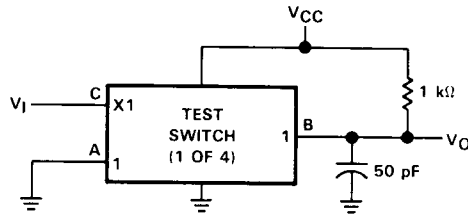


VOLTAGE WAVEFORMS

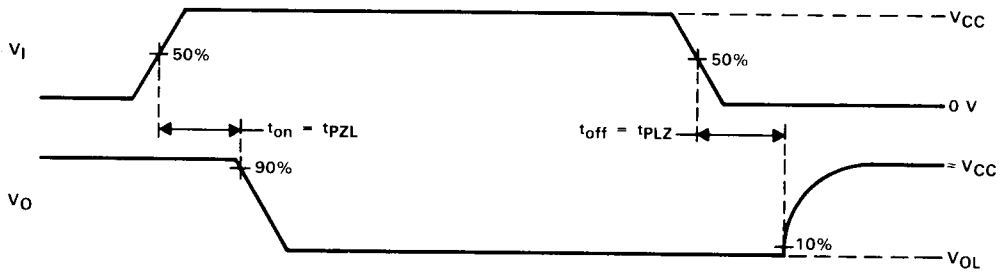
FIGURE 4. PROPAGATION DELAY TIME, SIGNAL INPUT TO SIGNAL OUTPUT

TLC4066M, TLC4066I
SILICON-GATE CMOS QUADRUPLE BILATERAL ANALOG SWITCH

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 5. SWITCHING TIME (t_{pZL} , t_{pLZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION

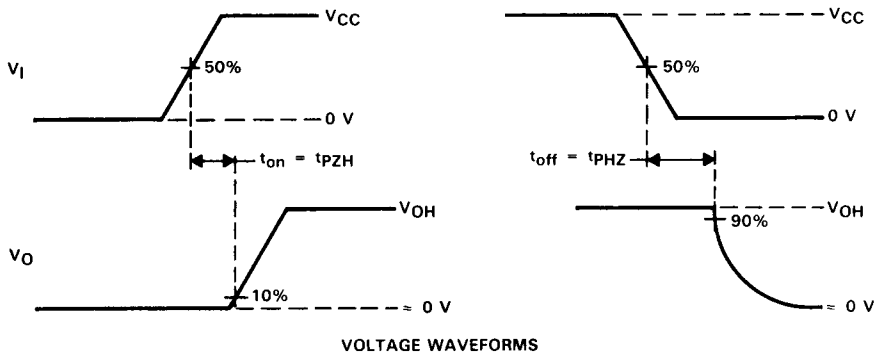
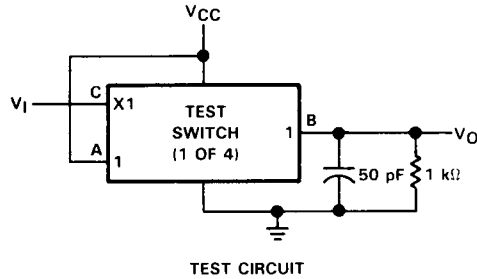


FIGURE 6. SWITCHING TIME (t_{PZH} , t_{PHZ}), CONTROL TO SIGNAL OUTPUT

TLC4066M, TLC4066I
SILICON-GATE CMOS QUADRUPLE BILATERAL ANALOG SWITCH

PARAMETER MEASUREMENT INFORMATION

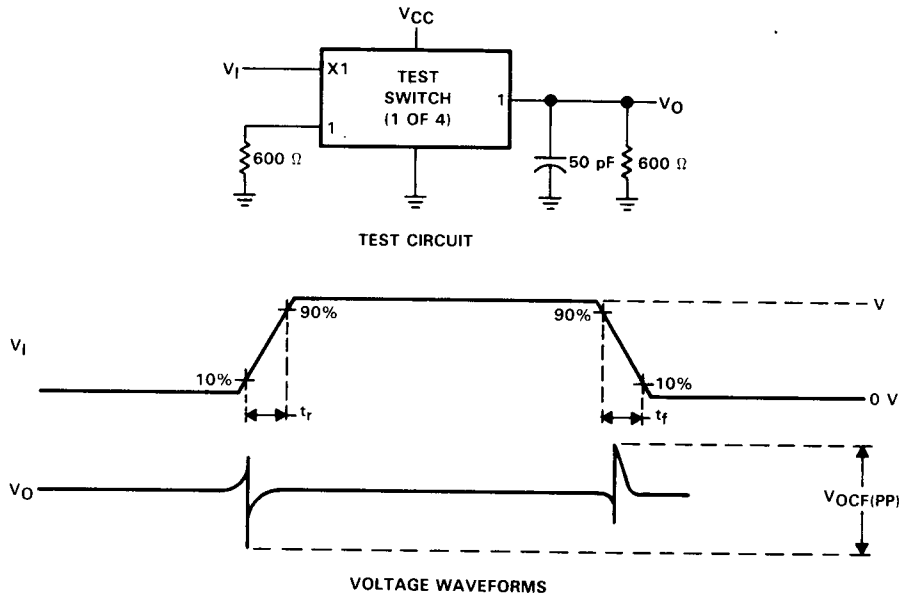


FIGURE 7. CONTROL FEEDTHROUGH VOLTAGE

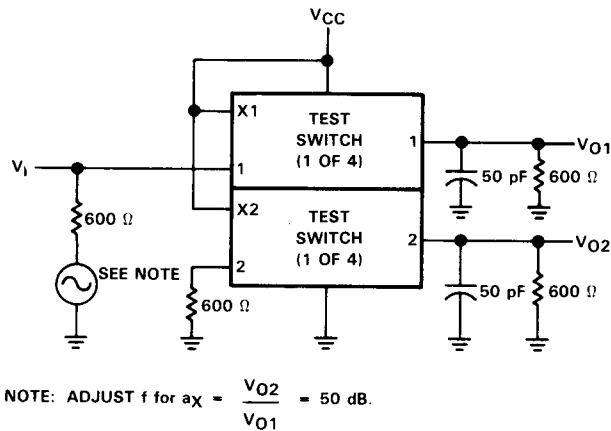


FIGURE 8. CROSSTALK BETWEEN ANY TWO SWITCHES, TEST CIRCUIT