



# Low-Power, Precision SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

## FEATURES

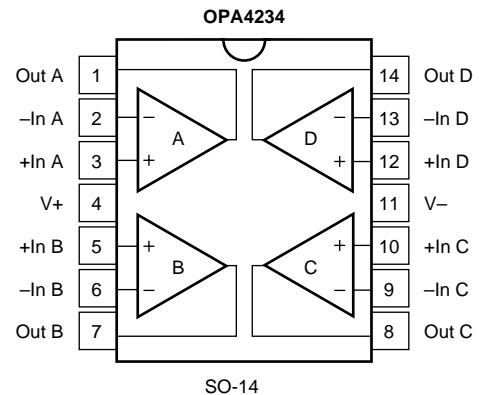
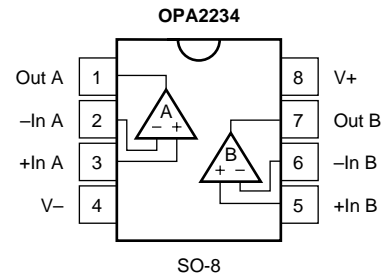
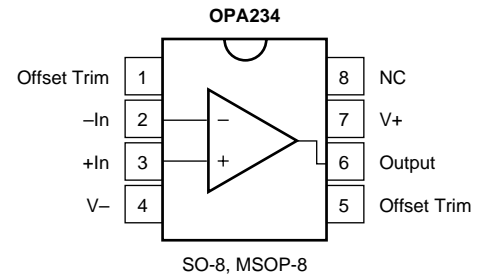
- **WIDE SUPPLY RANGE:**  
Single Supply:  $V_S = +2.7V$  to  $+36V$   
Dual Supply:  $V_S = \pm 1.35V$  to  $\pm 18V$
- **SPECIFIED PERFORMANCE:**  
 $+2.7V$ ,  $+5V$ , and  $\pm 15V$
- **LOW QUIESCENT CURRENT:**  $250\mu A/\text{amp}$
- **LOW INPUT BIAS CURRENT:**  $25nA$  max
- **LOW OFFSET VOLTAGE:**  $100\mu V$  max
- **HIGH CMRR, PSRR, and  $A_{OL}$**
- **SINGLE, DUAL, and QUAD VERSIONS**

## DESCRIPTION

The OPA234 series low-cost op amps are ideal for single-supply, low-voltage, low-power applications. The series provides lower quiescent current than older "1013"-type products and comes in current industry-standard packages and pinouts. The combination of low offset voltage, high common-mode rejection, high power-supply rejection, and a wide supply range provides excellent accuracy and versatility. Single, dual, and quad versions have identical specifications for maximum design flexibility. These general-purpose op amps are ideal for portable and battery-powered applications.

The OPA234 series op amps operate from either single or dual supplies. In single-supply operation, the input common-mode range extends below ground and the output can swing to within 50mV of ground. Excellent phase margin makes the OPA234 series ideal for demanding applications, including high load capacitance. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

Single version packages are in an SO-8 surface-mount and a space-saving MSOP-8 surface-mount. Dual packages are in an SO-8 surface-mount. Quad packages are in an SO-14 surface-mount. All are specified for  $-40^\circ C$  to  $+85^\circ C$  operation.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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# ELECTRICAL CHARACTERISTICS: $V_S = +5V$

At  $T_A = 25^\circ C$ ,  $V_S = +5V$ ,  $R_L = 10k\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.

PARAMETER	CONDITION	OPA234U, E OPA2234U			OPA234UA, EA OPA2234UA OPA4234UA, U			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b> Input Offset Voltage OPA234E, EA vs Temperature <sup>(1)</sup> vs Power Supply vs Time Channel Separation (Dual, Quad)	$V_{OS}$  $dV_{OS}/dT$ PSRR $V_{CM} = 2.5V$ Operating Temperature Range $V_S = +2.7V$ to $+30V$ , $V_{CM} = 1.7V$		$\pm 40$ $\pm 100$ $\pm 0.5$ 3 0.2 0.3	$\pm 100$ $\pm 150$ $\pm 3$ 10		*	$\pm 250$ $\pm 350$ *	$\mu V$ $\mu V$ $\mu V/^\circ C$ $\mu V/V$ $\mu V/mo$ $\mu V/V$
<b>INPUT BIAS CURRENT</b> Input Bias Current <sup>(2)</sup> Input Offset Current	$I_B$ $I_{OS}$ $V_{CM} = 2.5V$ $V_{CM} = 2.5V$		-15 $\pm 1$	-30 $\pm 5$		*	-50 *	nA nA
<b>NOISE</b> Input Voltage Noise Density Current Noise Density	$f = 1kHz$ $v_n$ $i_n$		25 80			*	*	$nV/\sqrt{Hz}$ $fA/\sqrt{Hz}$
<b>INPUT VOLTAGE RANGE</b> Common-Mode Voltage Range Common-Mode Rejection	CMRR $V_{CM} = -0.1V$ to $4V$	-0.1 91	106	(V+) -1	* 86	*	*	V dB
<b>INPUT IMPEDANCE</b> Differential Common-Mode	$V_{CM} = 2.5V$		$10^7 \parallel 5$ $10^{10} \parallel 6$			*	*	$\Omega \parallel pF$ $\Omega \parallel pF$
<b>OPEN-LOOP GAIN</b> Open-Loop Voltage Gain	$A_{OL}$ $V_O = 0.25V$ to $4V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	108 86	120 96		100 *	*	*	dB dB
<b>FREQUENCY RESPONSE</b> Gain-Bandwidth Product Slew Rate Settling Time: 0.1% 0.01% Overload Recovery Time	GBW SR $C_L = 100pF$ $G = 1$ , 3V Step, $C_L = 100pF$ $G = 1$ , 3V Step, $C_L = 100pF$ ( $V_{IN}$ ) (Gain) = $V_S$		0.35 0.2 15 25 16			*	*	MHz $V/\mu s$ $\mu s$ $\mu s$ $\mu s$
<b>OUTPUT</b> Voltage Output: Positive Negative Positive Negative Short-Circuit Current Capacitive Load Drive (Stable Operation) <sup>(3)</sup>	$I_{SC}$ $G = +1$ $R_L = 10k\Omega$ to $V_S/2$ $R_L = 10k\Omega$ to $V_S/2$ $R_L = 10k\Omega$ to Ground $R_L = 10k\Omega$ to Ground	(V+) -1 0.25 (V+) -1 0.1	(V+) -0.65 0.05 (V+) -0.65 0.05 $\pm 11$ 1000		*	*	*	V V V V mA pF
<b>POWER SUPPLY</b> Specified Operating Voltage Operating Voltage Range Quiescent Current (per amplifier)	$I_Q$ $I_O = 0$	+2.7	+5 250	+36 300	*	*	*	V V $\mu A$
<b>TEMPERATURE RANGE</b> Specified Range Operating Range Storage Thermal Resistance 8-Pin DIP SO-8 Surface-Mount MSOP-8 Surface-Mount 14-Pin DIP SO-14 Surface-Mount	$\theta_{JA}$	-40 -40 -55		+85 +125 +125	*	*	*	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$

\* Specifications same as OPA234U, E.

NOTES: (1) Wafer-level tested to 95% confidence level. (2) Positive conventional current flows into the input terminals. (3) See *Small-Signal Overshoot vs Load Capacitance* typical curve.

# ELECTRICAL CHARACTERISTICS: $V_S = +2.7V$

At  $T_A = 25^\circ C$ ,  $V_S = +2.7V$ ,  $R_L = 10k\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.

PARAMETER	CONDITION	OPA234U, E OPA2234U			OPA234UA, EA OPA2234UA OPA4234UA, U			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b>								
Input Offset Voltage OPA234E, EA	$V_{OS}$		$\pm 40$	$\pm 100$		*	$\pm 250$	$\mu V$
vs Temperature <sup>(1)</sup>	$dV_{OS}/dT$		$\pm 100$	$\pm 150$		*	$\pm 350$	$\mu V$
vs Power Supply	PSRR		$\pm 0.5$	$\pm 3$		*	*	$\mu V/^\circ C$
vs Time			3	10		*	20	$\mu V/V$
Channel Separation (Dual, Quad)			0.2			*		$\mu V/mo$
			0.3			*		$\mu V/V$
<b>INPUT BIAS CURRENT</b>								
Input Bias Current <sup>(2)</sup>	$I_B$	$V_{CM} = 1.35V$	-15	-30		*	-50	nA
Input Offset Current	$I_{OS}$	$V_{CM} = 1.35V$	$\pm 1$	$\pm 5$		*	*	n
<b>NOISE</b>		$f = 1kHz$						
Input Voltage Noise Density	$V_n$		25			*		$nV/\sqrt{Hz}$
Current Noise Density	$i_n$		80			*		$fA/\sqrt{Hz}$
<b>INPUT VOLTAGE RANGE</b>								
Common-Mode Voltage Range			-0.1		$(V+) - 1$	*	*	V
Common-Mode Rejection	CMRR	$V_{CM} = -0.1V$ to $1.7V$	91	106		*	*	dB
<b>INPUT IMPEDANCE</b>								
Differential		$V_{CM} = 1.35V$		$10^7 \parallel 5$		*		$\Omega \parallel pF$
Common-Mode				$10^{10} \parallel 6$		*		$\Omega \parallel pF$
<b>OPEN-LOOP GAIN</b>								
Open-Loop Voltage Gain	$A_{OL}$	$V_O = 0.25V$ to $1.7V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	108 86	125 96		100 86	*	dB dB
<b>FREQUENCY RESPONSE</b>								
Gain-Bandwidth Product	GBW	$C_L = 100pF$		0.35			*	MHz
Slew Rate	SR			0.2			*	$V/\mu s$
Settling Time: 0.1%		$G = 1$ , 1V Step, $C_L = 100pF$		6			*	$\mu s$
0.01%		$G = 1$ , 1V Step, $C_L = 100pF$		16			*	$\mu s$
Overload Recovery Time		$(V_{IN})$ (Gain) = $V_S$		8			*	$\mu s$
<b>OUTPUT</b>								
Voltage Output: Positive		$R_L = 10k\Omega$ to $V_S/2$	$(V+) - 1$	$(V+) - 0.6$		*	*	V
Negative		$R_L = 10k\Omega$ to $V_S/2$	0.25	0.05		*	*	V
Positive		$R_L = 10k\Omega$ to Ground	$(V+) - 1$	$(V+) - 0.65$		*	*	V
Negative		$R_L = 10k\Omega$ to Ground	0.1	0.05		*	*	V
Short-Circuit Current	$I_{SC}$			$\pm 8$		*	*	mA
Capacitive Load Drive (Stable Operation) <sup>(3)</sup>		$G = +1$		1000		*	*	pF
<b>POWER SUPPLY</b>								
Specified Operating Voltage			+2.7	+2.7		*	*	V
Operating Voltage Range				+36		*	*	V
Quiescent Current (per amplifier)	$I_Q$	$I_O = 0$		250		300	*	$\mu A$
<b>TEMPERATURE RANGE</b>								
Specified Range			-40		+85	*	*	$^\circ C$
Operating Range			-40		+125	*	*	$^\circ C$
Storage			-55		+125	*	*	$^\circ C$
Thermal Resistance	$\theta_{JA}$							
8-Pin DIP				100			*	$^\circ C/W$
SO-8 Surface-Mount				150			*	$^\circ C/W$
MSOP-8 Surface-Mount				220			*	$^\circ C/W$
14-Pin DIP				80			*	$^\circ C/W$
SO-14 Surface-Mount				110			*	$^\circ C/W$

\* Specifications same as OPA234U, E.

NOTES: (1) Wafer-level tested to 95% confidence level. (2) Positive conventional current flows into the input terminals. (3) See *Small-Signal Overshoot vs Load Capacitance* typical curve.

# ELECTRICAL CHARACTERISTICS: $V_S = \pm 15V$

At  $T_A = 25^\circ C$ ,  $V_S = \pm 15V$ , and  $R_L = 10k\Omega$  connected to ground, unless otherwise noted.

PARAMETER	CONDITION	OPA234U, E OPA2234U			OPA234UA, EA OPA2234UA OPA4234UA, U			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
<b>OFFSET VOLTAGE</b> Input Offset Voltage OPA4234U Model vs Temperature <sup>(1)</sup> vs Power Supply vs Time Channel Separation (Dual, Quad)	$V_{OS}$  $dV_{OS}/dT$ $PSRR$	$V_{CM} = 0V$  Operating Temperature Range $V_S = \pm 1.35V$ to $\pm 18V$ , $V_{CM} = 0V$		$\pm 70$ $\pm 0.5$ 3 0.2 0.3	$\pm 250$ $\pm 5$ 10		* $\pm 70$ * * *	$\pm 500$ $\pm 250$ * 20	$\mu V$ $\mu V$ $\mu V/^\circ C$ $\mu V/V$ $\mu V/mo$ $\mu V/V$
<b>INPUT BIAS CURRENT</b> Input Bias Current <sup>(2)</sup> Input Offset Current	$I_B$ $I_{OS}$	$V_{CM} = 0V$ $V_{CM} = 0V$		-12 $\pm 1$	-25 $\pm 5$		* *	-50 *	nA nA
<b>NOISE</b> Input Voltage Noise Density Current Noise Density	$V_n$ $i_n$	$f = 1kHz$		25 80			* *		$nV/\sqrt{Hz}$ $fA/\sqrt{Hz}$
<b>INPUT VOLTAGE RANGE</b> Common-Mode Voltage Range Common-Mode Rejection	CMRR	$V_{CM} = -15V$ to $14V$	(V-) 91	106	(V+) -1	* 86	* *	* *	V dB
<b>INPUT IMPEDANCE</b> Differential Common-Mode		$V_{CM} = 0V$		$10^7 \parallel 5$ $10^{10} \parallel 6$			* *		$\Omega \parallel pF$ $\Omega \parallel pF$
<b>OPEN-LOOP GAIN</b> Open-Loop Voltage Gain	$A_{OL}$	$V_O = -14.5V$ to $14V$	110	120		100	*		dB
<b>FREQUENCY RESPONSE</b> Gain-Bandwidth Product Slew Rate Settling Time: 0.1% 0.01% Overload Recovery Time	GBW SR	$C_L = 100pF$  $G = 1$ , 10V Step, $C_L = 100pF$ $G = 1$ , 10V Step, $C_L = 100pF$ ( $V_{IN}$ ) (Gain) = $V_S$		0.35 0.2 41 47 22			* * * * *		MHz V/ $\mu s$ $\mu s$ $\mu s$ $\mu s$
<b>OUTPUT</b> Voltage Output: Positive Negative Short-Circuit Current Capacitive Load Drive (Stable Operation) <sup>(3)</sup>	$I_{SC}$	$G = +1$	(V+) -1 (V-) +0.5	(V+) -0.7 (V-) +0.15 $\pm 22$ 1000		* *	* * * *		V V mA pF
<b>POWER SUPPLY</b> Specified Operating Voltage Operating Voltage Range Quiescent Current (per amplifier)	$I_Q$	$I_O = 0$	$\pm 1.35$	$\pm 15$ $\pm 275$	$\pm 18$ $\pm 350$	* *	* *	* *	V V $\mu A$
<b>TEMPERATURE RANGE</b> Specified Range Operating Range Storage Thermal Resistance 8-Pin DIP SO-8 Surface-Mount MSOP-8 Surface-Mount 14-Pin DIP SO-14 Surface-Mount	$\theta_{JA}$		-40 -40 -55		+85 +125 +125	* * *	* * *	* * *	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$

\* Specifications same as OPA234U, E.

NOTES: (1) Wafer-level tested to 95% confidence level. (2) Positive conventional current flows into the input terminals. (3) See *Small-Signal Overshoot vs Load Capacitance* typical curve.



# ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE MARKING
<b>Single</b> OPA234EA OPA234E OPA234UA OPA234U	MSOP-8 Surface-Mount " SO-8 Surface-Mount "	A34 " OPA234UA OPA234U
<b>Dual</b> OPA2234UA OPA2234U	SO-8 Surface-Mount "	OPA2234UA OPA2234U
<b>Quad</b> OPA4234UA OPA4234U	SO-8 Surface-Mount "	OPA4234UA OPA4234U

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

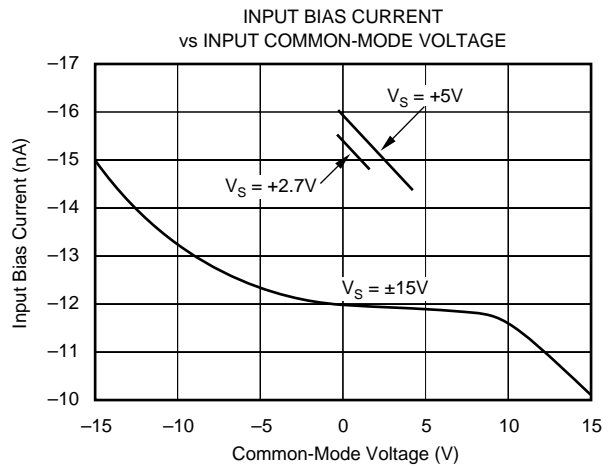
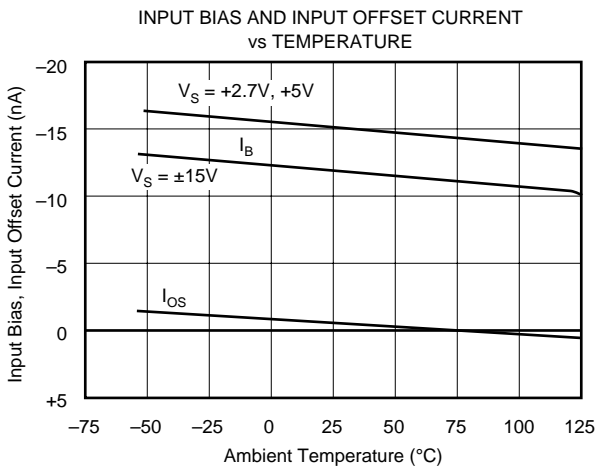
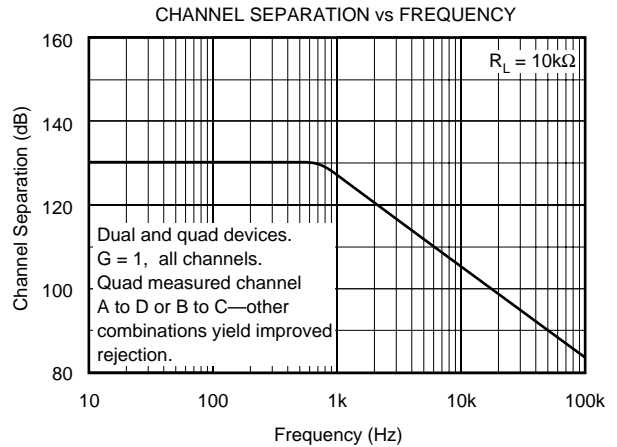
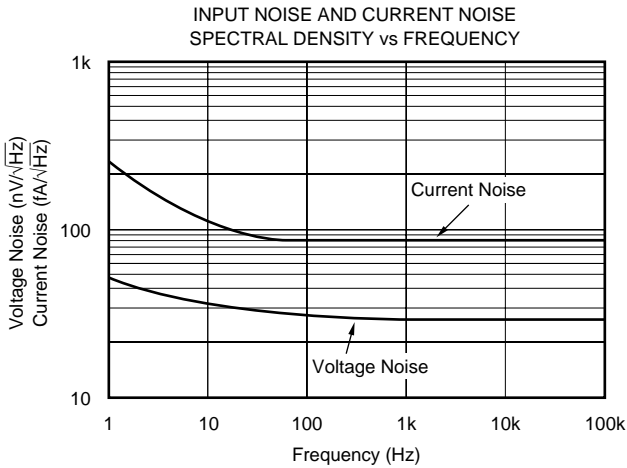
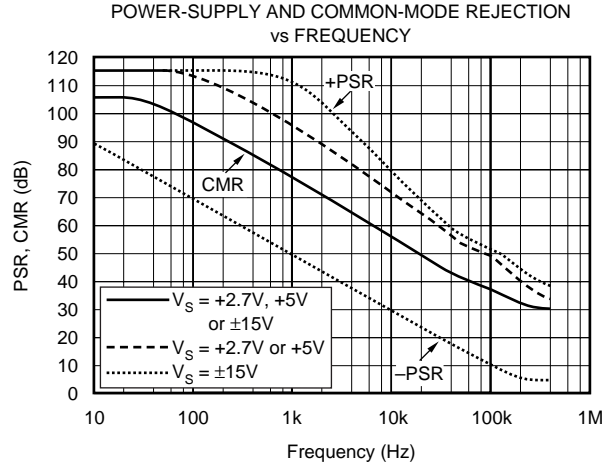
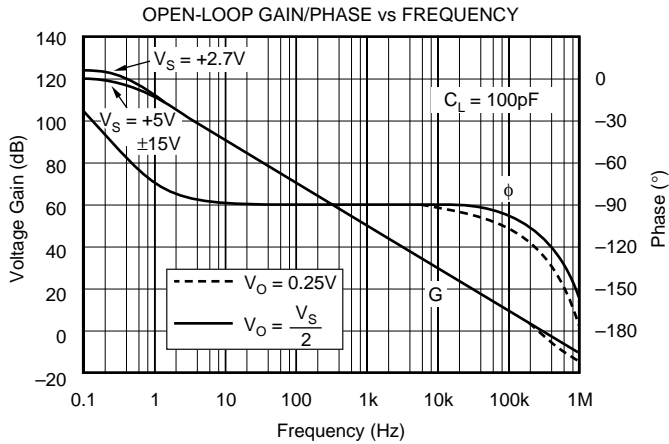
## ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V- .....	36V
Input Voltage .....	(V-) -0.7V to (V+) +0.7V
Output Short-Circuit <sup>(1)</sup> .....	Continuous
Operating Temperature .....	-40°C to +125°C
Storage Temperature .....	-55°C to +125°C
Junction Temperature .....	150°C
Lead Temperature (soldering, 10s) .....	300°C

NOTE: (1) Short-circuit to ground, one amplifier per package.

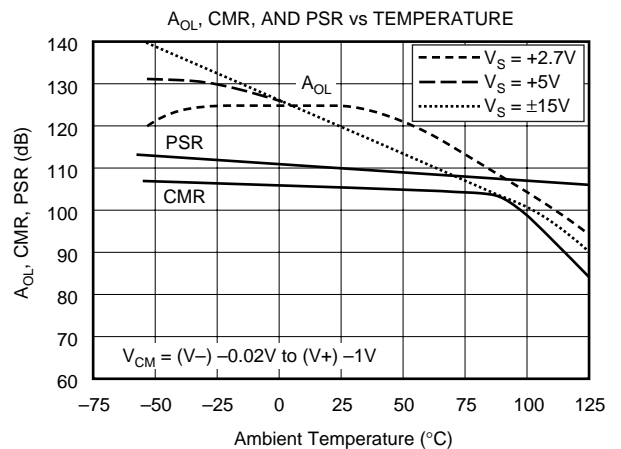
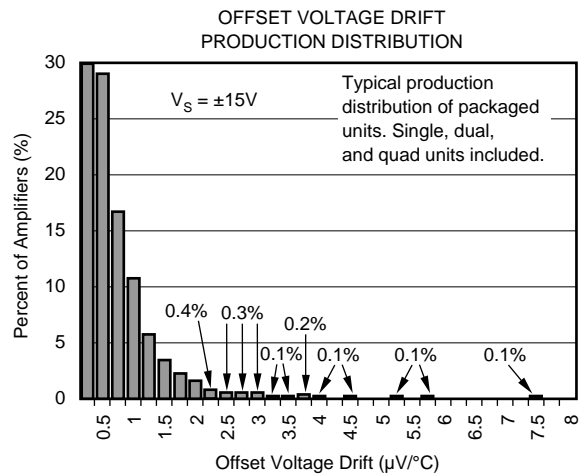
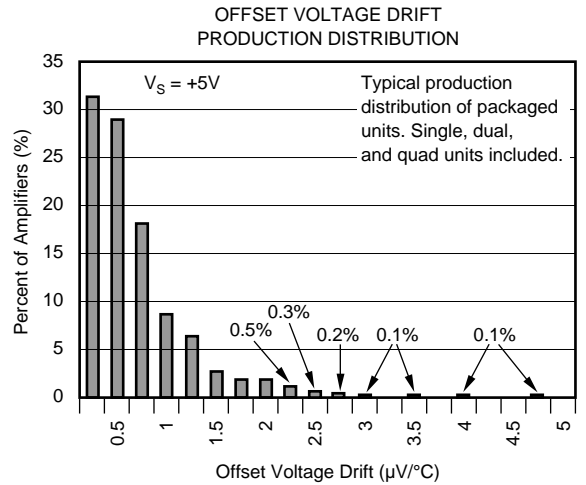
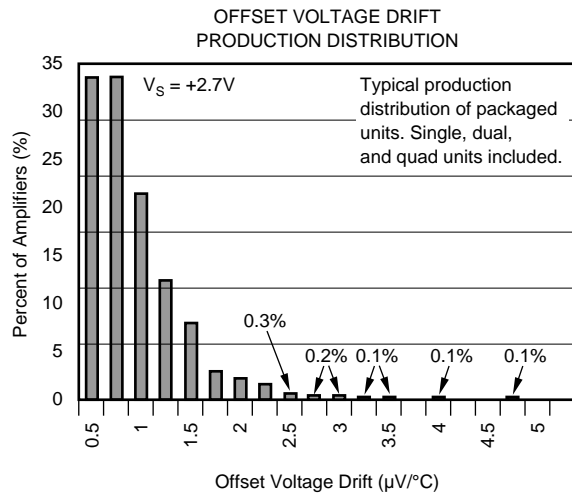
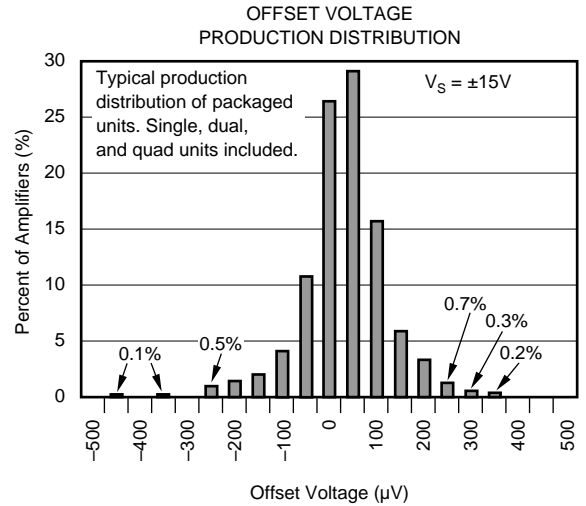
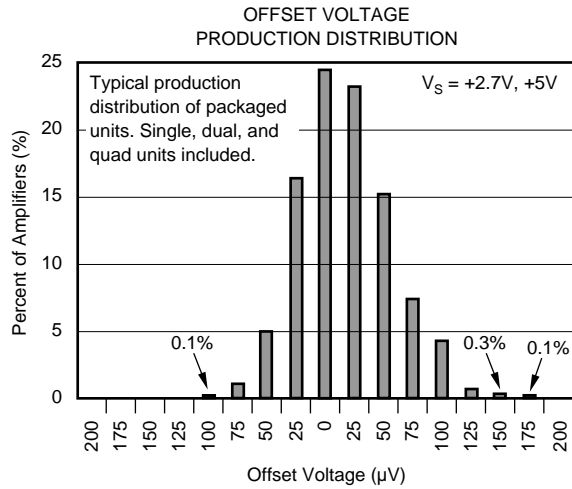
# TYPICAL CHARACTERISTIC CURVES

At  $T_A = +25^\circ\text{C}$  and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



# TYPICAL CHARACTERISTIC CURVES (Cont.)

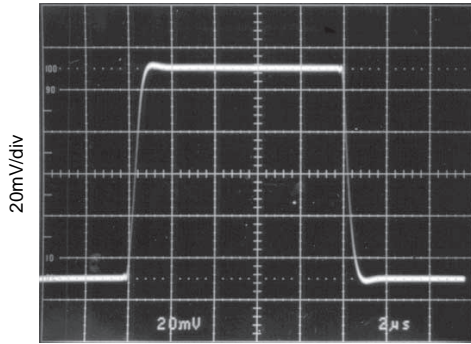
At  $T_A = +25^\circ\text{C}$  and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



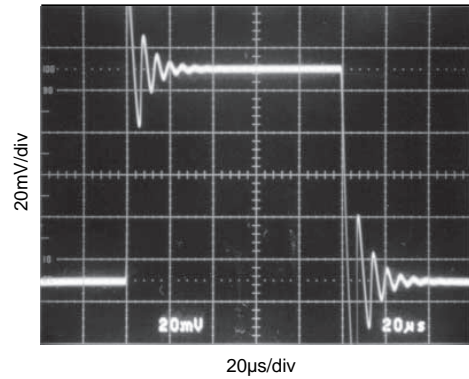
# TYPICAL CHARACTERISTIC CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$  and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

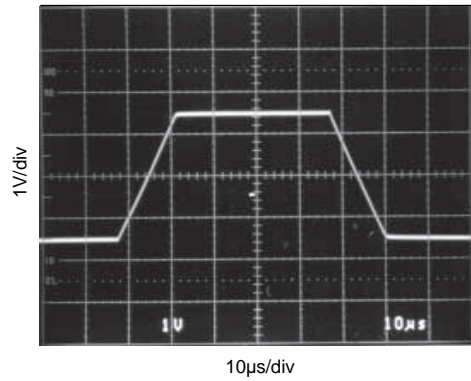
SMALL-SIGNAL STEP RESPONSE  
 $G = 1, C_L = 100\text{pF}, V_S = +5\text{V}$



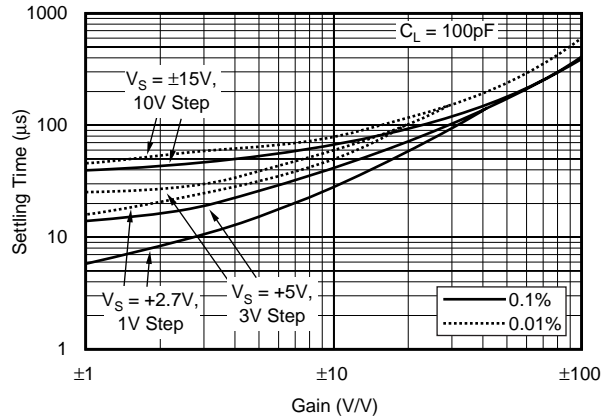
SMALL-SIGNAL STEP RESPONSE  
 $G = 1, C_L = 10,000\text{pF}, V_S = +5\text{V}$



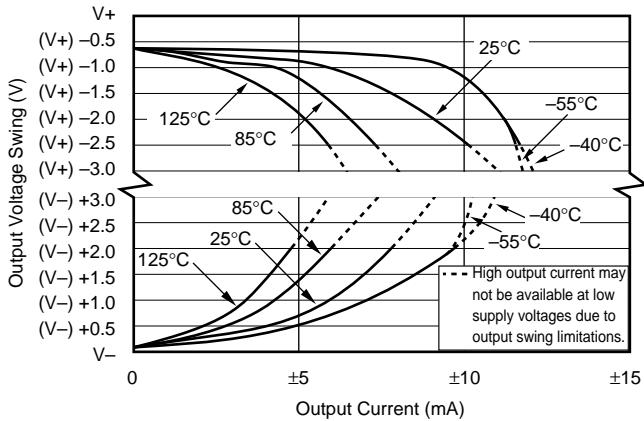
LARGE-SIGNAL STEP RESPONSE  
 $G = 1, C_L = 100\text{pF}, V_S = +5\text{V}$



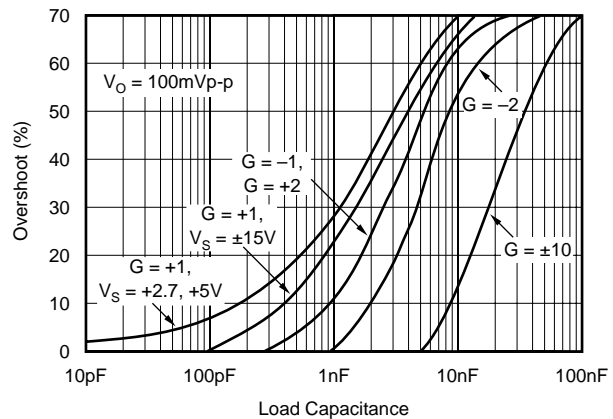
SETTLING TIME vs CLOSED-LOOP GAIN



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



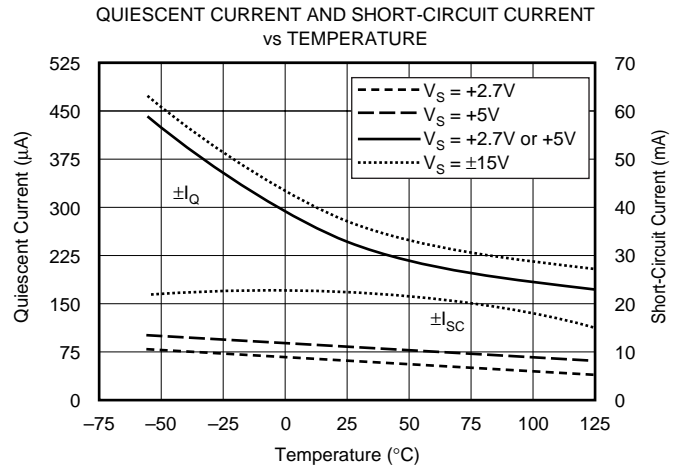
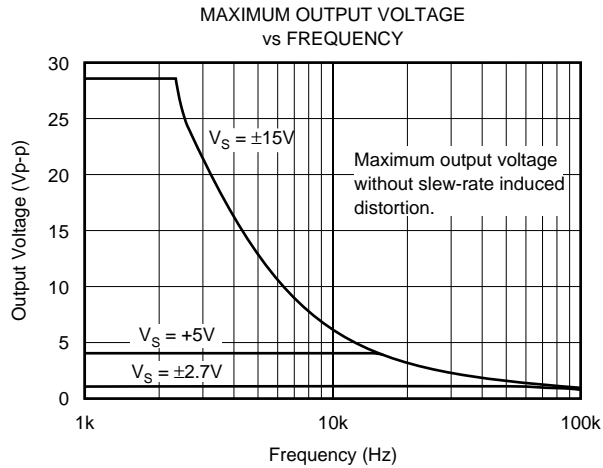
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE





# TYPICAL CHARACTERISTIC CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$  and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



## APPLICATIONS INFORMATION

The OPA234 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power-supply pins should be bypassed with 10nF ceramic capacitors.

### OPERATING VOLTAGE

The OPA234 series op amps operate from single (+2.7V to +36V) or dual ( $\pm 1.35\text{V}$  to  $\pm 18\text{V}$ ) supplies with excellent performance. Specifications are production tested with +2.7V, +5V, and  $\pm 15\text{V}$  supplies. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the Typical Characteristic curves.

### OFFSET VOLTAGE TRIM

Offset voltage of the OPA234 series amplifiers is laser trimmed and usually requires no user adjustment. The OPA234 (single op amp version) provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer, as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset could degrade the offset drift behavior of the op amp. While it is not possible to predict the exact change in drift, the effect is usually small.

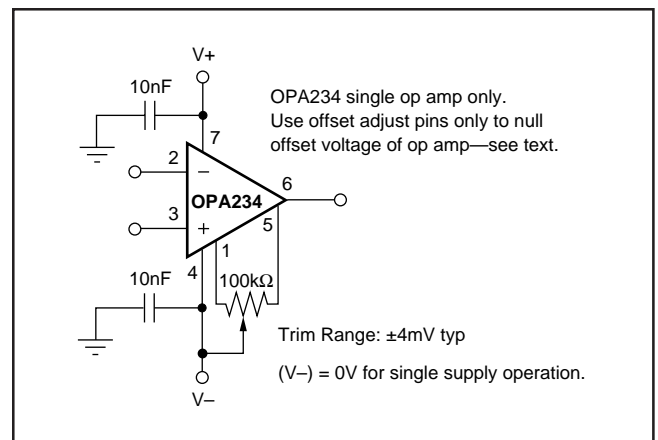


FIGURE 1. OPA234 Offset Voltage Trim Circuit.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2234U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 2234U	<a href="#">Samples</a>
OPA2234U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 2234U	<a href="#">Samples</a>
OPA2234U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 2234U	<a href="#">Samples</a>
OPA2234UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 2234U A	<a href="#">Samples</a>
OPA2234UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 2234U A	<a href="#">Samples</a>
OPA2234UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 2234U A	<a href="#">Samples</a>
OPA2234UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 2234U A	<a href="#">Samples</a>
OPA2234UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 2234U	<a href="#">Samples</a>
OPA234E/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU   Call TI	Level-3-260C-168 HR	-40 to 125	A34	<a href="#">Samples</a>
OPA234E/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 125	A34	<a href="#">Samples</a>
OPA234E/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   Call TI	Level-3-260C-168 HR	-40 to 125	A34	<a href="#">Samples</a>
OPA234EA/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU   Call TI	Level-3-260C-168 HR	-40 to 125	A34	<a href="#">Samples</a>
OPA234EA/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 125	A34	<a href="#">Samples</a>
OPA234EA/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   Call TI	Level-3-260C-168 HR	-40 to 125	A34	<a href="#">Samples</a>
OPA234U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	OPA 234U	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA234U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	OPA 234U	<a href="#">Samples</a>
OPA234UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	OPA 234U A	<a href="#">Samples</a>
OPA234UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	OPA 234U A	<a href="#">Samples</a>
OPA234UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	OPA 234U A	<a href="#">Samples</a>
OPA234UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	OPA 234U	<a href="#">Samples</a>
OPA4234U	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4234U	<a href="#">Samples</a>
OPA4234U/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4234U	<a href="#">Samples</a>
OPA4234UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4234U A	<a href="#">Samples</a>
OPA4234UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4234U A	<a href="#">Samples</a>
OPA4234UA/2K5G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4234U A	<a href="#">Samples</a>
OPA4234UAG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4234U A	<a href="#">Samples</a>
OPA4234UG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4234U	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF OPA2234 :**

- Military: [OPA2234M](#)

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2234U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2234UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA234E/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA234E/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA234EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA234EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA234U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA234UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4234U/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4234UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2234U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA2234UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA234E/250	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA234E/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA234EA/250	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA234EA/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA234U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA234UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA4234U/2K5	SOIC	D	14	2500	367.0	367.0	38.0
OPA4234UA/2K5	SOIC	D	14	2500	367.0	367.0	38.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

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