High Speed CMOS 8-Bit Buffer/Line Drivers

QS54/74FCT540T
QS54/74FCT541T

QS54/74FCT2540T
QS54/74FCT2541T

FEATURES/BENEFITS

- Pin and function compatible to the 74F540/541 74FCT540/541 and 74ABT540/541
- CMOS power levels: <7.5 mW static
- Available in DIP, SOIC, QSOP, ZIP, HQSOPW
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 540T, 541T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std. thru D speed grades with 3.8 ns t_{PD} for D
- I_{OL} = 64 mA Com., 48 mA Mil.

FCT-T 2540T, 2541T

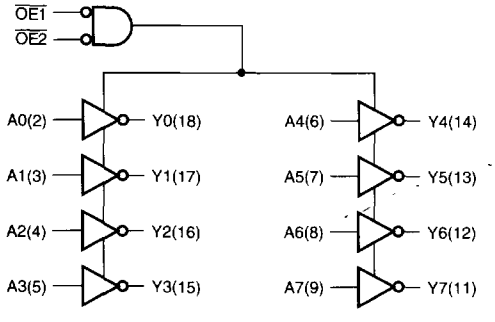
- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std. thru D speed grades with 3.8 ns t_{PD} for D
- I_{OL} = 12 mA Com.

DESCRIPTION

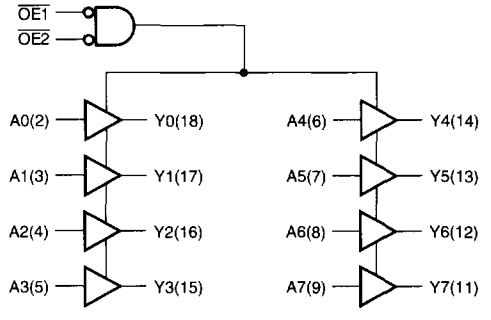
The QSFCT540T and QSFCT541T are 8-bit buffer/line drivers with three-state outputs that are ideal for driving high-capacitance loads as in memory address and data buses. The FCT2540 and FCT2541 are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2540 series parts can replace the 540 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

FCT540/2540

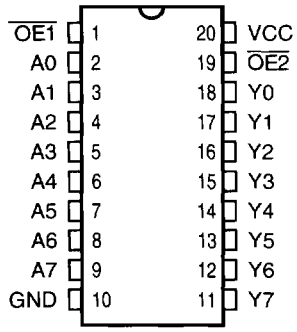


FCT541/2541

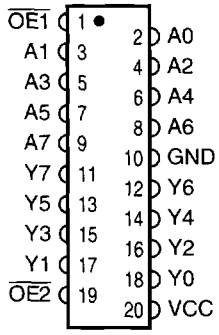


PIN CONFIGURATIONS (All Pins Top View)

PDIP, SOIC, QSOP, HQSOP



ZIP



PIN DESCRIPTION

Name	I/O	Description
A7-A0	I	Data Inputs
Y7-Y0	O	Data Outputs
$\overline{OE1}$, $\overline{OE2}$	I	Output Enable

FUNCTION TABLE

$\overline{OE1}$	$\overline{OE2}$	Input A	540 Output Y	541 Output Y	Function
H	X	X	Hi-Z	Hi-Z	Disable Outputs
X	H	X	Hi-Z	Hi-Z	
L	L	L	H	L	Enable Outputs
L	L	H	L	H	

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5V to +7.0V
DC Output Voltage V_{OUT}	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	–3.0V
DC Input Diode Current with $V_{IN} < 0$	–20 mA
DC Output Diode Current with $V_{OUT} < 0$	–50 mA
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1, 19	4	4	5	7	pF
—	6	6	7	9	pF
2-9, 11-18	8	8	9	10	pF

Note: Capacitance is characterized but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Min	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = Max., freq = 0 0V ≤ V_{IN} ≤ 0.2V or Vcc-0.2V ≤ V_{IN} ≤ Vcc	—	1.5	mA
ΔIcc	Supply Current per Input @ TTL HIGH	Vcc = Max., V_{IN} = 3.4V, freq = 0[2]	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz	Vcc = Max., Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or Vcc[3,4]	—	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	Vcc = Max., $0 \le V_{IN} < V_{CC}$	—	—	5	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	Vcc = Max., $0 \le V_{IN} \le V_{CC}$	—	—	5	µA
I_{OS}	Short Circuit Current (FCTXXX)	Vcc = Max., V_{OUT} = GND(2,3)	–60	—	—	mA
I_{OR}	Current Drive (FCT2XXX – 25Ω)	Vcc = Min., V_{OUT} = 2.0V(3)	50	—	—	mA
V_{IC}	Input Clamp Voltage	Vcc = Min., I_{IN} = –18 mA, T_A = 25°C(3)	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	Vcc = Min. I_{OH} = –12 mA (MIL) I_{OH} = –15 mA (COM)	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage (FCTXXX)	Vcc = Min. I_{OL} = 48 mA (MIL) I_{OL} = 64 mA (COM)	— —	— —	0.55 0.55	V
V_{OL}	Output LOW Voltage (FCT2XXX – 25Ω)	Vcc = Min. I_{OL} = 12 mA (MIL) I_{OL} = 12 mA (COM)	— —	— —	0.50 0.50	V
R_{OUT}	Output Resistance (FCT2XXX – 25Ω)	Vcc = Min. I_{OL} = 12 mA (MIL) I_{OL} = 12 mA (COM)	— 20	25 28	— 40	Ω

Notes:
1. Typical values indicate Vcc = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, Vcc = 5.0V ± 5% Military T_A = –55°C to 125°C, Vcc = 5.0V ± 10%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

QSFCT540/2540

Symbol	Description[1]		540T 2540T Min	540T 2540T Max	540AT 2540AT Min	540AT 2540AT Max	540CT 2540CT Min	540CT 2540CT Max	540DT 2540DT Min	540DT 2540DT Max	Unit
t_{PLH}	Propagation Delay	COM	1.5	8.5	1.5	4.8	1.5	4.1	1.5	3.8	ns
t_{PHL}	Ai to Yi	MIL	1.5	9.5	1.5	5.1	1.5	4.6	1.5	4.4	
t_{PZH}	Output Enable	COM	1.5	10	1.5	6.2	1.5	5.8	1.5	5.2	ns
t_{PZL}	$\overline{OE}$ to Yi	MIL	1.5	10.5	1.5	6.5	1.5	6.5	1.5	6.5	
t_{PLZ}	Disable Time	COM[2]	1.5	9.5	1.5	5.6	1.5	5.2	1.5	5.2	ns
t_{PHZ}		MIL[2]	1.5	12.5	1.5	5.9	1.5	5.7	1.5	5.7	

Notes:
1. Minimum propagation delay values are guaranteed but not tested.
2. This parameter is guaranteed but not tested.

QSFCT541/2541

Symbol	Description[1]		541T 2541T Min	541T 2541T Max	541AT 2541AT Min	541AT 2541AT Max	541CT 2541CT Min	541CT 2541CT Max	541DT 2541DT Min	541DT 2541DT Max	Unit
t_{PLH}	Propagation Delay	COM	1.5	8	1.5	4.8	1.5	4.1	1.5	3.8	ns
t_{PHL}	Ai to Yi	MIL	1.5	9	1.5	5.1	1.5	4.6	1.5	4.4	
t_{PZH}	Output Enable	COM	1.5	10	1.5	6.2	1.5	5.8	1.5	5.2	ns
t_{PZL}	$\overline{OE}$ to Yi	MIL	1.5	10.5	1.5	6.5	1.5	6.5	1.5	6.5	
t_{PLZ}	Disable Time	COM[2]	1.5	9.5	1.5	5.6	1.5	5.2	1.5	5.2	ns
t_{PHZ}		MIL[2]	1.5	12.5	1.5	5.9	1.5	5.7	1.5	5.7	

Notes:
1. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.