

Features

- Simple Single-Loop Control Design
 - Voltage-Mode PWM Control
- Excellent Output Voltage Regulation
 - PWM Output : $\pm 1\%$ Over Temperature
- Fast Transient Response
 - High-Bandwidth Error Amplifier
 - Full 0% to 100% Duty Ratio
- 3-Bit Digital-to-Analog Output Voltage Selection
- Over-Voltage and Over-Current Fault Monitors
- Small Converter Size
 - 200kHz Free-Running Oscillator
 - Programmable from 50kHz to 800kHz

Applications

- High-Power 5V to 3.3V (or below) DC-DC Regulators
- Low-Voltage Distributed Power Supplies
- VGA Card Power Regulation

General Description

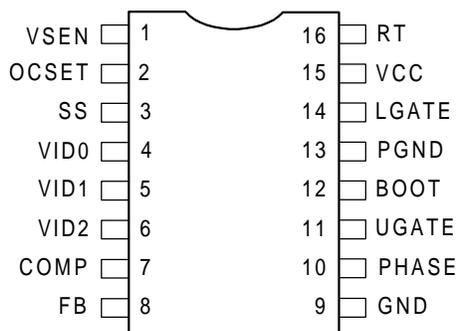
The APW7016 provides a complete control and protection for a DC-DC converter optimized for high performance microprocessor applications. It is designed to drive two N-Channel MOSFETs in a synchronous-rectified buck topology. The APW7016 integrates output voltage control, monitoring and protection functions into a single Package.

The APW7016 includes a 3-bit digital-to-analog converter (DAC) that provides a easily adjustable and precisely output voltage from $1.3V_{DC}$ to $1.65V_{DC}$ in 0.05V steps. Any selected output voltage can be maintained within $\pm 1\%$ accuracy over temperature and line voltage variations.

With a 200kHz free-running triangle-wave oscillator and a error amplifier featuring a 15MHz unity-gain bandwidth and 6V/ μ s slew rate inside the chip, APW7016 can implement a simple, single feedback loop, voltage-mode control topology with high transient performance.

The APW7016 also features with multiple protections against over-current and over-voltage conditions by inhibiting PWM operation. The APW7016 uses the $R_{DS(ON)}$ of the upper MOSFET as the current sensing element which eliminates the demand for an extra component. The APW7016 also monitors the output voltage using a comparator with hysteresis that tracks the DAC output.

Pin Description

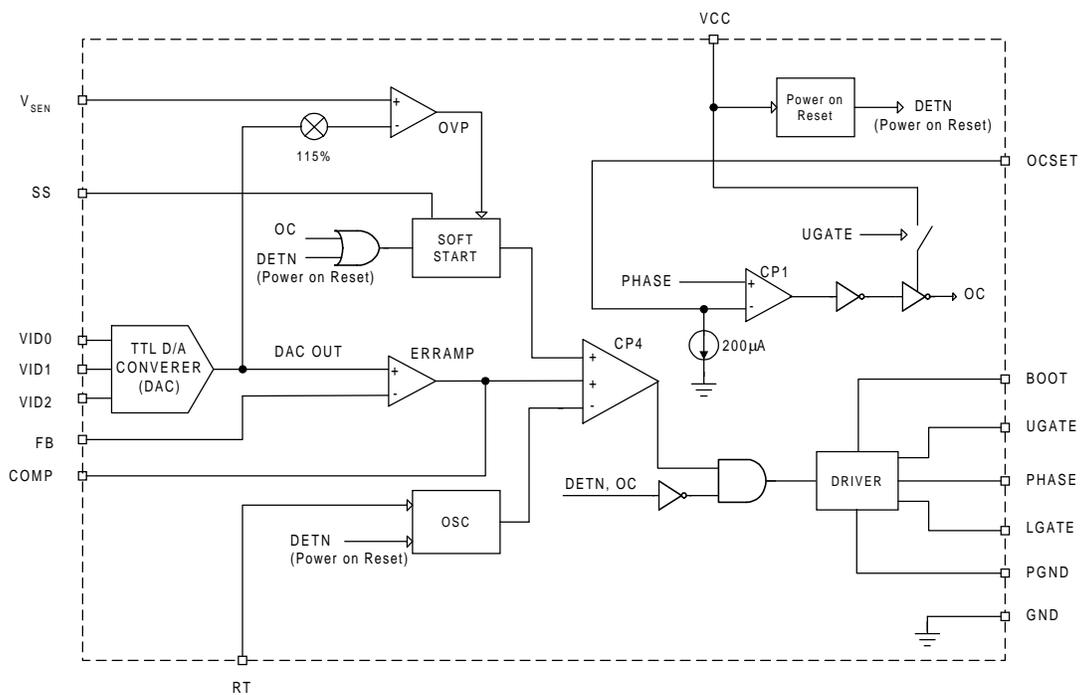


ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

<p>APW 7016 □□-□□□</p> <p style="margin-left: 40px;"> └─ Lead Free Code └─ Handling Code └─ Temp. Range └─ Package Code </p>	<p>Package Code K : SOP - 16 N : SSOP - 16</p> <p>Temp. Range C : 0 to 70 °C</p> <p>Handling Code TU : Tube TR : Tape & Reel</p> <p>Lead Free Code L : Lead Free Device Blank : Original Device</p>
<p>APM7016 K/N : APM7017 XXXXX</p>	<p>XXXXX - Date Code</p>

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V _{CC}	Supply Voltage	15	V
V _{BOOT}	Boot Voltage	15	V
V _I , V _O	Input , Output or I/O Voltage	GND - 0.3 V to V _{CC} + 0.3	V
T _A	Operating Ambient Temperature Range	0 to 70	°C
T _J	Junction Temperature Range	0 to 150	°C
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _S	Soldering Temperature	300,10 seconds	°C

Thermal Characteristics

Symbol	Parameter	Value	Unit
R _{θJA}	Thermal Resistance in Free Air		
	SOP , SSOP	110	°C/W
	SOP (with 3in ² of Copper)	86	

Electrical Characteristics

Recommended operating conditions , unless otherwise noted

Symbol	Parameter	Test Conditions	APW7016			Unit
			Min.	Typ.	Max.	
V_{CC} Supply Current						
I _{CC}	Nominal Supply	UGATE and LGATE open		3		mA
Power-on Reset						
	Rising V _{CC} Threshold	Vocset=4.5V			10.7	V
	Falling V _{CC} Threshold	Vocset=4.5V	8.2			V
Oscillator						
	Free Running Frequency	RT= Open	185	200	215	kHz
ΔV _{OSC}	Ramp Amplitude	RT= Open		2		V _{P-P}
Reference and DAC						
	DAC(VID0-VID2) Input Low Voltage				0.8	V
	DAC(VID0-VID2) Input High Voltage			3.0		V
	DACOUT Voltage accuracy		-1.0		+1.0	%
Error Amplifier						
	DC Gain			88		dB
GBW	Gain-Bandwidth Product			15		MHz
SR	Slew Rate	COMP=20pF		6		V/μs
PWM Controller Gate Driver						
R _{UGATE}	UGATE Source	V _{CC} =12V , V _{UGATE} =6V	350	500		mA
R _{UGATE}	UGATE Sink	V _{UGATE-PHASE} =1V		5.5	10	Ω
R _{LGATE}	LGATE Source	V _{CC} =12V , V _{LGATE} =1V	350	450		mA
R _{LGATE}	LGATE Sink	V _{LGATE} =1V		3.5	6.5	Ω
Protection						
	Over-Voltage Trip (V _{SEN} /DACOUT)			115	120	%
I _{OCSET}	OCSET Current Source	V _{OCSET} =4.5V _{DC}	170	200	230	μA
I _{SS}	Soft Start Current			10		μA

Pin Function Description

VSEN (pin 1)

Connect this pin to the converter's voltage output. The OVP comparator circuits monitor output voltage status and act over voltage protection by using this signal.

OCSET(pin 2)

Connect a resistor(R_{OCSET}) from this pin to the drain of the upper MOSFET. An internal 200 μ A current source (I_{OCS}), R_{OCSET} , and the upper MOSFET's on-resistance ($R_{DS(ON)}$) set the converter over-current (OC) trip point according to the following equation :

$$I_{PEAK} = \frac{I_{OCSET} * R_{OCSET}}{R_{DS(ON)}}$$

An over-current trip resets the soft-start function.

SS (Pin 3)

Connect a capacitor from this pin to ground. This capacitor, along with an internal 10 μ A current source, sets the soft-start interval of the converter.

VID0-2 (Pins 4-6)

VID0-2 are the input pins to the 3-bit DAC. The states of these three pins decide the internal voltage reference (DACOUT). The level of DACOUT sets the converter output voltage and also sets the OVP thresholds. Table 1 specifies DACOUT for the 8 combinations of DAC inputs.

COMP (pin 7) and FB (pin 8)

COMP and FB are the accessible pins of the error amplifier. FB pin is the inverting input of the error amplifier and COMP pin is output of the error amplifier. These pins provide the compensation for the voltage-control feedback loop of the converter.

GND (Pin 9)

GND is signal ground of the IC. All voltage levels are measured with respect to this pin.

PHASE (pin 10)

Connect the PHASE pin to the source of the upper MOSFET. This pin is used to monitor the voltage drop across the upper MOSFET for over-current protection.

UGATE (pin 11)

Connect UGATE to the upper MOSFET gate. This pin enables the gate drive signal to drive the upper MOSFET .

BOOT (pin 12)

BOOT pin provides bias voltage to the upper MOSFET gate driver. A bootstrap circuit could be used to pump a BOOT voltage for enforcing the driving capability of the gate driver and improving the performance of the upper MOSFET.

PGND(pin 13)

PGND pin provides the power ground connection. Connect this pin to the source of the lower MOSFET.

LGATE (pin 14)

Connect LGATE to the lower MOSFET gate. This pin enables the gate drive signal to drive the lower MOSFET.

VCC (pin 15)

Connect VCC to 12V voltage supply. This pin supplies the bias for the chip.

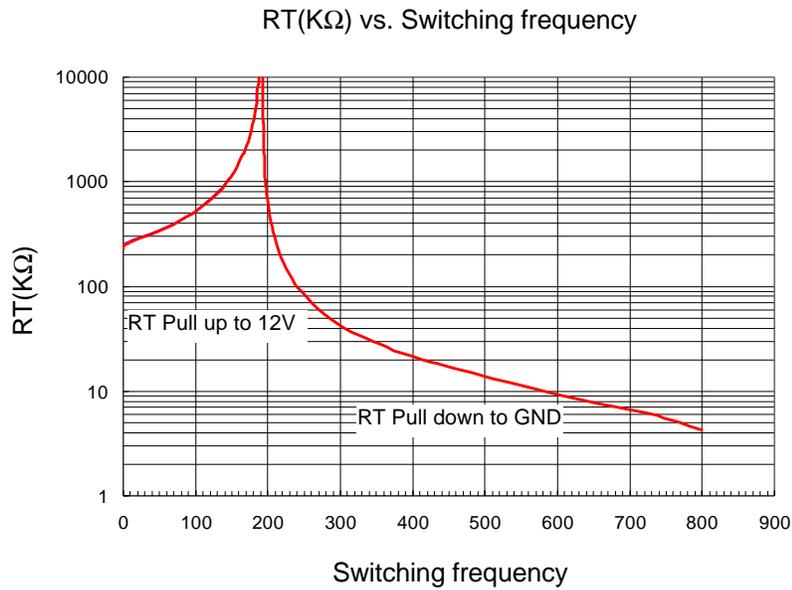
RT (pin 16)

RT pin provides oscillator switching frequency adjustment. By connecting a resistor (R_T) from this pin to GND, the nominal 200kHz switching frequency is increased. Conversely, connecting a pull-up resistor (R_T) from this pin to V_{CC} reduces the switching frequency.

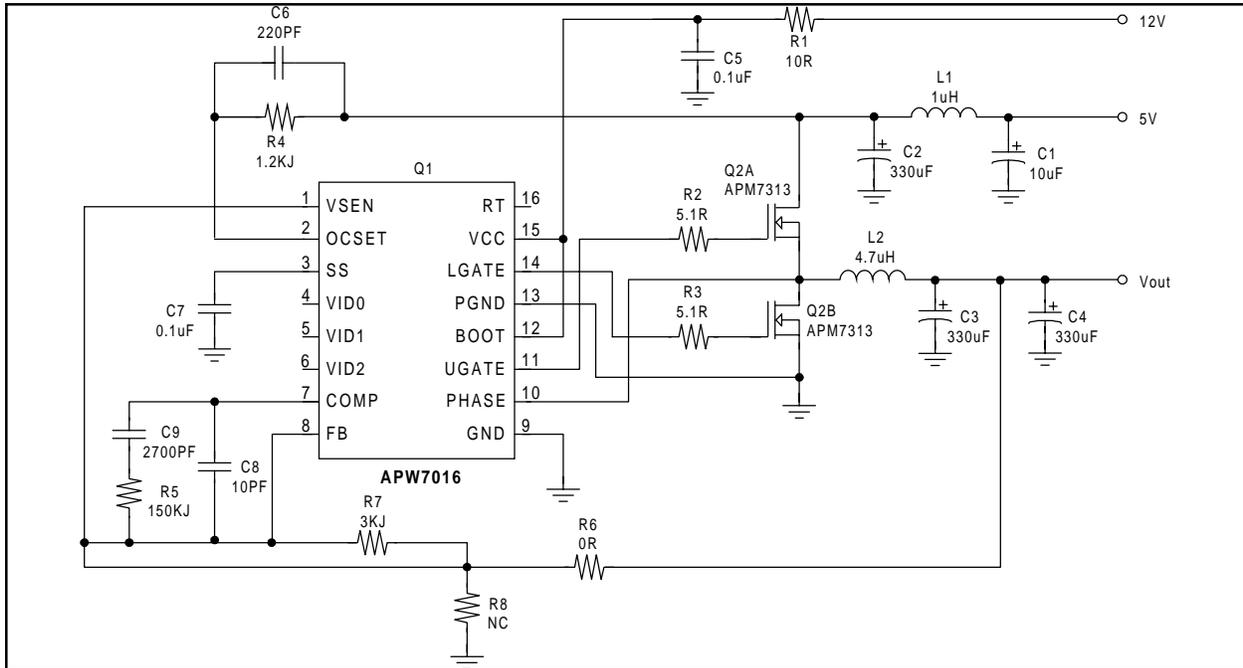
Table 1 Output Voltage Program

Pin Name			Nominal Output Voltage Dacout
VID2	VID1	VID0	
1	1	1	1.3
1	1	0	1.35
1	0	1	1.4
1	0	0	1.45
0	1	1	1.5
0	1	0	1.55
0	0	1	1.6
0	0	0	1.65

Typical Performance Curve

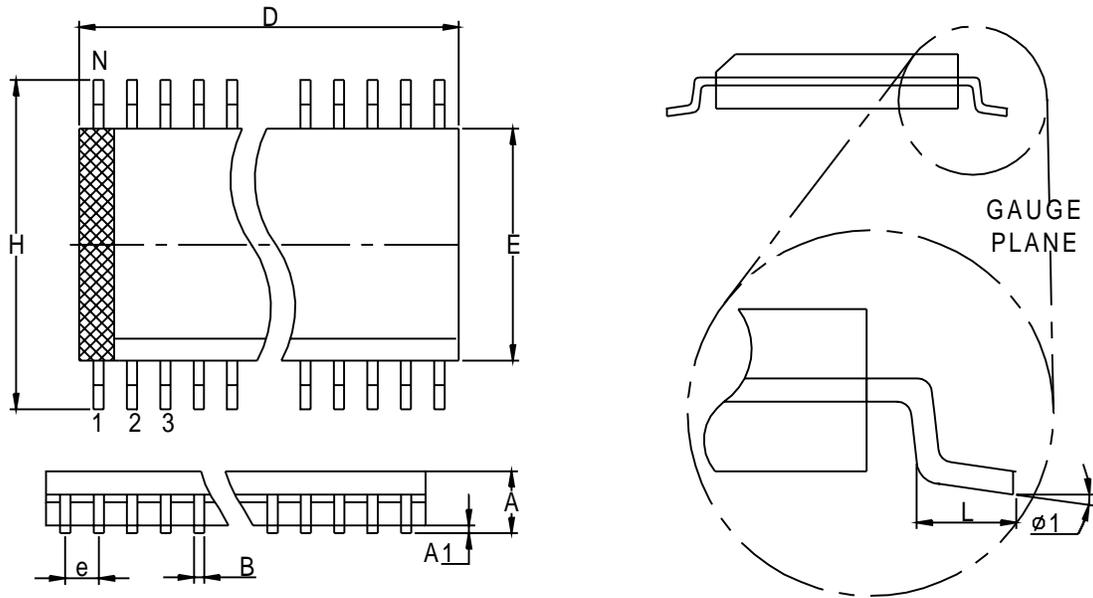


Application Schematic



Package Information

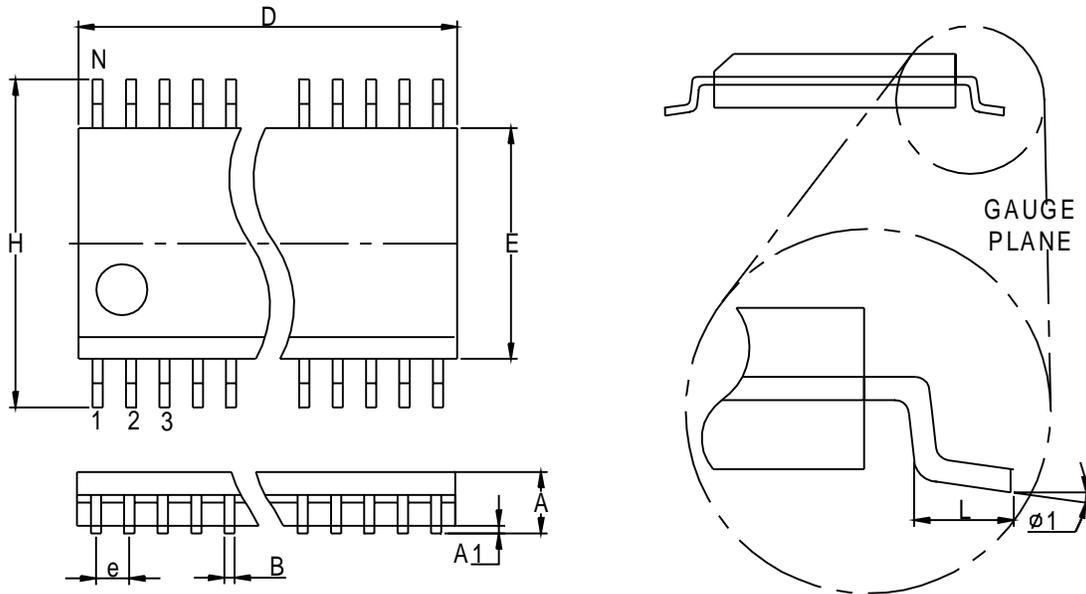
SO – 300mil (Reference JEDEC Registration MS-013)



Dim	Millimeters		Variations- D			Dim	Inches		Variations- D		
	Min.	Max.	Variations	Min.	Max.		Min.	Max.	Variations	Min.	Max.
A	2.35	2.65	SO-16	10.10	10.50	A	0.093	0.1043	SO-16	0.398	0.413
A1	0.10	0.30	SO-18	11.35	11.76	A1	0.004	0.0120	SO-18	0.447	0.463
B	0.33	0.51	SO-20	12.60	13	B	0.013	0.020	SO-20	0.496	0.512
D	See variations		SO-24	15.20	15.60	D	See variations		SO-24	0.599	0.614
E	7.40	7.60	SO-28	17.70	18.11	E	0.2914	0.2992	SO-28	0.697	0.713
e	1.27BSC		SO-14	8.80	9.20	e	0.050BSC		SO-14	0.347	0.362
H	10	10.65				H	0.394	0.419			
L	0.40	1.27				L	0.016	0.050			
N	See variations					N	See variations				
φ 1	0°	8°				φ 1	0°	8°			

Package Information

SSOP-16

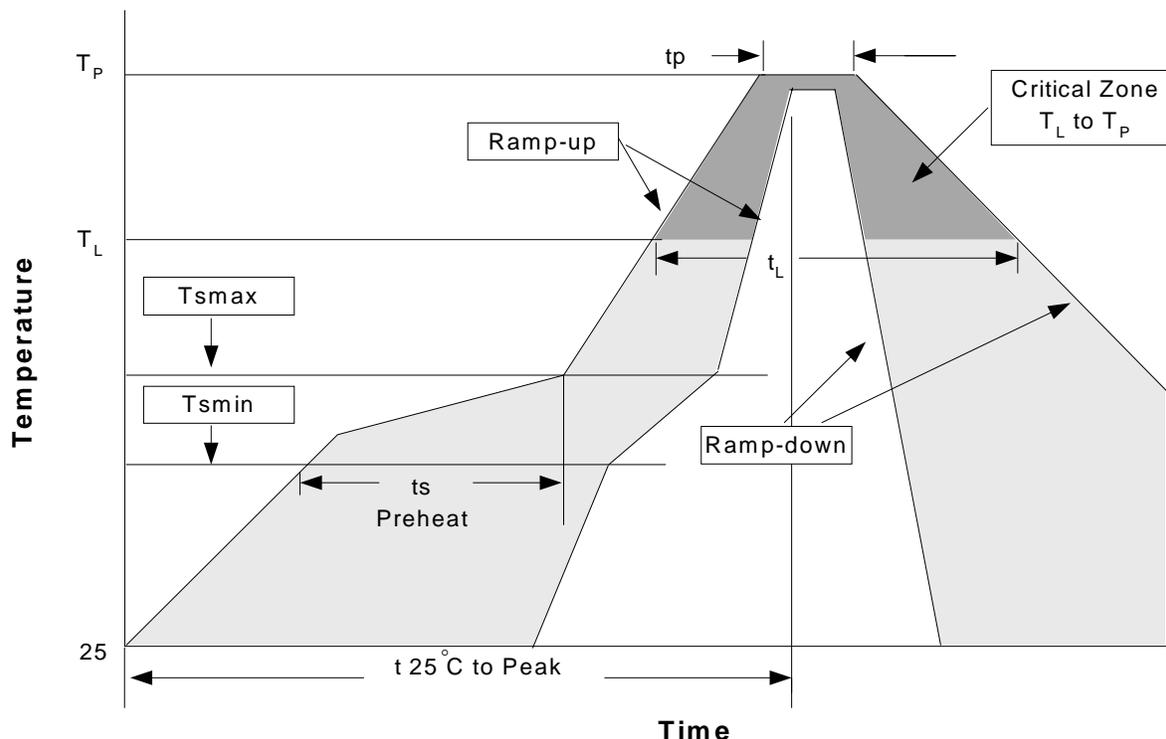


Dim	Millimeters		Variations- D			Dim	Inches		Variations- D		
	Min.	Max.	Variations	Min.	Max.		Min.	Max.	Variations	Min.	Max.
A	1.350	1.75	SSOP-16	4.75	5.05	A	0.053	0.069	SSOP-16	0.187	0.199
A1	0.10	0.25				A1	0.004	0.010			
B	0.20	0.30				B	0.008	0.012			
D	See variations					D	See variations				
E	3.75	4.05				E	0.147	0.160			
e	0.625 TYP.					e	0.025 TYP.				
H	5.75	6.25				H	0.226	0.246			
L	0.4	1.27				L	0.016	0.050			
N	See variations					N	See variations				
$\phi 1$	0°	8°				$\phi 1$	0°	8°			

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

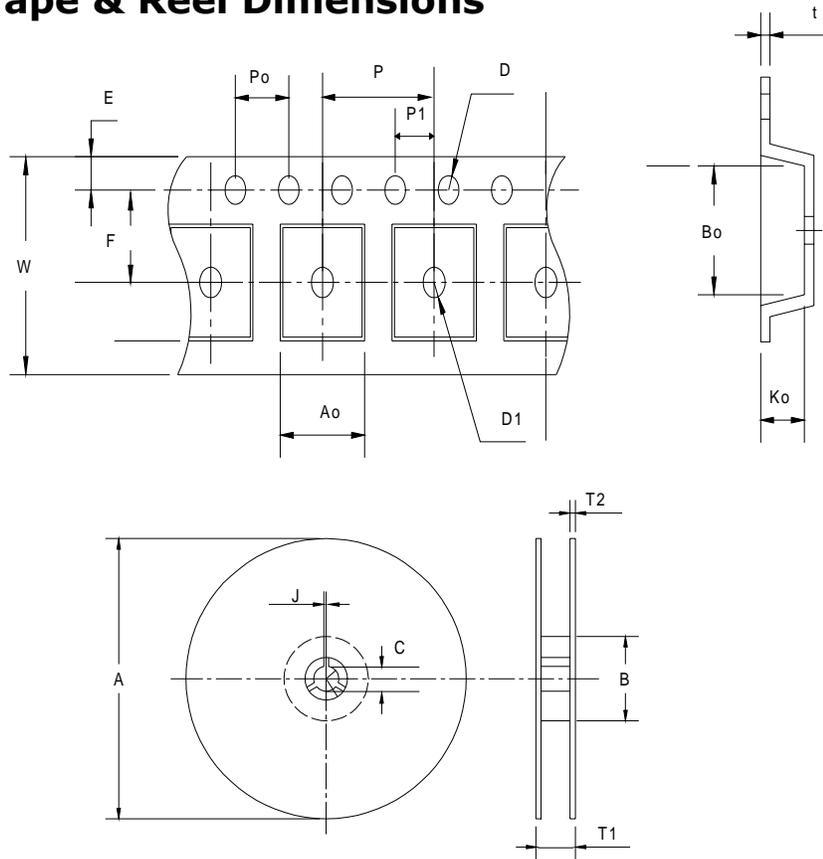
Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly	
	Large Body	Small Body	Large Body	Small Body
Average ramp-up rate (T_L to T_P)	3°C/second max.		3°C/second max.	
Preheat				
- Temperature Min (T_{smin})	100°C		150°C	
- Temperature Mix (T_{smax})	150°C		200°C	
- Time (min to max)(t_s)	60-120 seconds		60-180 seconds	
T_{smax} to T_L				
- Ramp-up Rate			3°C/second max	
T_{smax} to T_L				
- Temperature(T_L)	183°C		217°C	
- Time (t_L)	60-150 seconds		60-150 seconds	
Peak Temperature(T_p)	225 +0/-5°C	240 +0/-5°C	245 +0/-5°C	250 +0/-5°C
Time within 5°C of actual Peak Temperature(t_p)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.		6°C/second max.	
Time 25°C to Peak Temperature	6 minutes max.		8 minutes max.	

Note: All temperatures refer to topside of the package. Measured on the body surface.

Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I _{lr} > 100mA

Carrier Tape & Reel Dimensions



Application	A	B	C	J	T1	T2	W	P	E
SOP- 16	330 ± 1	100 +2	13+ 0.5	2 ± 0.5	16.4 ^{+0.3} _{-0.2}	2.5 ± 0.5	16± 0.2	12± 0.1	1.75±0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	7.5± 0.1	1.5 +0.1	1.5+ 0.25	4.0 ± 0.1	2.0 ± 0.1	10.9 ± 0.1	10.8± 0.1	3.0± 0.1	0.3±0.013
Application	A	B	D0	D1	E	F	P0	P1	P2
SSOP-16	6.95	5.4	1.55±0.05	1.55±0.1	1.75±0.1	5.5±0.05	4.0±0.1	8.0±0.1	2.0±0.05
	T	T2	W	W1	C1	C2	T1	T2	C
	0.3±0.05	2.2	12.0±0.3	9.5	13±0.3	21±0.8	13.5±0.5	2.0±0.2	80±1

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 16	24	21.3	1000

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