FEATURES/BENEFITS

- **Generates system clock for 80286 processors**
- **Uses crystal or TTL signal for frequency source**
- **Provides local $\overline{\text{READY}}$ and IEEE-796 (Multibus®) $\overline{\text{READY}}$ synchronization**
- **Generates system RESET output from Schmitt trigger input**
- **Single +5V power supply**
- **Low power CMOS**
- **Works with KS82C288 Bus Controller and KS82C289 Bus Arbiter**
- **10, 12.5, and 16 MHz versions**
- **20-lead PLCC or 18-pin plastic DIP**

DESCRIPTION

The KS82C284 clock generator/driver provides clock signals for 80286 processors and support components. It also supplies the $\overline{\text{READY}}$ signal to the CPU from either synchronous or asynchronous sources. The KS82C284 supplies synchronous RESET from an asynchronous input with hysteresis.

Figure 1. KS82C284 Block Diagram

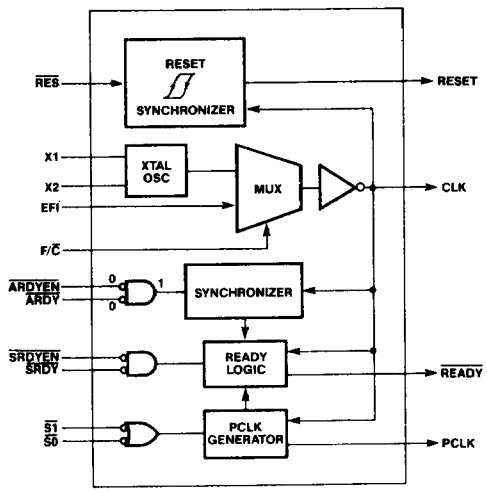


Figure 2a. KS82C284 PLCC Pin Diagram

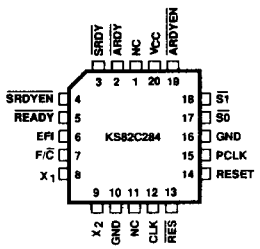


Figure 2b. KS82C284 Plastic DIP Pin Diagram

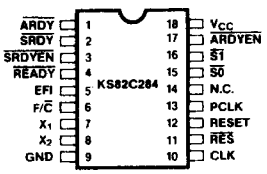


Table 1: KS82C284 Interface Signal Descriptions

Symbol	Type	Name and Function
CLK	O	**System Clock:** This signal is used by the processor and support devices (which must be synchronous with the processor). The frequency of the CLK output is twice the processor's desired internal clock frequency. CLK can drive both TTL- and MOS-level inputs.
F/$\overline{C}$	I	**Frequency/Crystal Select:** This is a strapping option that selects the source for the CLK output. When F/$\overline{C}$ is strapped LOW, the internal crystal oscillator drives CLK. When F/$\overline{C}$ is strapped HIGH, EFI drives the CLK output.
X1, X2	I	**Crystal in 1, Crystal in 2:** A parallel resonant fundamental mode crystal is attached to these pins for the internal oscillator. When F/$\overline{C}$ is LOW, the internal oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the processor's desired internal clock frequency.
EFI	I	**External Frequency In:** This signal drives the CLK when the F/$\overline{C}$ input is strapped HIGH. The EFI input frequency must be twice the processor's desired internal clock frequency.
PCLK	O	**Peripheral Clock:** Provides a 50% duty-cycle clock with 1/2 the frequency of CLK. PCLK will be in phase with the internal processor clock following the first bus cycle after the processor has been reset.
$\overline{\text{ARDYEN}}$	I	**Asynchronous Ready Enable:** Qualifies the Asynchronous Ready ($\overline{\text{ARDY}}$) input. $\overline{\text{ARDYEN}}$ selects $\overline{\text{ARDY}}$ as the source of $\overline{\text{READY}}$ for the current bus cycle. Inputs to $\overline{\text{ARDYEN}}$ may be applied asynchronously to CLK. Setup and hold times must be observed in order to assure a guaranteed response to synchronous inputs.
$\overline{\text{ARDY}}$	I	**Asynchronous Ready:** Used to terminate the current bus cycle. The $\overline{\text{ARDY}}$ input is qualified by $\overline{\text{ARDYEN}}$. Input to $\overline{\text{ARDY}}$ may be applied asynchronously to CLK. Setup and hold times must be observed in order to assure a guaranteed response to synchronous outputs.
$\overline{\text{SRDYEN}}$	I	**Synchronous Ready Enable:** Qualifies the Synchronous Ready ($\overline{\text{SRDY}}$) input. $\overline{\text{SRDYEN}}$ selects $\overline{\text{SRDY}}$ as the source for $\overline{\text{READY}}$ to the CPU for the current bus cycle. Setup and hold times must be observed for proper operation.
$\overline{\text{SRDY}}$	I	**Synchronous Ready:** Terminates the current bus cycle. The $\overline{\text{SRDY}}$ input is qualified by the $\overline{\text{SRDYEN}}$ input. Setup and hold times must be observed for proper operation.
$\overline{\text{READY}}$	O	**Ready:** Signals that the current bus cycle is completed. The $\overline{\text{SRDY}}$, $\overline{\text{SRDYEN}}$, $\overline{\text{ARDY}}$, $\overline{\text{ARDYEN}}$, S1, $\overline{\text{S0}}$, and $\overline{\text{RES}}$ inputs control $\overline{\text{READY}}$ as explained in the $\overline{\text{READY}}$ generator section of this data sheet. $\overline{\text{READY}}$ is an open-drain output requiring an external pull-up resistor.
$\overline{\text{S0}}$, $\overline{\text{S1}}$	I	**Status 0, Status 1:** These signals prepare the KS82C284 for a subsequent bus cycle. $\overline{\text{S0}}$ and $\overline{\text{S1}}$ synchronize PCLK to the internal processor clock and control $\overline{\text{READY}}$. These inputs have internal pull-up resistors to keep them HIGH if nothing is driving them. Setup and hold times must be observed for proper operation.
RESET	O	**Reset:** Derived from the $\overline{\text{RES}}$ input. RESET is used to force the system into an initial state. When RESET is active (HIGH), $\overline{\text{READY}}$ will be active (LOW).
$\overline{\text{RES}}$	I	**Reset In:** Generates the system reset signal, RESET. Signals to $\overline{\text{RES}}$ may be applied asynchronously to CLK. A Schmitt trigger input is provided on $\overline{\text{RES}}$ so that an RC circuit can be used to provide a time delay. Setup and hold times must be observed to assure a guaranteed response to synchronous inputs.
V_{CC}	I	5V $\pm$ 5%.
GND	I	Ground.

FUNCTIONAL DESCRIPTION

Clock Generator

The CLK output provides the basic timing control for an 80286-based system. CLK has output characteristics sufficient to drive MOS devices. CLK is generated by either an internal crystal oscillator or an external source as selected by the F/$\overline{C}$ strapping option. When F/$\overline{C}$ is LOW, the crystal oscillator drives the CLK output. When F/$\overline{C}$ is HIGH, the EFI drives the CLK output.

The KS82C284 provides a second clock output, PCLK, for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and MOS output drive characteristics. PCLK is normally synchronized to the internal processor clock.

After RESET, the PCLK signal may be out of phase with the internal processor clock. The $\overline{S0}$ and $\overline{S1}$ signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its HIGH time beyond one system clock (see waveforms). PCLK is forced HIGH whenever either $\overline{S0}$ or $\overline{S1}$ have been active (LOW) for the two previous CLK cycles. PCLK continues to oscillate when both $\overline{S0}$ and $\overline{S1}$ are HIGH.

Since the phase of the internal processor clock will not change except during RESET, the phase of PCLK will not change except during the first bus cycle after RESET.

Oscillator

The KS82C284 incorporates a linear Pierce oscillator which requires an external parallel-resonant, fundamental mode, crystal. The output of the oscillator is internally buffered. The crystal frequency should be twice the required internal processor clock frequency. The crystal should have a typical load capacitance of 32pF.

X1 and X2 are the oscillator crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in Table 2.

The sum of the board-capacitance and loading-capacitance should equal the values shown. Stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) should be limited to less than 10pF between the X1 and X2 pins.

Decouple V_{CC} and GND as close to the KS82C284 as possible.

OPERATIONAL DESCRIPTION

CLK Termination

The CLK output has a very fast rise and fall time, so the CLK line be properly terminated at frequencies above 10MHz to avoid signal reflections and ringing. To terminate the CLK, insert a small resistor (typically 10Ω-74Ω) in series with the output, as shown in Figure 3. This type of termination is called series termination. The resistor value plus the circuit output impedance should be made equal to the impedance of the transmission line.

Figure 3. Series Termination

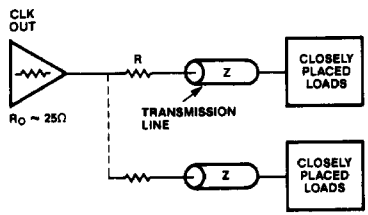


Table 2. KS82C284 Crystal Loading Capacitance Values

Crystal Frequency	C1 Capacitance X1	C2 Capacitance X2
1 to 8 MHz	60pF	40pF
8 to 20 MHz	25pF	15pF
Above 20 MHz	15pF	15pF

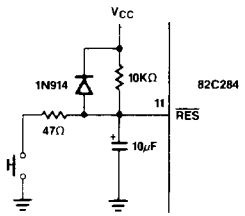
Note: Capacitance values must include stray board-capacitance.

Reset Operation

The reset logic provides the RESET output to force the system into a known, initial state. When the $\overline{RES}$ input is active (LOW), the RESET output goes active (HIGH). $\overline{RES}$ is synchronized internally at the falling edge of CLK before generating the RESET output (see waveforms). Synchronization of the RES input introduces a one- or two-CLK delay before affecting the RESET output.

On power-up, the system's V_{CC} and CLK are unstable. To prevent spurious activity, $\overline{RES}$ should be asserted until V_{CC} and CLK stabilize at their operating values. 80286 processors and support components also require their RESET inputs to be HIGH a minimum of 16 CLK cycles. An RC network, as shown in Figure 4, will keep $\overline{RES}$ LOW long enough to satisfy both the stability and CLK cycle requirements.

Figure 4. Typical RC $\overline{RES}$ Timing Circuit



An internal Schmitt trigger input with hysteresis on $\overline{RES}$ assures a single transition of RESET with an RC circuit on $\overline{RES}$. The hysteresis separates the input voltage-level at which the circuit output switches from HIGH to LOW from the input voltage level at which the circuit output switches from LOW to HIGH. The $\overline{RES}$ HIGH-to-LOW input transition voltage is lower than the $\overline{RES}$ LOW-to-HIGH input transition voltage. As long as the slope of the $\overline{RES}$ input voltage remains in the same direction (increasing or decreasing) around the $\overline{RES}$ input transition voltage, the RESET output will make a single transition.

Ready Operation

The KS82C284 accepts two ready sources for the system READY signal which terminates the current bus cycle. Either a synchronous ($\overline{SRDY}$) or an asynchronous ready ($\overline{ARDY}$) source may be used. Each ready input has an enable ($\overline{SRDYEN}$ and $\overline{ARDYEN}$) for selecting the type of ready source required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.

$\overline{READY}$ is enabled (LOW) if either SRDY + $\overline{SRDYEN}$ = 0 or ARDY + $\overline{ARDYEN}$ = 0 when sampled by the KS82C284 $\overline{READY}$ generation logic. $\overline{READY}$ will remain active for at least two CLK cycles.

The $\overline{READY}$ output has an open-drain driver allowing other ready circuits to be wire OR'ed with it, as shown in Figure 5. The $\overline{READY}$ signal of an 80286 system requires an external pull-up resistor. To force the $\overline{READY}$ signal inactive (HIGH) at the start of a bus cycle, the $\overline{READY}$ output floats when either $\overline{S0}$ or $\overline{S1}$ are sampled LOW at the falling edge of CLK. Two system clock periods are allowed for the pull-up resistor to pull the $\overline{READY}$ signal to V_{IH}. When RESET is active, $\overline{READY}$ is forced active one CLK later (see waveforms).

Figure 5. Recommended Crystal and $\overline{READY}$ Connections

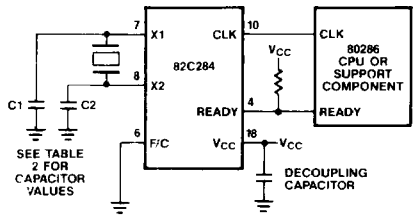


Figure 6 illustrates the operation of $\overline{SRDY}$ and $\overline{SRDYEN}$. These inputs are sampled on the falling edge of CLK when $\overline{S0}$ and $\overline{S1}$ are inactive (HIGH) and PCLK is HIGH. $\overline{READY}$ is forced active when both $\overline{SRDY}$ and $\overline{SRDYEN}$ are sampled as LOW.

Figure 7 shows the operation of $\overline{ARDY}$ and $\overline{ARDYEN}$. These inputs are sampled by an internal synchronizer at each falling edge of CLK. The output of the synchronizer is then sampled when PCLK is HIGH. If the synchronizer resolved both the $\overline{ARDY}$ and $\overline{ARDYEN}$ as active, the $\overline{SRDY}$ and $\overline{SRDYEN}$ inputs are ignored. Either $\overline{ARDY}$ or $\overline{ARDYEN}$ must be HIGH at the end of T_S (see Figure 7).

$\overline{READY}$ remains active until either $\overline{S0}$ or $\overline{S1}$ are sampled LOW, or the ready inputs are sampled as inactive.

Figure 6. Synchronous $\overline{\text{READY}}$ Operation

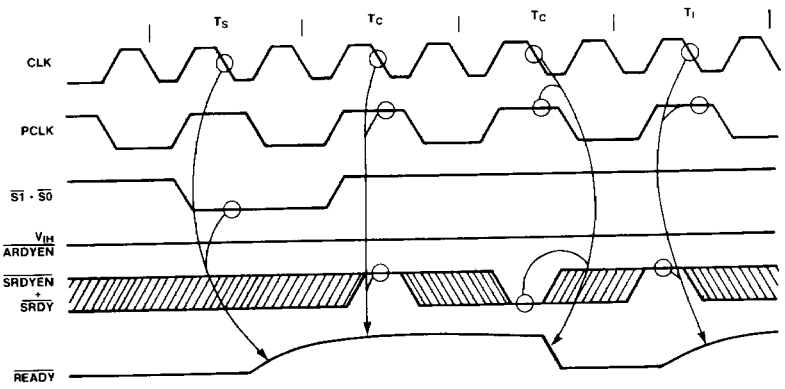
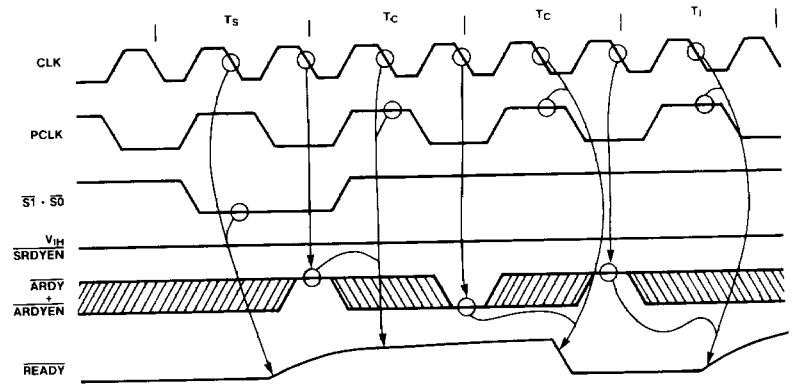


Figure 7. Asynchronous $\overline{\text{READY}}$ Operation



Absolute Maximum Ratings*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
All Output and Supply Voltages ..... -0.5V to +7V
All Input Voltages ..... -1.0V to +5.5V
Power Dissipation ..... 1 Watt

***Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

DC Characteristics (T_{CASE} = 0°C to +85°C,* V_{CC} = 5V ± 5%)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IHR}	$\overline{RES}$ and EFI Input HIGH Voltage		2.6		V
V_{HYS}	$\overline{RES}$ Input Hysteresis		0.25		V
V_{OL}	RESET, PCLK Output LOW Voltage	I_{OL} = 5 mA		0.45	V
V_{OH}	RESET, PCLK Output HIGH Voltage	I_{OH} = -1 mA	2.4		V
		I_{OH} = -0.2 mA	V_{CC}-0.5		V
V_{OLR}	$\overline{READY}$, Output LOW Voltage	I_{OL} = 9 mA		0.45	V
V_{OLC}	CLK Output LOW Voltage	I_{OL} = 5 mA		0.45	V
V_{OHC}	CLK Output HIGH Voltage	I_{OH} = -800 μA	4.0		V
I_{IL}	Input Sustaining Current on $\overline{S0}$ and $\overline{S1}$ Pins	V_{IN} = 0V	30	500	μA
I_{LI}	Input Leakage Current	$0 \leq V_{IN} \leq V_{CC}$ (1)		±10	μA
I_{CC}	Power Supply Current	at 32 MHz Output CLK Frequency		75	mA
C_I	Input Capacitance	F_C = 1 MHz		10	pF

*T_A is guaranteed from 0°C to +70°C as long as T_{CASE} is not exceeded.

Note:
1. Status lines $\overline{S0}$ and $\overline{S1}$ excluded because they have internal pull-up resistors.

AC CHARACTERISTICS (V_{CC} = 5V ± 5%, T_{CASE} = 0°C to +85°C*)

Timing are referenced to 0.8V and 2.0V points of signals as illustrated in the datasheet waveforms, unless otherwise noted.

82C284 AC Timing Parameters

No.	Parameter	Test Conditions	8.0 MHz		10.0 MHz		12.5 MHz Preliminary		16.0 MHz Preliminary		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
1	EFI to CLK Delay	At 1.5V[1]		25		25		25		25	ns
2	EFI LOW Time	At 1.5V[1, 7]	28		22.5		13		10		ns
3	EFI HIGH Time	At 1.5V[1, 7]	28		22.5		22		17		ns
4	CLK Period		62	500	50	500	40	500	62	500	ns
5	CLK LOW Time	At 1.0V[1, 2, 7, 8, 9, 10]	15		12		11		9		ns
6	CLK HIGH Time	At 3.6V[1, 2, 7, 8, 9, 10]	25		16		13		10		ns
7	CLK Rise Time	1.0V to 3.6V[1, 2, 10, 11]		10		8		8		6	ns
8	CLK Fall Time	3.6V to 1.0V[1, 9, 10, 11]		10		8		8		6	ns
9	Status Setup Time	(Note 1)	22		—		—		—		ns
9a	Status Setup Time for Status Going Active	(Note 1)	—		20		22		18		ns
9b	Status Setup Time for Status Going Inactive	(Note 1)	—		20		18		14		ns
10	Status Hold Time	(Note 1)	1		1		3		3		ns
11	$\overline{SRDY}$ or $\overline{SRDYEN}$ Setup Time	(Note 1)	17		15		15		12		ns
12	$\overline{SRDY}$ or $\overline{SRDYEN}$ Hold Time	(Notes 1, 11)	0		0		0		0		ns
13	$\overline{ARDY}$ or $\overline{ARDYEN}$ Setup Time	(Notes 1, 3)	0		0		0		0		ns
14	$\overline{ARDY}$ or $\overline{ARDYEN}$ Hold Time	(Notes 1, 3)	30		30		25		20		ns
15	$\overline{RES}$ Setup Time	(Notes 1, 3)	20		20		18		15		ns
16	$\overline{RES}$ Hold Time	(Notes 1, 3)	10		10		8		6		ns
17	$\overline{READY}$ Inactive Delay	At 0.8V[4]	5		5		5		5		ns
18	$\overline{READY}$ Active Delay	At 0.8V[4]	0	24	0	24	0	18	0	15	ns
19	PCLK Delay	(Note 5)	0	45	0	35	0	23	0	18	ns
20	RESET Delay	(Note 5)	5	34	5	27	3	22	3	17	ns
21	PCLK LOW Time	(Notes 5, 6)	t4-20		t4-20		t4-20		t4-20		ns
22	PCLK HIGH Time	(Notes 5, 6)	t4-20		t4-20		t4-20		t4-20		ns

*T_A is guaranteed from 0°C to 70°C as long as T_{CASE} is not exceeded.

Notes:

1. CLK loading: C_L = 100 pF. The 82C284's X_1 and X_2 inputs are designed primarily for parallel-resonant crystals. Serial-resonant crystals may also be used, however, they may oscillate up to 0.01% faster than their nominal frequencies when used with the 82C284. For either type of crystal, capacitive loading should be as specified by Table 2.

Notes:

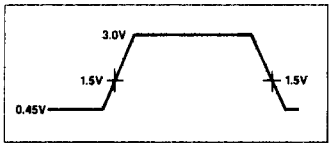
2. With the internal crystal oscillator using recommended crystal and capacitive loading; or with the EFI input meeting specifications t2 and t3. The recommended crystal loading for CLK frequencies of 8 MHz-20 MHz are 25 pF from pin X_1 to ground, and 15 pF from pin X_2 to ground; for CLK frequencies above 20 MHz 15 pF from pin X_1 to ground, and 15 pF from pin X_2 to ground. These recommended values are ±5 pF and include all stray capacitance. Decouple V_{CC} and GND as close to the 82C284 as possible.
3. This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at specific CLK edge.
4. Pull-up resistor values for READY pin:

CPU Frequency	8 MHz	10 MHz	12.5 MHz	16.0 MHz
Resistor	910Ω	700Ω	600Ω	560Ω
C_L	150 pF	150 pF	150 pF	150 pF
I_{OL}	7 mA	7 mA	9 mA	9 mA

5. PCLK and RESET loading: C_L = 75 pF
6. t4 refers to any allowable CLK period.
7. When driving the 82C284 with EFI, provide minimum EFI HIGH and LOW times as follows:

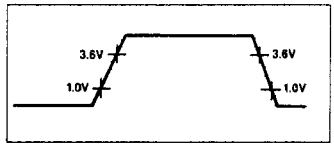
CLK Output Frequency	16 MHz	20 MHz	25 MHz	32 MHz
Min. Required EFI HIGH Time	28 ns	22.5 ns	22 ns	20 ns
Min. Required EFI LOW Time	28 ns	22.5 ns	13 ns	10 ns

Reset Drive EFI Drive and Measurement Points



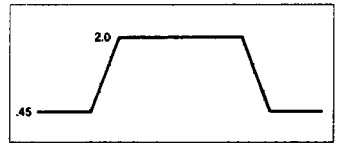
Note 9

CLK Output Measurement Points



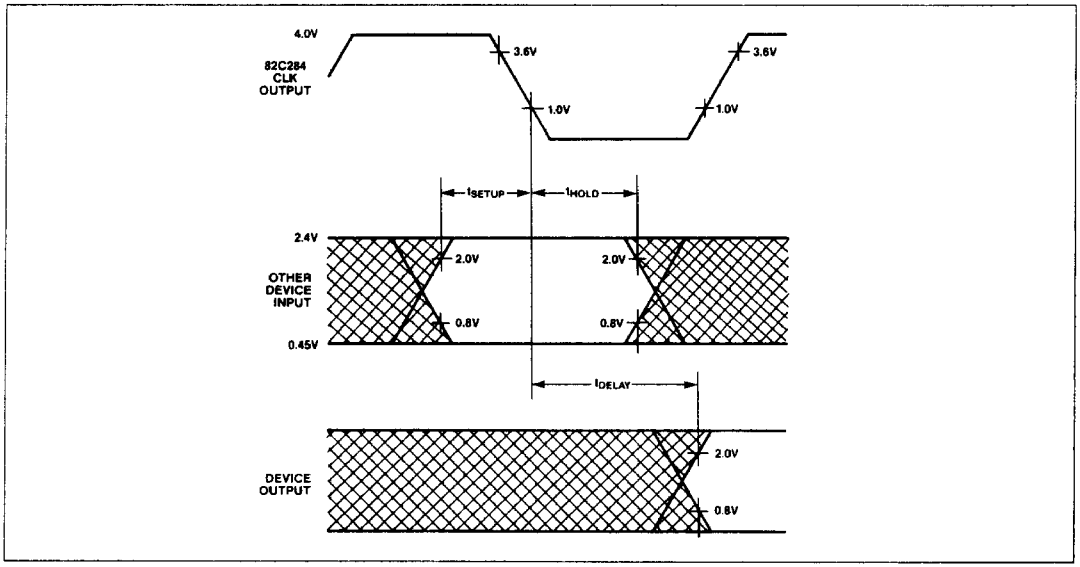
Note 10

F/$\overline{C}$ Drive Points



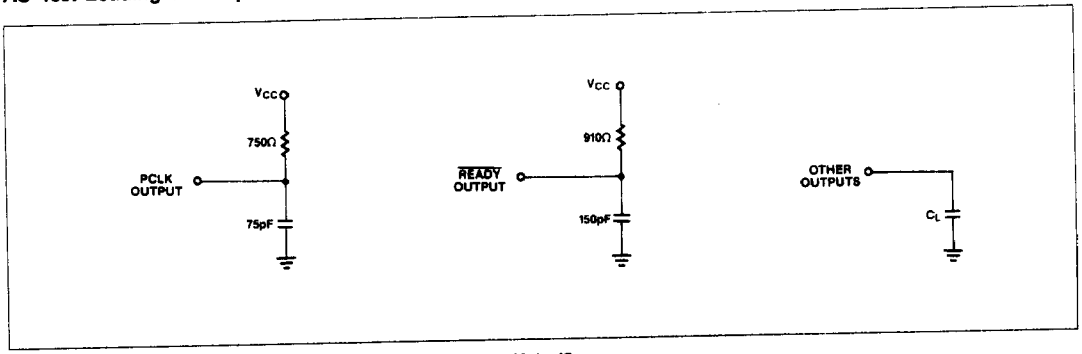
Note 11

AC Setup, Hold and Delay Time Measurement — General



Note 12

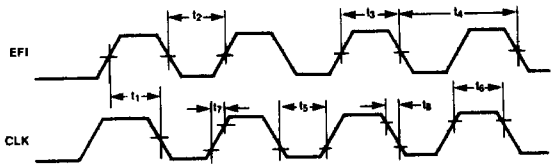
AC Test Loading on Outputs



Note 13

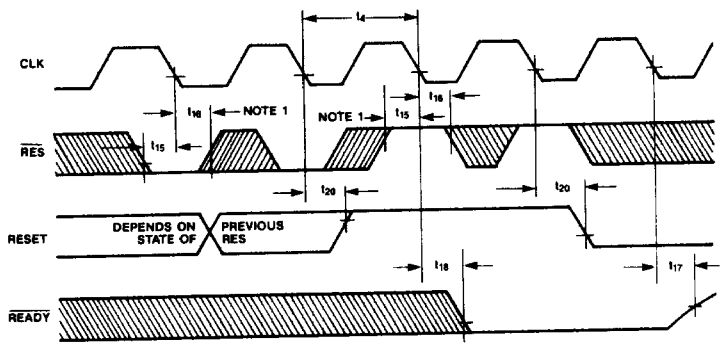
WAVEFORMS

CLK as a Function of EFI



Note:
The EFI input LOW and HIGH times as shown are required to guarantee the CLK LOW and HIGH times shown.

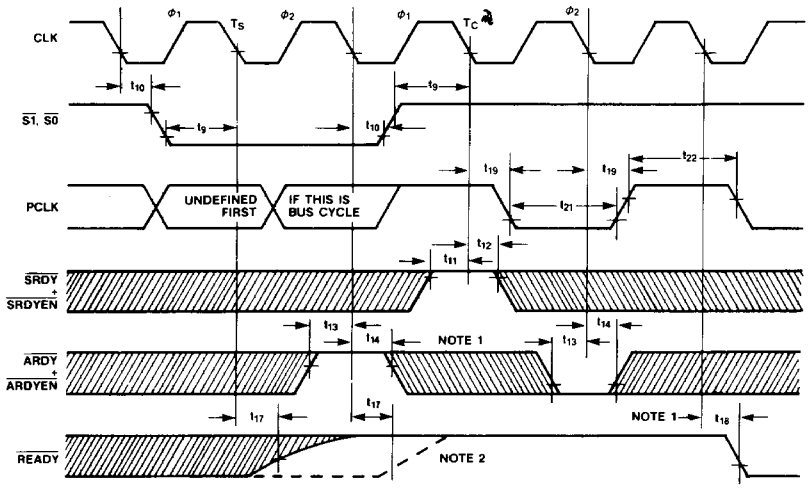
RESET and $\overline{\text{READY}}$ Timing as a Function of $\overline{\text{RES}}$ with $\overline{\text{S1}}$, $\overline{\text{S0}}$, $\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$, and $\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ High



Note:
1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

WAVEFORMS (Continued)

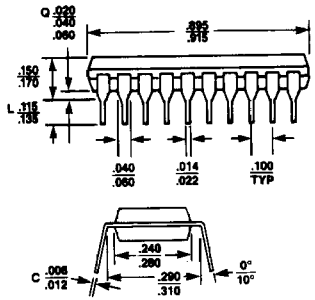
$\overline{\text{READY}}$ and PCLK Timing with $\overline{\text{RES}}$ High



Notes:

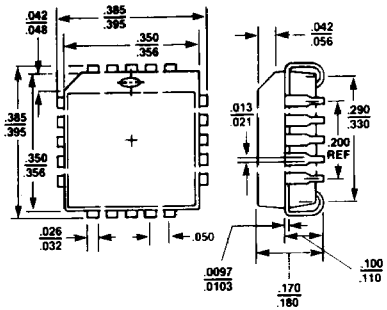
1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
2. If $\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ or $\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ are active before and/or during the first bus cycle after RESET, READY may not be deasserted until the falling edge of $\phi 2$ of T_S.

PACKAGE DIMENSIONS



ALL DIMENSIONS IN INCHES

18-pin DIP



20-pin PLCC

ORDERING INFORMATION AND PRODUCT CODE

KS 82C284 X X X

SAMSUNG SEMICONDUCTOR

Part Number

Speed

-8.0	8.0MHz
-10.0	10.0MHz
-12.5	12.5MHz
-16.0	16.0MHz

Packaging
P — Plastic DIP
L — Plastic Leaded Chip Carrier (PLCC)

Temperature
C — Commercial (0°C to +70°C)
I — Industrial (-40°C to +85°C)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Product Group.