T-51-09-90

MP7610

Micro Power Systems

Octal 14-Bit DAC Array™ Digital-to-Analog Converter with Output Amplifier and Serial Data/Address µP Control Logic

FEATURES

- **Eight Independent 14-Bit DACs with Output Amplifiers**
- **Low Power 320 mW (typ.)**
- **Serial Digital Data and Address Port (3-Wire Standard)**
- **14-Bit Resolution, 12-Bit Accuracy**
- **Extremely Well Matched DACs**
- **Extremely Low Analog Ground Current (<60µA/Channel)**
- **±10 V Output Swing with ±11.4 V Supplies**
- **Zero Volt Output Preset (Data = 10 .. 00)**
- **Rugged Construction – Latch-Up Free**
- **Available in 28 pin, 346 mil SOIC & 400 mil PDIP**

APPLICATIONS

- **Data Acquisition Systems**
- **ATE**
- **Process Control**
- **Self-Diagnostic Systems**
- **Logic Analyzers**
- **Digital Storage Scopes**
- **PC Based Controller/DAS**

4

GENERAL DESCRIPTION

The MP7610 provides eight independent 14-bit resolution digital-to-analog converters with voltage output amplifiers and a 3-wire standard serial digital address and data port.

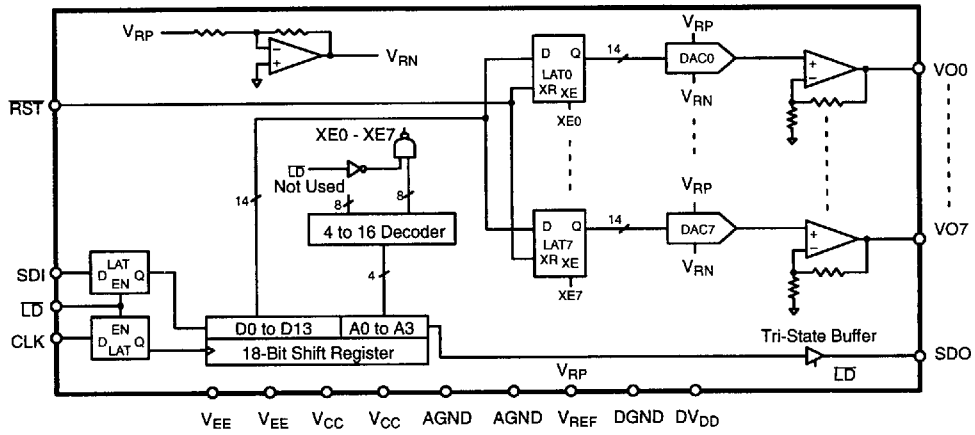
Typical DAC matching for C grade versions is 1.5 LSB across all codes. Accuracy of ±2 LSB for DNL and ±2 LSB for INL is also achieved for C grade. The output amplifier is capable of sinking and sourcing 5mA, and the output voltage settles to 12-bits in less than 30µs (typ.).

The MP7610 is equipped with a serial data (3-wire standard) µ-processor logic interface to reduce pin count, package size, and board space.

Built on Micro Power Systems advanced linear BiCMOS, these devices offer rugged solutions that are latch-up free, and take advantage of Micro Power Systems' patented thin-film resistor process which exhibits excellent long term stability and reliability.

Specified for operation over the commercial / industrial (–40 to +85°C) temperature range, the MP7610 is available Plastic dual-in-line (PDIP) and Surface Mount (SOIC) packages.

SIMPLIFIED BLOCK DIAGRAM



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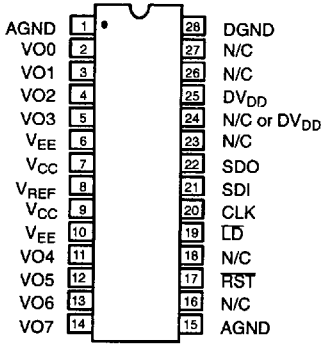
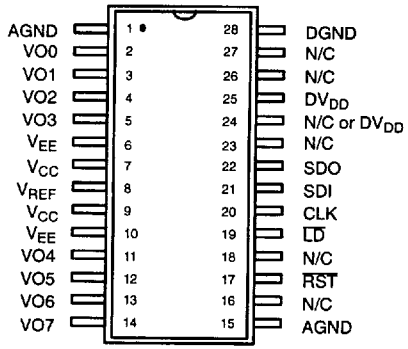
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	Res. (Bits)	INL (LSB)	DNL (LSB)	FSE (LSB)	CH/CH Match (LSB)
PDIP	–40 to +85°C	MP7610CN	14	±2	±2	±16	±1.5
PDIP	–40 to +85°C	MP7610BN	14	±4	±3	±24	±2.8
PDIP	–40 to +85°C	MP7610AN	14	±8	±4	±32	±4
SOIC	–40 to +85°C	MP7610CS	14	±2	±2	±16	±1.5
SOIC	–40 to +85°C	MP7610BS	14	±4	±3	±24	±2.8
SOIC	–40 to +85°C	MP7610AS	14	±8	±4	±32	±4

PIN CONFIGURATIONS



28 Pin PDIP (0.400")
NW28



28 Pin SOIC (Jedec, 0.346")
SW28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	AGND	Analog Ground
2	VO0	DAC 0 Output
3	VO1	DAC 1 Output
4	VO2	DAC 2 Output
5	VO3	DAC 3 Output
6	V_{EE}	Analog Negative Power Supply (–12 V)
7	V_{CC}	Analog Positive Power Supply (+12 V)
8	V_{REF}	Voltage Reference Input (+5 V)
9	V_{CC}	Analog Positive Power Supply (+12 V)
10	V_{EE}	Analog Negative Power Supply (–12 V)
11	VO4	DAC 4 Output
12	VO5	DAC 5 Output
13	VO6	DAC 6 Output
14	VO7	DAC 7 Output

PIN NO.	NAME	DESCRIPTION
15	AGND	Analog Ground
16	N/C	No Connection
17	$\overline{RST}$	Reset all DACs to 0 V Output
18	N/C	No Connection
19	$\overline{LD}$	Load Signal; Load Data to Selected DAC
20	CLK	Serial Data Clock
21	SDI	Serial Data Input
22	SDO	Shift Register Serial Output
23	N/C	No Connection
24	N/C	No Connection or DV_{DD}
25	DV_{DD}	Digital Positive Power Supply (+5 V)
26	N/C	No Connection
27	N/C	No Connection
28	DGND	Digital Ground

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MP7610

ELECTRICAL CHARACTERISTICS

V_{CC} = +12 V, V_{EE} = −12 V, V_{REF} = 5 V, DV_{DD} = 5.0 V, T = 25°C, Output Load = 5kΩ (unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE								
Resolution (All Grades)	N	14					Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec
A				±8		±8		
B				±4		±4		
C				±2		±2		
Differential Non-Linearity	DNL						LSB	
A				±4		±4		
B				±3		±3		
C				±2		±2		
Positive Full Scale Error	+FSE						LSB	
A			24	±32		±32		
B			16	±24		±24		
C			12	±16		±16		
Negative Full Scale Error	−FSE						LSB	
A			24	±32		±32		
B			16	±24		±24		
C			12	±16		±16		
Bipolar Zero Offset	ZOFS						LSB	
A				±8		±8		
B				±4		±4		
C				±3		±3		
Channel-to-Channel Maximum Error (All Codes)	ΔE						LSB	
A				±4		±4		
B				±2.8		±2.8		
C				±1.5		±1.5		
All Channels Maximum Error with DAC 0 adjusted to minimum error	ME						LSB	
A				±16		±16		
B				±8		±8		
C				±6		±6		
All Channels Maximum Error Span with DAC 0 adjusted to minimum error	MES						LSB	
A				±20		±20		
B				±8		±8		
C				±6		±6		

4

MP7610

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ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE								
Voltage Settling from $\overline{LD}$ to VDAC Out[1]	t_{sd}		30	50		50	µsec	ZS to FS (20 V Step) 5k, 50pF load
Channel-to-Channel Crosstalk[6]	CT		0.01				LSB	DC
Digital Feedthrough[1, 6]	Q		–70				dB	CLK and Data to V_{OUTi}
Power Supply Rejection Ratio	PSRR			5			ppm/%	ΔV_{EE} & ΔV_{CC} = ±5%, ppm of FS
REFERENCE INPUTS								
Impedance of V_{REF}	REF	350	700	1.05k	350	1.05k	Ω	See Application Hints for Driving the reference input
V_{REF} Voltage1, [2]	V_{REF}	3.5		6			V	
DIGITAL INPUTS[3]								
Logic High	V_{IH}	2.4					V	
Logic Low	V_{IL}			0.8			V	
Input Current	I_L			±10			µA	
Input Capacitance[1]	C_L			8			pF	
ANALOG OUTPUTS								
Output Swing		$-V_{EE}$ +1.4	V_{CC} –1.4				V	
Output Drive Current		–5		5			mA	
Output Impedance	R_O		1				Ω	
Output Short Circuit Current	I_{SC}		25				mA	+FS to AGND
			30				mA	+FS to V_{EE}
			40				mA	–FS to AGND
			55				mA	–FS to V_{CC}
DIGITAL OUTPUTS								
Output High Voltage	V_{OH}		4.5				V	
Output Low Voltage	V_{OL}		0.5				V	
POWER SUPPLIES								
V_{CC} Voltage[5]	V_{CC}	V_{REF}+1.5	12	12.75	V_{REF}+1.5	12.75	V	
V_{EE} Voltage[5]	V_{EE}	–12.75	–12	–5	–12.75	–5	V	
DV_{DD} Voltage	DV_{DD}	4.5	5	5.5	4.5	5.5	V	
Positive Supply Current	I_{CC}		8	10			mA	Bipolar zero
Negative Supply Current	I_{EE}		15	20			mA	Bipolar zero
Digital Supply Current	I_{DD}			1			mA	Bipolar zero
Power Dissipation	PD_{ISS}		320	420		450	mW	Bipolar zero
ANALOG GROUND CURRENT								
Per Channel[1]	I_{AGND}		±60				µA	See Application Notes
DIGITAL TIMING SPECIFICATIONS[1,4]								V_{IL} = 0, V_{IH} = 5.0, C_L = 20 pF
Input Clock Pulse Width	t_{CH}, t_{CL}	35					ns	
Data Setup Time	t_{DS}	15					ns	
Data Hold Time	t_{DH}	15					ns	
CLK to SDO Propagation Delay	t_{PD}			40			ns	
DAC Register Load Pulse Width	t_{LD}	35					ns	
Preset Pulse Width	t_{PR}	50					ns	

Micro Power Systems

MP7610

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL TIMING SPECIFICATIONS[1, 4] (CONT'D)								
Clock Edge to Load Time	t_{CKLD1} t_{CKLD2}	140 0					ns	Note: t_{LD} and t_{CKLD2} cannot both be min. since $t_{CKLD1}=t_{CKLD2}+t_{LD}$
$\overline{LD}$ Falling Edge to SDO Tri-state Enable	t_{HZ1}	50					ns	
$\overline{LD}$ Rising Edge to SDO Tri-state Disable	t_{HZ2}	50					ns	
$\overline{LD}$ Rising Edge to CLK Enable	t_{LDCK}	50					ns	
$\overline{LD}$ Set-up Time with Respect to CLK	t_{LDSU}	30					ns	

NOTES:

(1) Guaranteed; not tested.
(2) Specified values guarantee functionality.
(3) Digital inputs should not go below ground or exceed positive supply voltage.
(4) *See Figures 2 and 3.* All digital input signals are specified with $t_R = t_F = 10$ ns 10% to 90% and timed from a 50% voltage level.
(5) For power supply values < $\pm 2 * V_{REF}$, the output swing is limited as specified in Analog Outputs.
(6) Digital feedthrough and channel-to-channel crosstalk are heavily dependent on the board layout and environment.

Specifications are subject to change without notice

4

ABSOLUTE MAXIMUM RATINGS (1, 2) (TA = +25°C unless otherwise noted)

V_{CC} to AGND ..... +16.5 V
V_{EE} to AGND ..... –16.5 V
DV_{DD} to DGND ..... +6.5 V
AGND to DGND ..... ±1 V
(Functionality guaranteed for ±0.5 V only)
Digital Input & Output Voltage to DGND –0.5 to DV_{DD} +0.5V
Analog Inputs & Outputs ..... Indefinite Shorts to V_{CC}, V_{EE}, DV_{DD}, AGND, DGND (provided that power dissipation of the package spec is not exceeded)

Operating Temperature Range
Extended Industrial ..... –40°C to +85°C
Maximum Junction Temperature ..... –65°C to 150°C
Storage Temperature ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation Rating @ 75°C
SOIC, PDIP 1150mW
Derates above 75°C ..... 15mW/°C

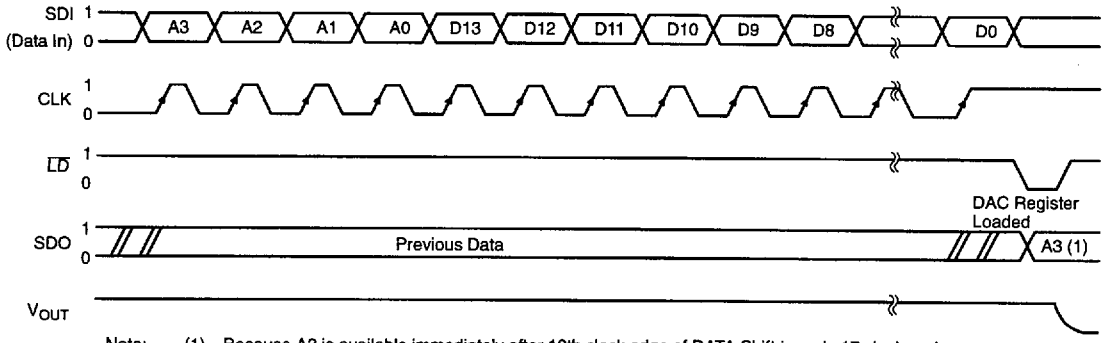
NOTES:

(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
(2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

APPLICATION NOTES

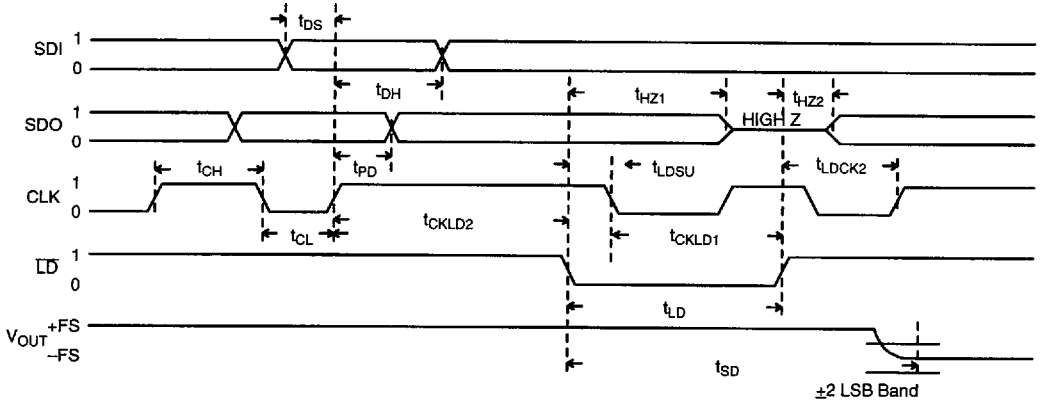
Refer to Section 8 for Applications Information

NOTE: When using these DACs to drive remote devices, the accuracy of the output can be improved by utilizing a remote analog ground connection. The difference between the DGND and AGND should be limited to ±300 mV to assure normal operation. If there is any chance that the AGND to DGND can be greater than ±1 V, we recommend two back-to-back diodes be used between DGND and AGND to clamp the voltage and prevent damage to the DAC. Using a buffer between the remote ground location and AGND may help reduce noise induced from long lead or trace lengths.



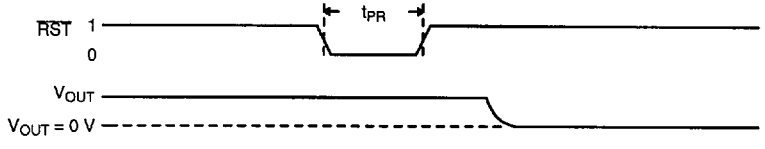
Note: (1) Because A3 is available immediately after 18th clock edge of DATA Shift-in, only 17 clock cycles are needed to complete the readback.

Figure 1. Serial Data Timing and Loading



Note: (1) CLK should be high during the falling edge of $\overline{LD}$ to insure proper function of the shift register.

Figure 2. Serial Data Input Timing ($\overline{RST}$ = "1")



Note: Reset settling time is ≤t_{SD}

Figure 3. Reset Operation

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MP7610

The MP7610 is equipped with a serial data (3-wire standard) µ-processor logic interface to reduce pin count, package size, and board wire (space). If the $\overline{LD}$ signal is high, the CLK signal loads the digital input bits (SDI) into the shift register (4 bits address A3 to A0 plus 14 bits data D13 to D0 for the MP7610). The $\overline{LD}$ signal going low loads the data into the selected DAC. The $\overline{LD}$ signal going low also disables the serial data (SDI), output (SDO tri-stated) and the CLK input. This design tremendously reduces digital noise and glitch transients into the DACs due to free running CLK and SDI. Note also that the preset signal ($\overline{RST}$) resets all analog outputs to 0 volt regardless of digital inputs.

Function	A3	A2	A1	A0	$\overline{LD}$	CLK	$\overline{RST}$	SDI	SDO
Shift Data In and Out	X	X	X	X	1	0→1 Repeat	1	Data Input Valid	Data Output Valid
Stop Shifting Data In and Out	X	X	X	X	0	X	1	X	Hi-Z
Load DACs	0	0	0	0	No Operation				
DAC 0	0	0	0	1	1→0	X	1	X	Hi-Z
DAC 1	0	0	1	0	1→0	X	1	X	Hi-Z
DAC 2	0	0	1	1	1→0	X	1	X	Hi-Z
DAC 3	0	1	0	0	1→0	X	1	X	Hi-Z
DAC 4	0	1	0	1	1→0	X	1	X	Hi-Z
DAC 5	0	1	1	0	1→0	X	1	X	Hi-Z
DAC 6	0	1	1	1	1→0	X	1	X	Hi-Z
DAC 7	1	0	0	0	1→0	X	1	X	Hi-Z
⋮	⋮	⋮	⋮	⋮	No Operation	X	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	X	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	X	⋮	⋮	⋮
⋮	1	1	1	0	No Operation	X	1	X	Hi-Z
⋮	1	1	1	1	No Operation	X	1	X	Hi-Z
Reset all DACs to 0 V	X	X	X	X	X	X	0	X	X

Table 1. Digital Function Truth Table
Serial In/Serial Out

Note: For timing information See Electrical Characteristics.

Hex Code	Binary Code	Output Voltage = $2 \bullet Vr\left(-1 + \frac{2 \bullet D}{16384}\right)$ (Vr = +5 V)
0 0 0 0	00000000000000	$10 \bullet (-1 + 0) = -10$
⋮	⋮	⋮
1 F F F	01111111111111	$10 \bullet \left(-1 + \frac{16382}{16384}\right) = -1.22$ mV
2 0 0 0	10000000000000	$10 \bullet \left(-1 + \frac{16384}{16384}\right) = 0$
2 0 0 1	10000000000001	$10 \bullet \left(-1 + \frac{16386}{16384}\right) = 1.22$ mV
⋮	⋮	⋮
3 F F F	11111111111111	$10 \bullet \left(-1 + \frac{32766}{16384}\right) = 9.99878$

Table 2. MP7610
Ideal DAC Output vs. Input Code
(Two's Complement Architecture)

Note: See Electrical Characteristics for real system accuracy

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SERIAL INTERFACE DIAGRAMS

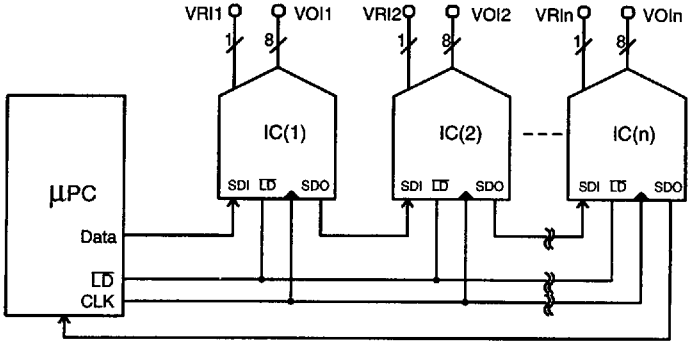


Figure 4. Simplified Diagram

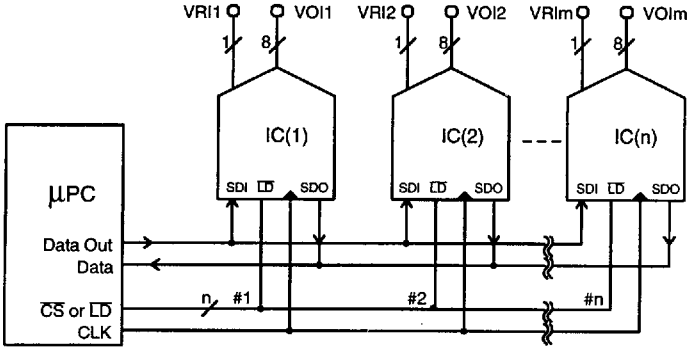


Figure 5. Simplified Diagram

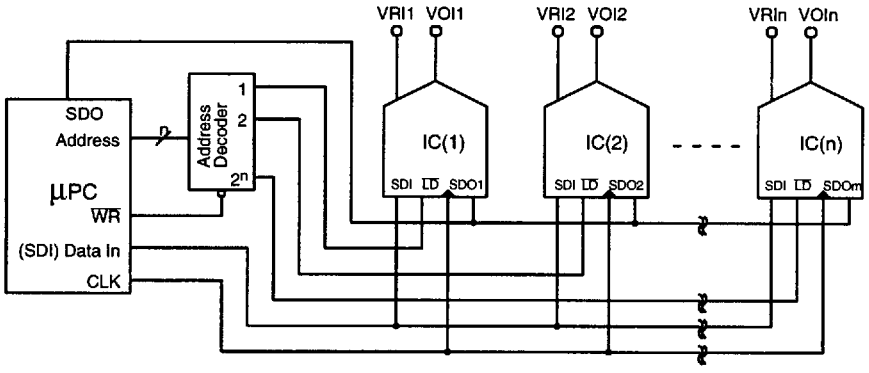
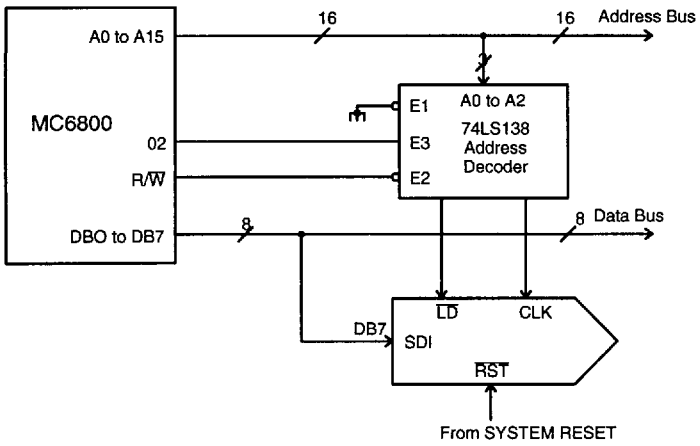
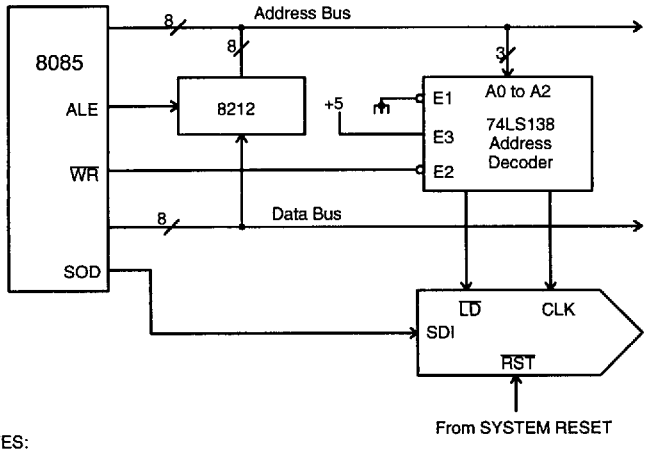


Figure 6. Simplified Diagram



NOTES
1. Execute consecutive memory write instructions while manipulating the data between WRITEs so that each WRITE presents the next bit.
2. The serial data loading is triggered by the CLK pulse which is asserted by a decoded memory WRITE to memory location 2000, R/W, and 02. A WRITE to address 4000 transfers data from input shift register to DAC register.

Figure 7. MC6800 Interface



NOTES:
1. Clock generated by $\overline{WR}$ and decoding address 8000.
2. Data is clocked in the DAC shift register by executing memory write instructions. The clock input is generated by decoding address 8000 and WR. Data is then loaded into the DAC register with a memory write instruction to address 4000.
3. Serial data must be present in the right justified format in registers H & L of the microprocessor.

Figure 8. 8085 Interface

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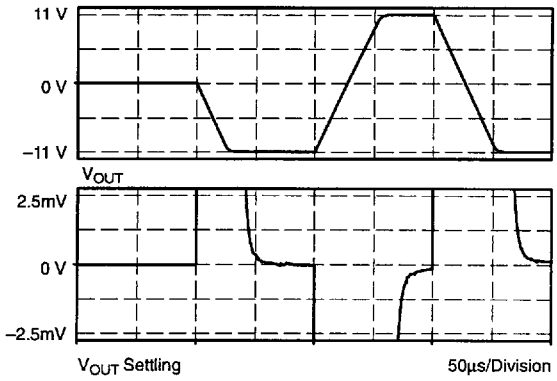
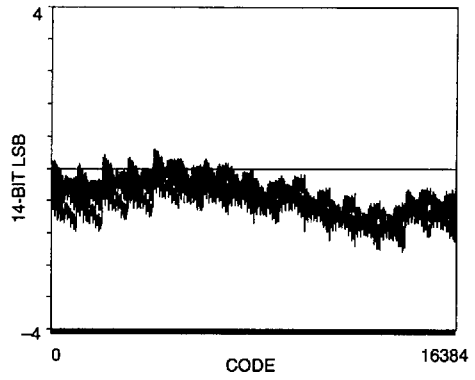
PERFORMANCE CHARACTERISTICS



Graph 1. Typical Output Settling Characteristic
V_{REF} = 5 V, R_L = 5K, C_L = 500pF

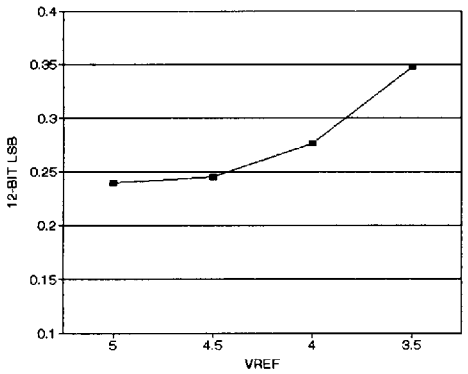
Graph 1 shows the typical output settling characteristic of the MP7610 Family for a RESET →ZS→FS→ZS series of code transitions. The top graph shows the output voltage transients, while the bottom graph shows the difference between the output and the ideal output.



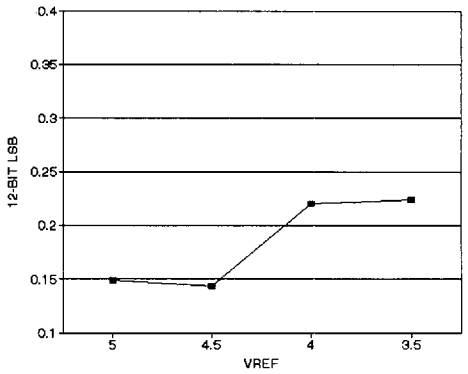
Graph 2. Linearity with
V_{REF} = 5 V, All DACs, All Codes

Micro Power Systems

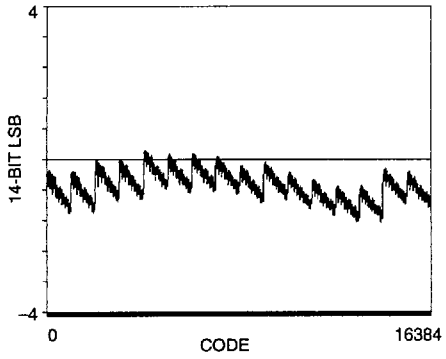
MP7610



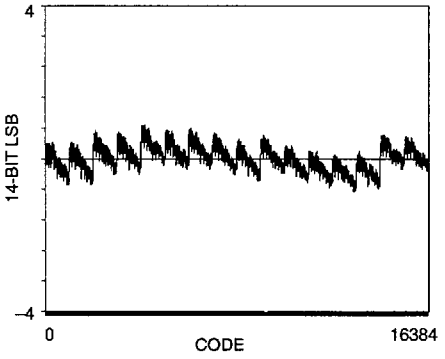
Graph 3. DAC 0 INL vs. V_{REF}



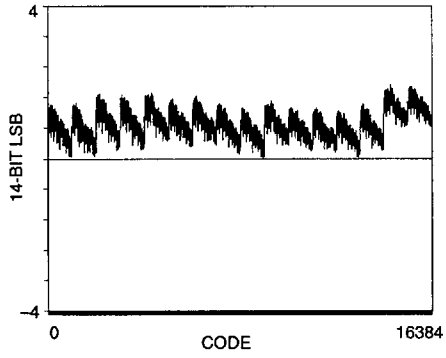
Graph 4. DAC 0 DNL vs. V_{REF}



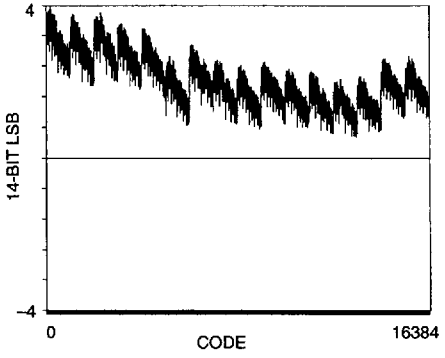
Graph 5. DAC 0 Linearity with V_{REF} = 5 V, V_{OUT} = ±10



Graph 6. DAC 0 Linearity with V_{REF} = 4.5 V, V_{OUT} = ±9



Graph 7. DAC 0 Linearity with V_{REF} = 4 V, V_{OUT} = ±8



Graph 8. DAC 0 Linearity with V_{REF} = 3.5 V, V_{OUT} = ±7

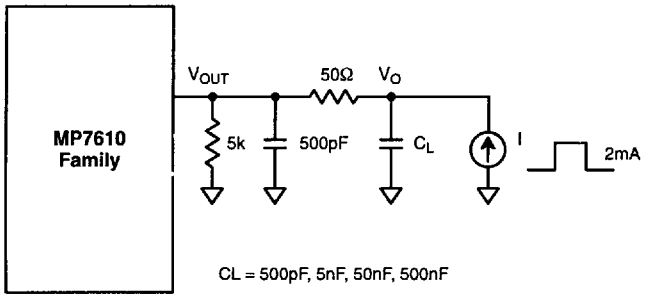
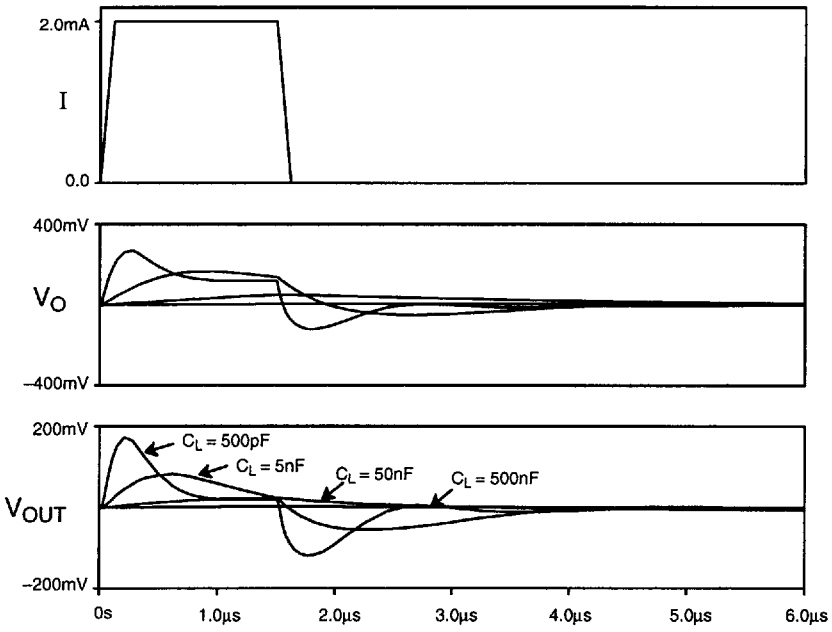


Figure 9. Circuit for Determining Typical Analog Output Pulse Response



Graph 9. Typical Response of the MP7610 Family Analog Output to a Current Pulse with CL=500pF, 5nF, 50nF, 500nF
(See Figure 9. above)