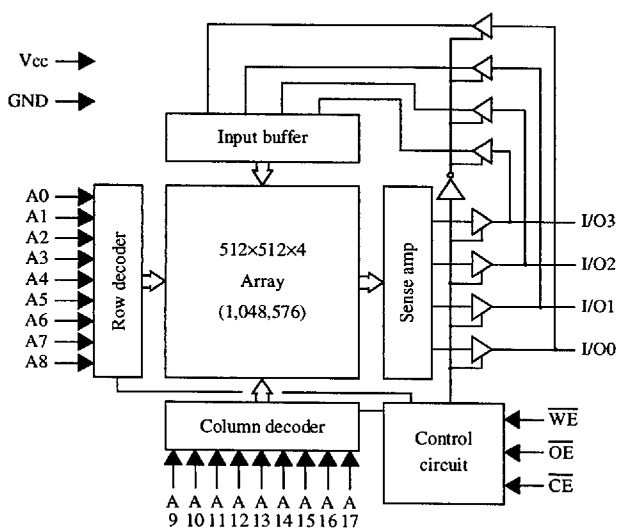
256K×4 CMOS SRAM

Features

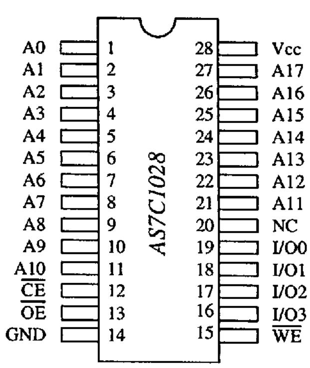
- Organization: 262,144 words × 4 bits
- High speed
  - 12/15/20/25/35 ns address access time
  - 4/4/5/6/8 ns output enable access time
- Low power consumption
  - Active: 660 mW max (15 ns cycle)
  - Standby: 27.5 mW max, CMOS I/O
    5.5 mW max, CMOS I/O, L version
  - Very low DC component in active power
- 2.0V data retention (L version)
- Equal access and cycle times
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- 28-pin JEDEC standard packages
  - 300 mil PDIP and SOJ
  - 400 mil PDIP and SOJ
- ESD protection > 2000 volts
- Latch-up current > 200 mA

Logic block diagram



Pin arrangement

DIP, SOJ



Selection guide

		7C1028-12	7C1028-15	7C1028-20	7C1028-25	7C1028-35	Unit
Maximum address access time		12	15	20	25	35	ns
Maximum output enable access time		4	4	5	6	8	ns
Maximum operating current		130	120	110	100	80	mA
Maximum CMOS standby current		5.0	5.0	5.0	5.0	5.0	mA
	L	1.0	1.0	1.0	1.0	1.0	mA

Shaded areas contain advance information.

Functional description

The AS7C1028 is a high performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) organized as 262,144 words × 4 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 12/15/20/25/35 ns with output enable access times (t_{OE}) of 4/4/5/6/8 ns are ideal for high performance applications. A chip enable ($\overline{CE}$) input permits easy memory expansion with multiple-bank memory organizations.

When $\overline{CE}$ is HIGH the device enters standby mode. The standard AS7C1028 is guaranteed not to exceed 27.5 mW power consumption in standby mode; the L version is guaranteed not to exceed 5.5 mW, and typically requires only 800 µW. The L version also offers 2.0V data retention, with maximum power consumption in this mode of 600 µW.

A write cycle is accomplished by asserting chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) LOW. Data on the input pins I/O0-I/O3 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW, with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When chip enable or output enable is HIGH, or write enable is LOW, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5V supply. The AS7C1028 is packaged in high volume industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on any pin relative to GND	V_t	–0.5	+7.0	V
Power dissipation	P_D	–	1.0	W
Storage temperature (plastic)	T_{stg}	–55	+150	°C
Temperature under bias	T_{bias}	–10	+85	°C
DC output current	I_{out}	–	20	mA

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	High Z	Output Disable
L	H	L	D_{out}	Read
L	L	X	D_{in}	Write

Key: X = Don't Care, L = LOW, H = HIGH

Recommended operating conditions

(T_a = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input voltage	V_{IH}	2.2	–	V_{CC}+1	V
	V_{IL}	–0.5†	–	0.8	V

† V_{IL} min = –3.0V for pulse width less than $t_{RC}/2$

DC operating characteristics[1]

(V_{CC} = 5V±10%, GND = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	Test Conditions		-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	-25 Min	-25 Max	-35 Min	-35 Max	Unit
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = Max, V_{in} = GND to V_{CC}		–	1	–	1	–	1	–	1	–	1	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE}$ = V_{IH}, V_{CC} = Max, V_{out} = GND to V_{CC}		–	1	–	1	–	1	–	1	–	1	µA
Operating power supply current	I_{CC}	$\overline{CE}$ = V_{IL}, f = f_{max}, I_{out} = 0 mA		–	130	–	120	–	110	–	100	–	80	mA
			L	–	125	–	115	–	105	–	95	–	75	mA
Standby power supply current	I_{SB}	$\overline{CE}$ = V_{IH}, f = f_{max}		–	50	–	40	–	40	–	35	–	30	mA
			L	–	45	–	35	–	35	–	30	–	25	mA
	I_{SB1}	$\overline{CE}$ > V_{CC}–0.2V, f = 0, V_{in} ≤ 0.2V or V_{in} ≥ V_{CC}–0.2V		–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	mA
			L	–	1.0	–	1.0	–	1.0	–	1.0	–	1.0	mA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min		–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min		2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	V

Capacitance[2]

(f = 1 MHz, T_a = Room Temperature, V_{CC} = 5V)

Parameter	Symbol	Signals	Test Conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{in} = V_{out} = 0V	7	pF

Key to switching waveforms

Rising input   Falling input   Undefined output/don't care

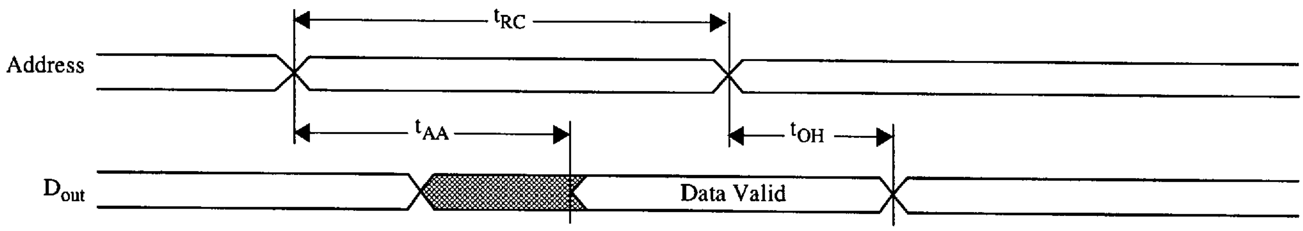
Read cycle[3,9]

(V_{CC} = 5V±10%, GND = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	-25 Min	-25 Max	-35 Min	-35 Max	Unit	Notes
Read cycle time	t_{RC}	12	–	15	–	20	–	25	–	35	–	ns	
Address access time	t_{AA}	–	12	–	15	–	20	–	25	–	35	ns	3
Chip enable ($\overline{CE}$) access time	t_{ACE}	–	12	–	15	–	20	–	25	–	35	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	–	3	–	4	–	5	–	6	–	8	ns	
Output hold From address change	t_{OH}	3	–	3	–	3	–	3	–	3	–	ns	5
Chip enable to output in Low Z	t_{CLZ}	3	–	3	–	3	–	3	–	3	–	ns	4, 5
Chip disable to output in High Z	t_{CHZ}	–	3	–	4	–	5	–	6	–	8	ns	4, 5
Output enable to output in Low Z	t_{OLZ}	0	–	0	–	0	–	0	–	0	–	ns	4, 5
Output disable to output in High Z	t_{OHZ}	–	3	–	4	–	5	–	6	–	8	ns	4, 5
Chip enable to power up time	t_{PU}	0	–	0	–	0	–	0	–	0	–	ns	4, 5
Chip Disable to power down time	t_{PD}	–	12	–	15	–	20	–	25	–	35	ns	4, 5

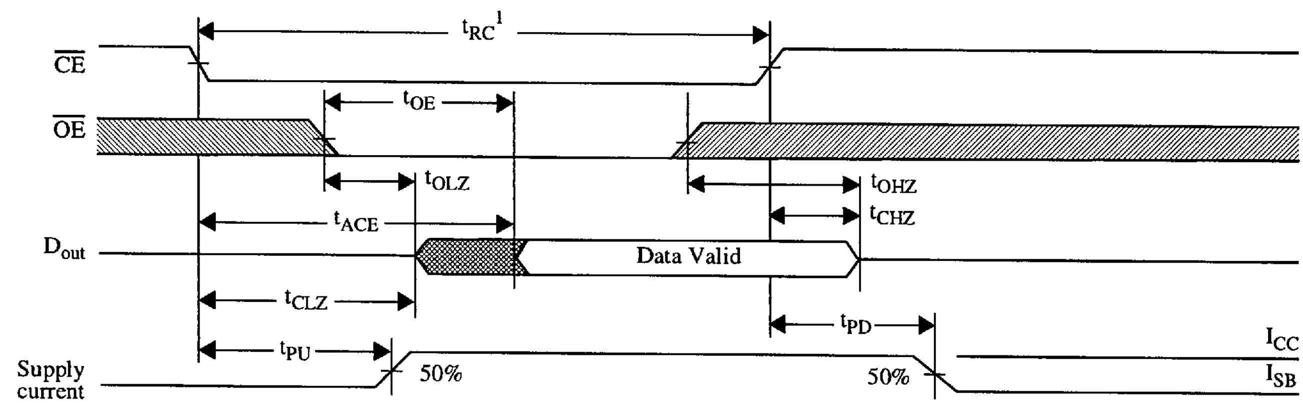
Read waveform 1[3,6,7,9]

Address controlled



Read waveform 2[3,6,8,9]

CE controlled



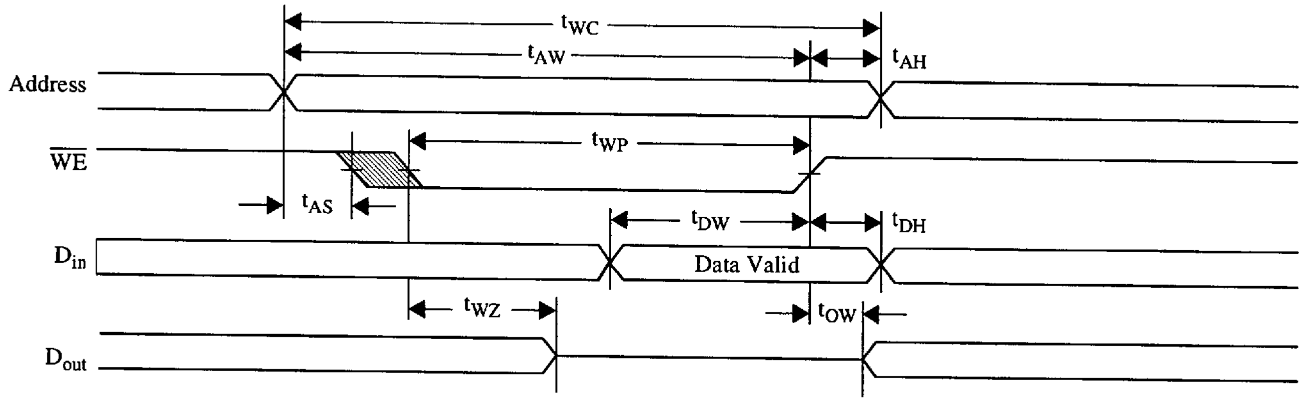
Write cycle[11]

(V_{CC} = 5V±10%, GND = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	-25 Min	-25 Max	-35 Min	-35 Max	Unit	Notes
Write cycle time	t_{WC}	12	–	15	–	20	–	20	–	30	–	ns	
Chip enable to write end	t_{CW}	10	–	10	–	12	–	15	–	20	–	ns	
Address setup to write end	t_{AW}	10	–	10	–	12	–	15	–	20	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	0	–	ns	
Write pulse width	t_{WP}	8	–	9	–	12	–	15	–	17	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	8	–	9	–	10	–	10	–	15	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	0	–	ns	4, 5
Write enable to output in High Z	t_{WZ}	–	5	–	5	–	5	–	5	–	5	ns	4, 5
Output active from write end	t_{OW}	3	–	3	–	3	–	3	–	3	–	ns	4, 5

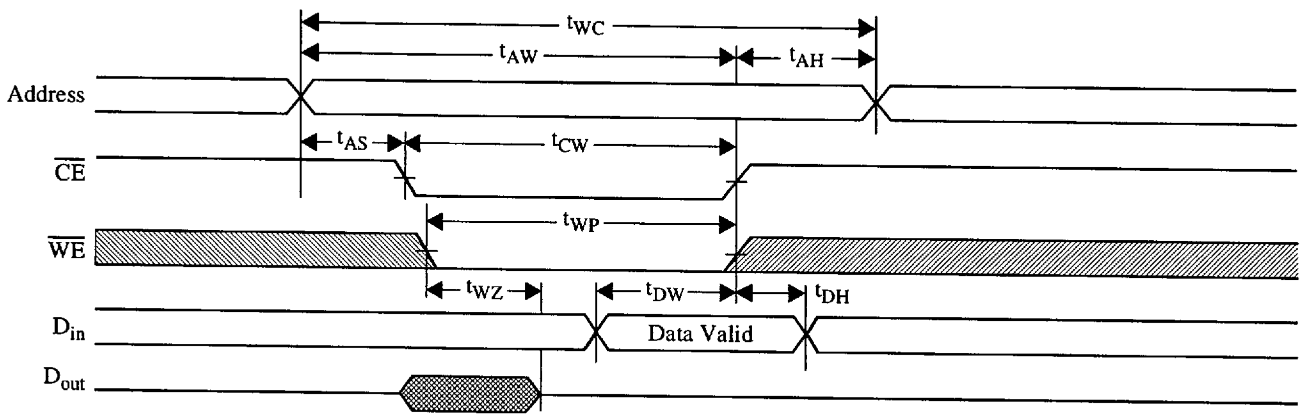
Write waveform 1 [10,11]

$\overline{WE}$ controlled



Write waveform 2 [10,11]

$\overline{CE}$ controlled



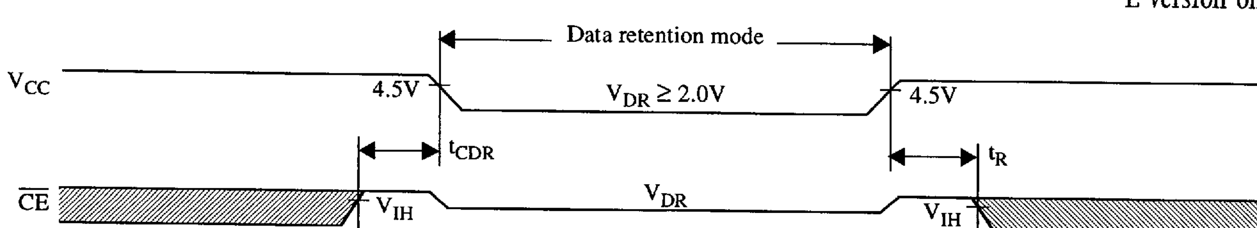
Data retention characteristics

L version only

Parameter	Symbol	Test Conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	$V_{CC} = 2.0V$	2.0	–	V
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{CC}-0.2V$	–	300	µA
Chip deselect to data retention time	t_{CDR}		0	–	ns
Operation recovery time	t_R	$V_{in} \geq V_{CC}-0.2V$ or	t_{RC}	–	ns
Input leakage current	$\lvert I_{LI} \rvert$	$V_{in} \leq 0.2V$	–	1	µA

Data retention waveform

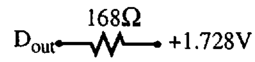
L version only



AC test conditions

- Output load: see Figure B, except for t_{CLZ} and t_{CHZ} see Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

Thevenin Equivalent:



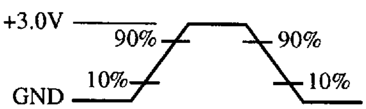


Figure A: Input Waveform

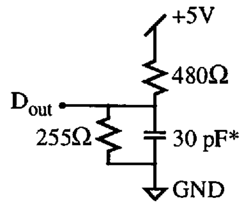
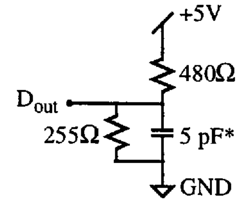


Figure B: Output Load



*including scope and jig capacitance

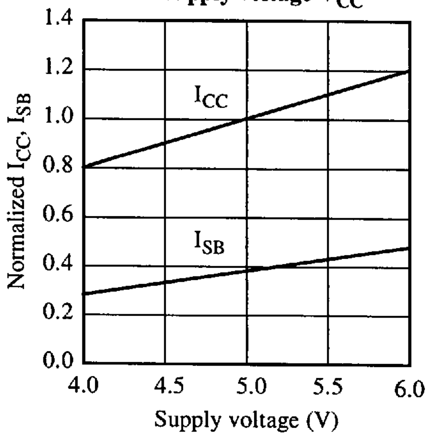
Figure C: Output Load for t_{CLZ}, t_{CHZ}

Notes

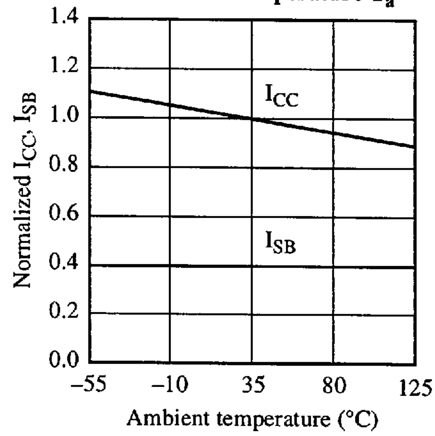
1. During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2. This parameter is sampled and not 100% tested.
3. For test conditions, see *AC Test Conditions*, Figures A, B, C.
4. t_{CLZ} and t_{CHZ} are specified with CL = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5. This parameter is guaranteed but not tested.
6. $\overline{WE}$ is HIGH for read cycle.
7. $\overline{CE}$ and $\overline{OE}$ are LOW for read cycle.
8. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
9. All read cycle timings are referenced from the last valid address to the first transitioning address.
10. $\overline{CE}$ or $\overline{WE}$ must be HIGH during address transitions.
11. All write cycle timings are referenced from the last valid address to the first transitioning address.

Typical DC and AC characteristics

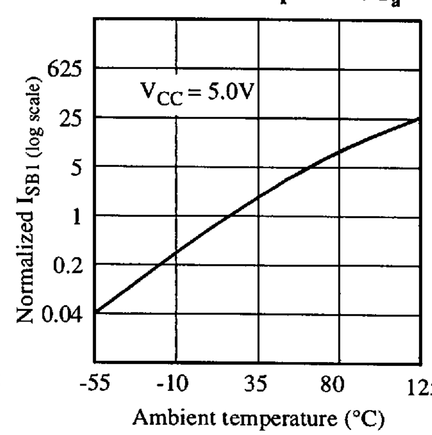
Normalized supply current I_{CC}, I_{SB} vs. supply voltage V_{CC}



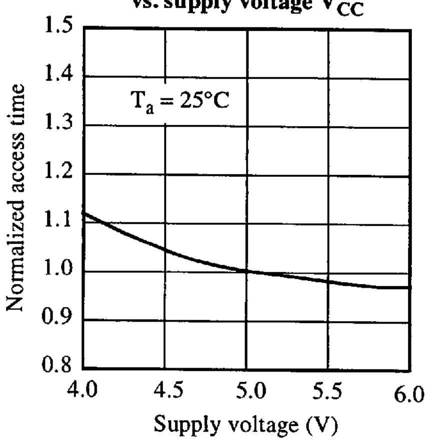
Normalized supply current I_{CC}, I_{SB} vs. ambient temperature T_a



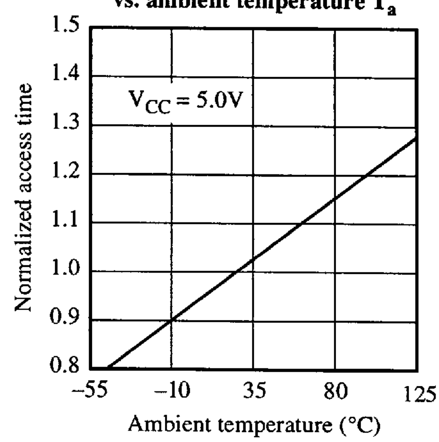
Normalized supply current I_{SB1} vs. ambient temperature T_a



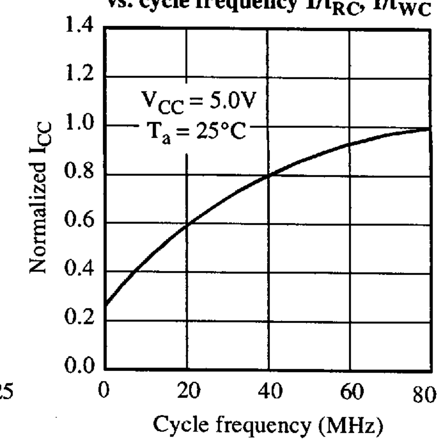
Normalized access time t_{AA} vs. supply voltage V_{CC}



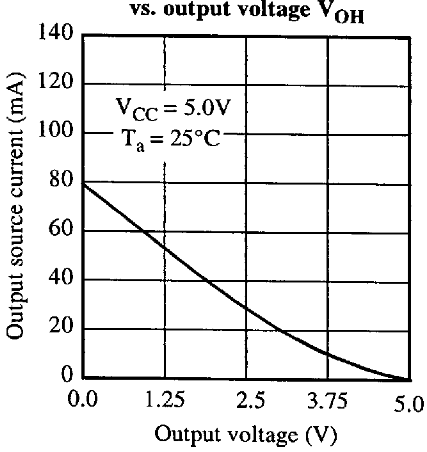
Normalized access time t_{AA} vs. ambient temperature T_a



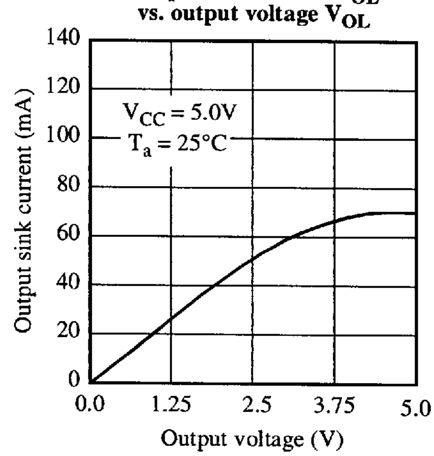
Normalized supply current I_{CC} vs. cycle frequency $1/t_{RC}$, $1/t_{WC}$



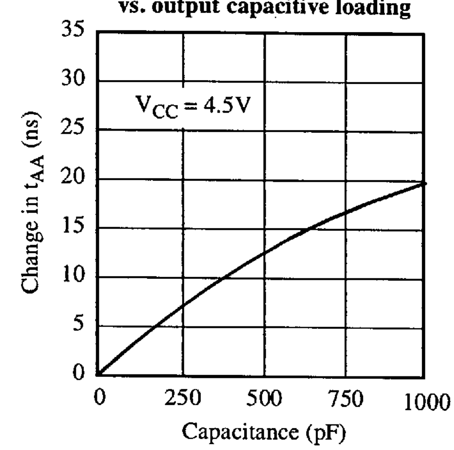
Output source current I_{OH} vs. output voltage V_{OH}



Output sink current I_{OL} vs. output voltage V_{OL}



Typical access time change Δt_{AA} vs. output capacitive loading



Ordering codes

Package \ Access Time	12 ns	15 ns	20 ns	25 ns	35 ns
Plastic DIP, 300 mil	AS7C1028-12TPC AS7C1028L-12TPC	AS7C1028-15TPC AS7C1028L-15TPC	AS7C1028-20TPC AS7C1028L-20TPC	AS7C1028-25TPC AS7C1028L-25TPC	AS7C1028-35TPC AS7C1028L-35TPC
Plastic DIP, 400 mil	AS7C1028-12PC AS7C1028L-12PC	AS7C1028-15PC AS7C1028L-15PC	AS7C1028-20PC AS7C1028L-20PC	AS7C1028-25PC AS7C1028L-25PC	AS7C1028-35PC AS7C1028L-35PC
Plastic SOJ, 300 mil	AS7C1028-12TJC AS7C1028L-12TJC	AS7C1028-15TJC AS7C1028L-15TJC	AS7C1028-20TJC AS7C1028L-20TJC	AS7C1028-25TJC AS7C1028L-25TJC	AS7C1028-35TJC AS7C1028L-35TJC
Plastic SOJ, 400 mil	AS7C1028-12JC AS7C1028L-12JC	AS7C1028-15JC AS7C1028L-15JC	AS7C1028-20JC AS7C1028L-20JC	AS7C1028-25JC AS7C1028L-25JC	AS7C1028-35JC AS7C1028L-35JC

Shaded areas contain advance information.

Part numbering system

AS7C	1028	X	–XX	X	C
[illegible]	Device number	Blank = Standard power L = Low power	Access time	Package: TP = PDIP 300 mil P = PDIP 400 mil TJ = SOJ 300 mil J = SOJ 400 mil	Commercial temperature range, 0°C to 70 °C

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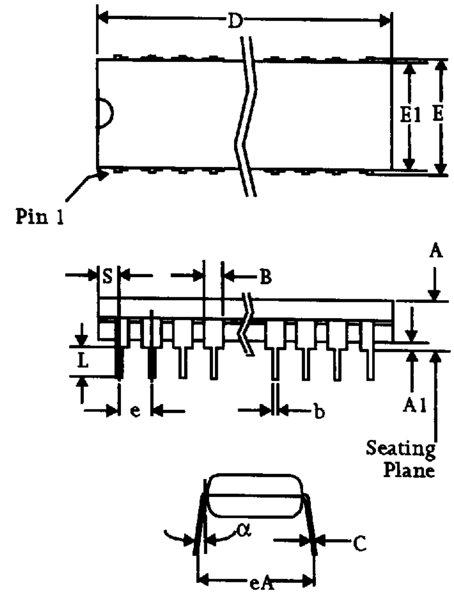
Package diagrams

Plastic dual in-line package (PDIP)

	20-pin 300 mil		28-pin 300 mil		32-pin 300 mil		32-pin 400 mil	
	Min	Max	Min	Max	Min	Max	Min	Max
A	-	0.175	-	0.175	-	0.180	-	0.200
A1	0.010	-	0.010	-	0.015	-	0.015	-
B	0.046	0.054	0.058	0.064	0.045	0.055	0.045	0.065
b	0.018	0.024	0.016	0.022	0.015	0.021	0.014	0.022
C	0.008	0.014	0.008	0.014	0.008	0.012	0.009	0.015
D	-	0.980	-	1.400	-	1.571	-	1.620
E	0.290	0.310	0.295	0.320	0.300	0.325	0.390	0.425
E1	0.263	0.293	0.278	0.298	0.280	0.295	0.340	0.390
e	0.100 BSC		0.100 BSC		0.100 BSC		0.100 BSC	
eA	0.310	0.350	0.330	0.370	0.330	0.370	0.430	0.470
L	0.110	0.130	0.120	0.140	0.110	0.142	0.118	0.162
α	0°	15°	0°	15°	0°	15°	0°	15°
S	-	0.040	-	0.055	-	0.043	-	0.065

Dimensions in inches



Plastic small outline J-bend (SOJ)

	20/26-pin 300 mil		28-pin 300 mil		32-pin 300 mil		28-pin 400 mil		32-pin 400 mil		36-pin 400 mil		40-pin 400 mil		42-pin 400 mil		44-pin 400 mil	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	-	0.140	-	0.140	-	0.145	0.132	0.146	-	0.145	-	-	-	0.145	0.128	0.148	0.128	0.148
A1	0.020	-	0.025	-	0.025	-	0.062	-	0.025	-	-	-	0.025	-	0.025	-	0.025	-
A2	0.095	0.105	0.095	0.105	0.086	0.105	0.105	115	0.086	0.115	0.102 NOM		0.086	0.115	1.105	1.115	1.105	1.115
B	0.025	0.032	0.028 TYP		0.026	0.032	0.024	0.032	0.026	0.032	-	0.032	0.026	0.032	0.026	0.032	0.026	0.032
b	0.016	0.022	0.018 TYP		0.014	0.020	0.013	0.021	0.015	0.020	0.013	0.021	0.015	0.022	0.015	0.020	0.015	0.020
c	0.008	0.014	0.010 TYP		0.006	0.013	0.005	0.012	0.007	0.013	-	-	0.007	0.014	0.007	0.013	0.007	0.013
D	-	0.686	-	0.730	0.820	0.830	0.720	0.729	0.820	0.830	0.920	0.930	1.015	1.035	1.070	1.080	1.120	1.130
E	0.327	0.347	0.327	0.347	0.330	0.340	0.430	0.440	0.435	0.445	0.350	0.390	0.435	0.445	0.370 NOM		0.370 NOM	
E1	0.295	0.305	0.295	0.305	0.292	0.305	0.395	0.405	0.395	0.405	0.400 NOM		0.395	0.405	0.395	0.405	0.395	0.405
E2	0.245	0.285	0.245	0.285	0.250	0.275	0.354	0.378	0.360	0.380	0.435	0.445	0.348	0.390	0.435	0.445	0.435	0.445
e	0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.045	0.055	0.050 BSC		0.050 NOM		0.050 NOM	

Dimensions in inches