DPS256Q8

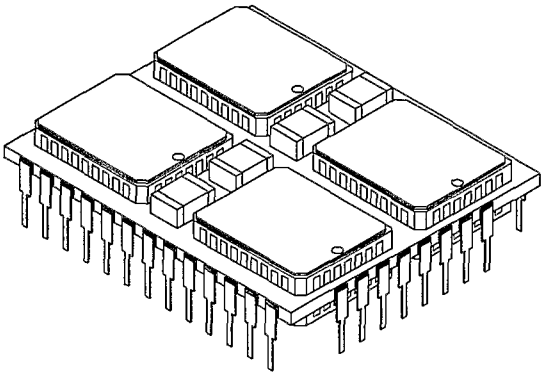
256K X 8 CMOS SRAM MODULE

DESCRIPTION:

The DPS256Q8 is a 2 Megabit (256K X 8) CMOS Static RAM module constructed on a co-fired ceramic substrate using eight low power 32K X 8 CMOS Static RAMs in leadless chip carrier packages.

The DPS256Q8 is offered in a 42-pin Cer-Quad Package which allows two megabits of memory to be placed in less than 1.6 square inches of board space.

The DPS256Q8 is available in fast access time over the commercial, industrial and military temperature ranges, with minimal power consumption.

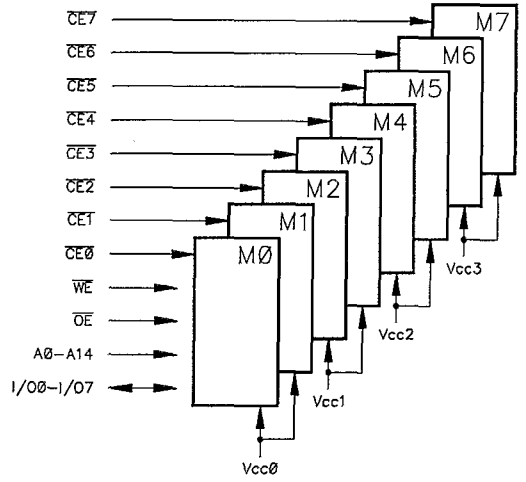


FEATURES:

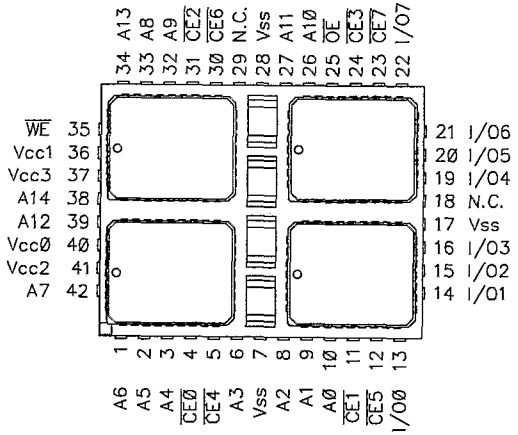
- High-Density 2 Megabit (256K X 8) CMOS Static RAM Module
- Access Times: 25, 35, 45, 55, 70, 85, 100, 120, 150ns (max.)
- Inputs/Outputs Directly TTL Compatible
- Single +5V (±10% Tolerance) Power Supply
- Low Power CMOS Design
- Low Data Retention Voltage: 2.0V min.
- Modules available with semiconductor components compliant to MIL-STD-883, Class B, Rev. C.
- 42-Pin, Cer-Quad Package for Maximum Space Savings
- Module Weight is 16 Grams

PIN NAMES	
A0-A14	Address Inputs
I/O0-I/O7	Data In/Out
$\overline{CE0}$ - $\overline{CE7}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc0 - Vcc3	Power (+5V) Bank
Vss	Ground
N.C.	No Connect

FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAM



CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{CE}	Chip Enable	35	pF	V_{IN} = 0V
C_{ADR}	Address Input	80		
C_{WE}	Write Enable	80		
C_{OE}	Output Enable	80		
$C_{I/O}$	Data Input/Output	80		

RECOMMENDED OPERATING RANGE[1]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{CC}+0.3	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.8	V

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input Timing Reference Levels	1.5V

* Transition between 0.8V and 2.2V.

AC TEST CONDITIONS		
Load	C_L	Parameters Measured
1	100pF	except t_{CLZ}, t_{CHZ}, t_{WHZ}, t_{WLZ}, t_{OLZ} and t_{OHZ}
2	5 pF	t_{CLZ}, t_{CHZ}, t_{WHZ}, t_{WLZ}, t_{OLZ} and t_{OHZ}

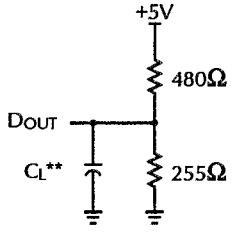
ABSOLUTE MAXIMUM RATINGS[3]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to + 150	°C
T_{BIAS}	Temperature Under Bias	-55 to + 125	°C
V_{CC}	Supply Voltage[1]	-0.5 to + 7.0	V
$V_{I/O}$	Input/Output Voltage[1]	-0.5 to V_{CC} + 0.5	V

TRUTH TABLE					
Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
D_{OUT} Disable	L	H	H	HIGH-Z	Active
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	D_{IN}	Active

L = LOW H = HIGH X = Don't Care

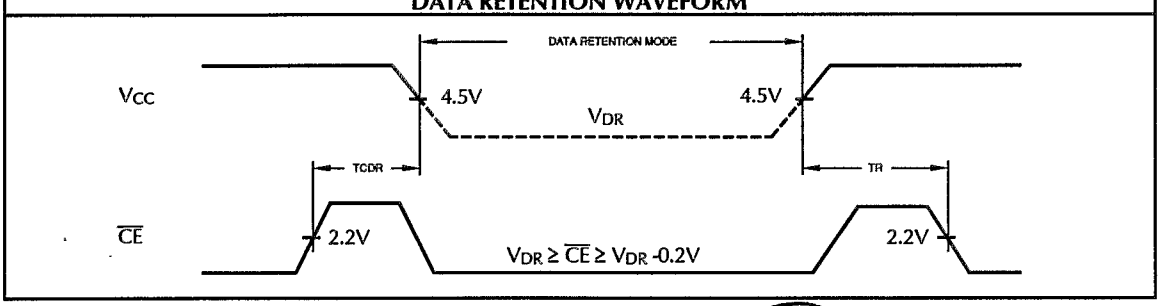
Figure 1. Output Load

** Including Probe and Jig Capacitance.



DATA RETENTION CHARACTERISTICS						
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DR}	Data Retention Voltage	$\overline{CE} \geq V_{CC}$ -0.2V	2.0	5.0	5.5	V
t_{CDR}	Chip Disable to Data Retention Time		0			ns
t_R	Recovery Time	t_{RC} = Read Cycle Timing	t_{RC}			ns

DATA RETENTION WAVEFORM



DPS256Q8-25, 35, 45, 55, 70, 85, 100 DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-20	20	-20	20	-20	20	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-20	20	-20	20	-20	20	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		310		360		365	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA		350		405		405	mA
I_{SB1}	Full Standby Supply Current (CMOS)	$\overline{CE}$ ≥ V_{CC} -0.2V		16		16		16	mA
I_{SB2}	Standby Supply (TTL)	$\overline{CE}$ = V_{IH}		240		280		280	mA
I_{CCDR2}	Data Retention Supply Current	V_{DR} = 2V $\overline{CE}$ ≥ V_{DR} - 0.2V		2.8		3.2		6.4	mA
I_{CCDR3}	Data Retention Supply Current	V_{DR} = 3V $\overline{CE}$ ≥ V_{DR} -0.2V		2.4		2.8		4.8	mA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA	2.4		2.4		2.4		V

DPS256Q8-120, 150 DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-20	20	-20	20	-20	20	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-20	20	-20	20	-20	20	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		60		60		60	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA		75		80		85	mA
I_{SB1}	Full Standby Supply Current (CMOS)	$\overline{CE}$ ≥ V_{CC} -0.2V		0.8		1.6		2.4	mA
I_{SB2}	Standby Supply (TTL)	$\overline{CE}$ = V_{IH}		16		16		16	mA
I_{CCDR2}	Data Retention Supply Current	V_{DR} = 2V $\overline{CE}$ ≥ V_{DR} - 0.2V		0.25		0.35		1.60	mA
I_{CCDR3}	Data Retention Supply Current	V_{DR} = 3V $\overline{CE}$ ≥ V_{DR} -0.2V		0.35		0.40		1.95	mA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA	2.4		2.4		2.4		V

DPS256Q8-25, 35, 45, 55, 70, 85 AC Operating Conditions And Characteristics - READ CYCLE: Over operating ranges

No.	Symbol	Parameter	-25		-35		-45		-55		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	25		35		45		55		70		85		ns
2	t_{AA}	Address Access Time		25		35		45		55		70		85	ns
3	t_{CO}	Chip Enable to Output Valid		25		35		45		55		70		85	ns
4	t_{OV}	Output Enable to Output Valid		15		20		25		35		40		60	ns
5	t_{OH}	Output Hold from Address Change	3		3		3		3		3		3		ns
6	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 5]	5		5		5		5		5		5		ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [4, 5]	5		5		5		5		5		5		ns
8	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 5]		15		15		20		25		30		30	ns
9	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 5]		15		15		20		25		30		30	ns

DPS256Q8-25, 35, 45, 55, 70, 85 AC Operating Conditions And Characteristics - WRITE CYCLE [6,7]: Over operating ranges

No.	Symbol	Parameter	-25		-35		-45		-55		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time	25		35		45		55		70		85		ns
11	t_{AW}	Address Valid to End of Write	20		30		40		50		65		75		ns
12	t_{CW}	Chip Enable to End of Write	20		30		40		50		65		75		ns
13	t_{DW}	Data Valid to End of Write	15		20		25		25		30		35		ns
14	t_{DH}	Data Hold Time	3		3		3		3		3		0		ns
15	t_{WP}	Write Pulse Width	20		30		35		40		45		65		ns
16	t_{AS}	Address Set-up Time*	0		0		0		0		0		0		ns
17	t_{AH}	Address Hold Time	0		0		0		0		0		0		ns
18	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 5]		15		15		15		20		25		30	ns
19	t_{WLZ}	Write Enable to Output in LOW-Z [4, 5]	5		5		5		5		5		5		ns

DPS256Q8-100, 120, 150 AC Operating Conditions And Characteristics - READ CYCLE: Over operating ranges

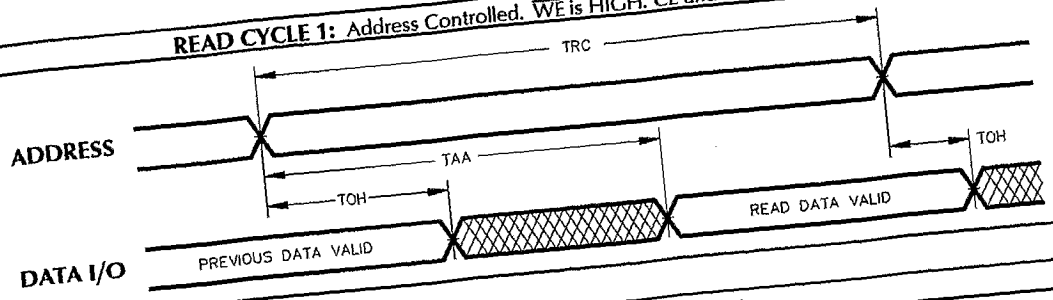
No.	Symbol	Parameter	-100		-120		-150		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	100		120		150		ns
2	t_{AA}	Address Access Time		100		120		150	ns
3	t_{CO}	Chip Enable to Output Valid		100		120		150	ns
4	t_{OV}	Output Enable to Output Valid		60		60		70	ns
5	t_{OH}	Output Hold from Address Change	10		10		10		ns
6	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 5]	10		10		10		ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [4, 5]	5		5		5		ns
8	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 5]		35		40		50	ns
9	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 5]		35		40		50	ns

DPS256Q8-100, 120, 150 AC Operating Conditions And Characteristics - WRITE CYCLE [6,7]: Over operating ranges

No.	Symbol	Parameter	-100		-120		-150		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time	100		120		150		ns
11	t_{AW}	Address Valid to End of Write	90		100		120		ns
12	t_{CW}	Chip Enable to End of Write	90		100		120		ns
13	t_{DW}	Data Valid to End of Write	40		50		60		ns
14	t_{DH}	Data Hold Time	0		0		0		ns
15	t_{WP}	Write Pulse Width	75		90		110		ns
16	t_{AS}	Address Set-up Time*	0		0		0		ns
17	t_{AH}	Address Hold Time	0		0		0		ns
18	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 5]		35		40		50	ns
19	t_{WLZ}	Write Enable to Output in LOW-Z [4, 5]	5		5		5		ns

* Valid for both Read and Write Cycles.

READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ and $\overline{OE}$ are LOW.



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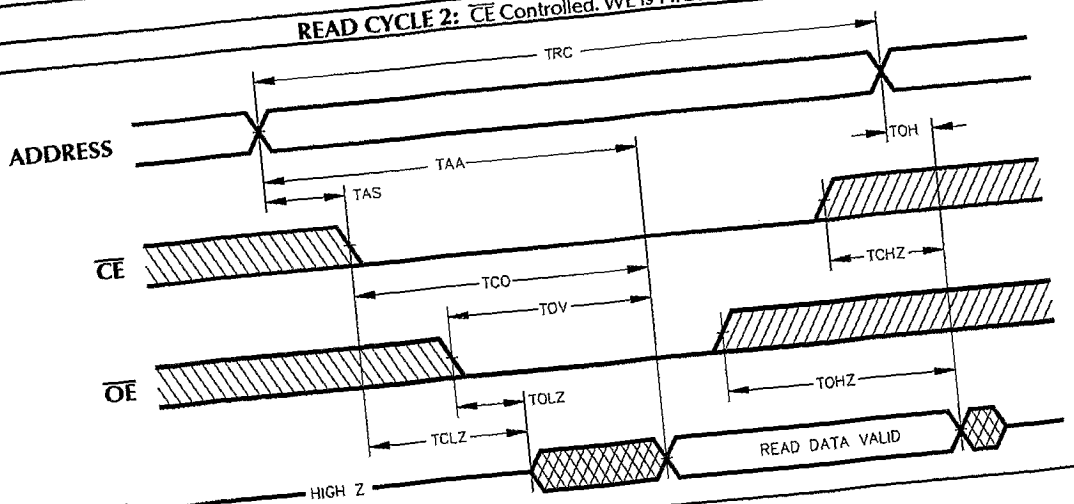
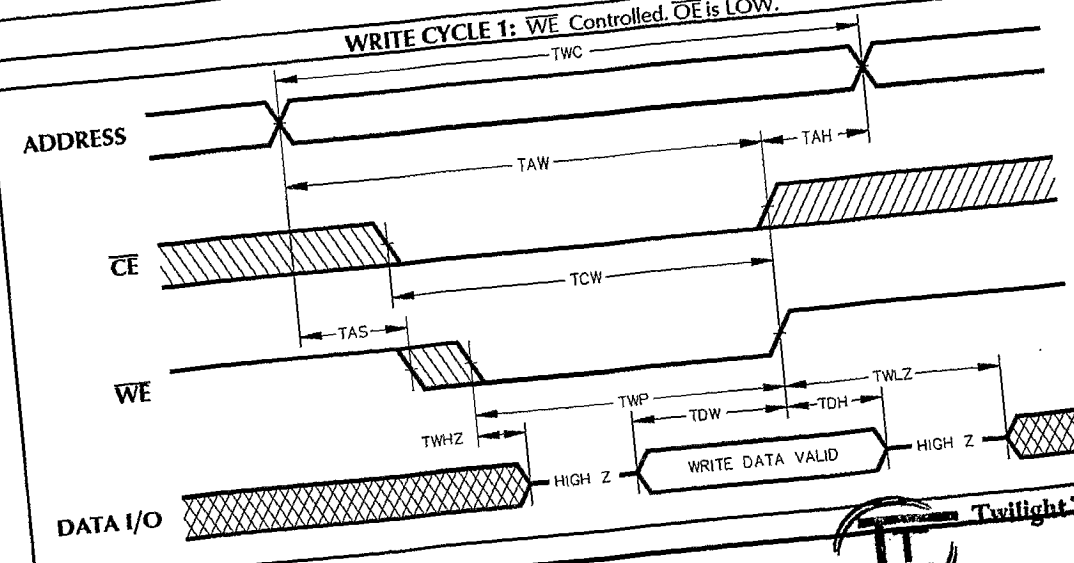
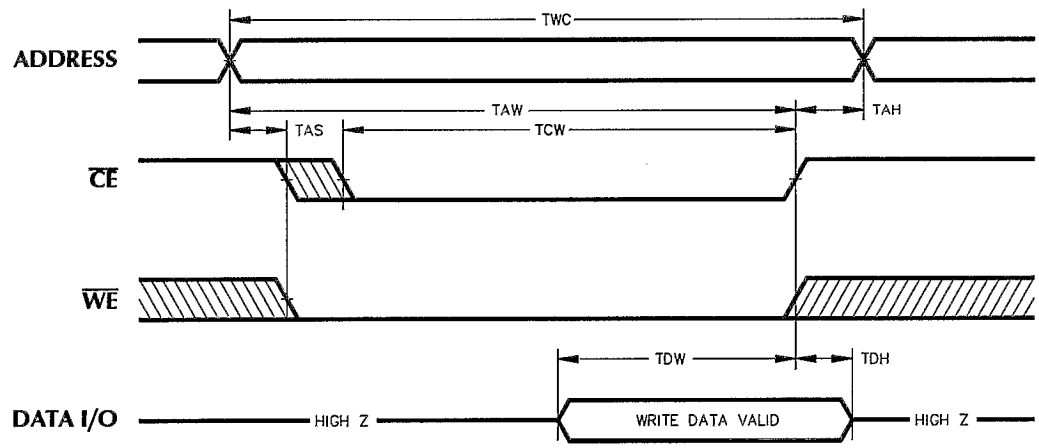
READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.



WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW.



WRITE CYCLE 2: $\overline{CE}$ Controlled. $\overline{OE}$ is HIGH.



NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min.= -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ± 500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

WAVEFORM KEY

Data Valid	Transition from HIGH to LOW	Transition from LOW to HIGH	Data Undefined or Don't Care

ORDERING INFORMATION

DP S256Q8 – XXX X

PREFIX | DEVICE TYPE | SPEED | GRADE

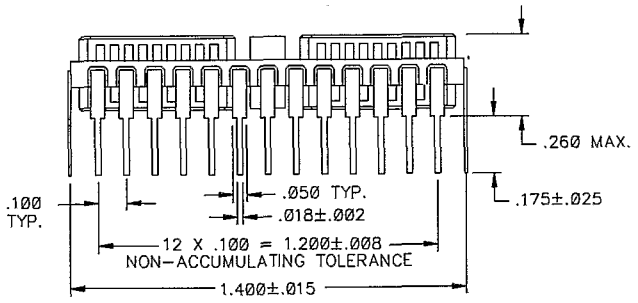
C	COMMERCIAL	0°C to +70°C
I	INDUSTRIAL	−40°C to +85°C
M	MILITARY	−55°C to +125°C
B*	MIL−PROCESSED	−55°C to +125°C

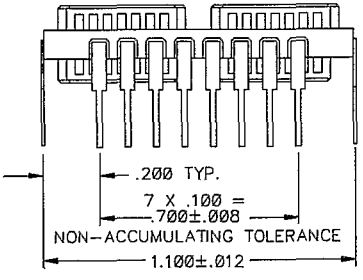
25	25ns
35	35ns
45	45ns
55	55ns
70	70ns
85	85ns
100	100ns
120	120ns
150	150ns

CMOS SRAM 256K X 8 CER−QUAD PACKAGE

* B grade modules can be constructed with 883 devices.

MECHANICAL DIAGRAMS





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