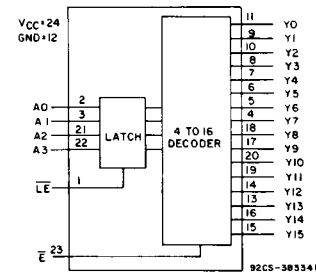
CD54HC4514/3A
CD54HCT4514/3A

4-to-16-Line Decoder/Demultiplexer w/Input Latches

The RCA CD54HC4514 and CD54HCT4514 are high-speed silicon-gate devices consisting of a 4-bit strobed latch and a 4-to-16-line decoder. The selected output is enabled by a low on the enable input ($\overline{E}$). A high on $\overline{E}$ inhibits selection of any output. Demultiplexing is accomplished by using the E input as the data input and the select inputs (A0-A3) as addresses. This $\overline{E}$ input also serves as a chip select when these devices are cascaded.

When Latch Enable ($\overline{LE}$) is high the output follows changes in the inputs. When $\overline{LE}$ is low the output is isolated from changes in the input and remains at the level (high) it had before the latches were enabled. These devices, enhanced versions of the equivalent CMOS types, can drive 10 LSTTL loads.



FUNCTIONAL DIAGRAM

Package Specifications

See Section 11, Fig. 15

Static Electrical Characteristics (Limits with black dots (•) are tested 100%)

CHARACTERISTICS		TEST CONDITIONS HC/HCT V_{DD}	V_O	I_O	V_{CC} or GND	V_{IN} HC V_{IL} or V_{IH}	V_{IN} HCT V_{IL} or V_{IH}	LIMITS MIN.	LIMITS MAX.	UNITS
Quiescent Device Current I_{CC}	25°C	6	—	—	6, 0	—	—	—	8•	μA
	-55°C / +125°C	6	—	—	6, 0	—	—	—	160•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

HCT INPUT LOADING TABLE

INPUT	UNIT LOAD*
A0 - A3	0.15
$\overline{LE}$	0.85
$\overline{E}$	0.3

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54HC4514/3A
CD54HCT4514/3A

Switching Speed (Limits with black dots (•) are tested 100%.)

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-55°C to +125°C				UNITS
			HC		HCT		54HC		54HCT		
		V	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Select to Outputs	t_{PLH} t_{PHL}	2	—	275	—	—	—	115	—	—	ns
		4.5	—	55•	—	55•	—	83•	—	83•	
		6	—	47	—	—	—	71	—	—	
$\overline{LE}$ to Outputs		2	—	225	—	—	—	340	—	—	
		4.5	—	45•	—	50•	—	68•	—	75•	
		6	—	38	—	—	—	58	—	—	
$\overline{E}$ to Outputs		2	—	175	—	—	—	265	—	—	
		4.5	—	35•	—	40•	—	53•	—	60•	
		6	—	30	—	—	—	45	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	110	—	—	
		4.5	—	15	—	15	—	22	—	22	
		6	—	13	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	pF

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT4514	4-11,13-20	1-3,12,21-23	24	4-11,13-20	12	1-3,21-24
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR 50 kHz**	**OSCILLATOR 25 kHz**
CD54HC/HCT4514	—	2,3,12	4-11,13-20	21,22,24	1	23

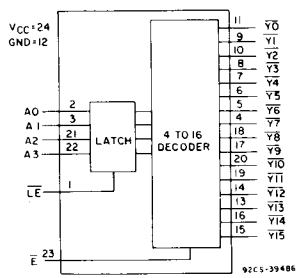
NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

4-to-16-Line Decoder with Input Latches

CD54HC4515/3A
CD54HCT4515/3A

The RCA CD54HC4515 and CD54HCT4515 are high-speed silicon-gate devices consisting of a 4-bit strobed latch and a 4-to-16-line decoder. The selected output is enabled by a low on the enable input ($\overline{E}$). A high on $\overline{E}$ inhibits selection of any output. Demultiplexing is accomplished by using the $\overline{E}$ input as the data input and the select inputs (A0-A3) as addresses. This $\overline{E}$ input also serves as a chip select when these devices are cascaded.

When Latch Enable ($\overline{LE}$) is high the output follows changes in the inputs. When $\overline{LE}$ is low the output is isolated from changes in the input and remains at the level (low) it had before the latches were enabled. These devices, enhanced versions of the equivalent CMOS types, can drive 10 LSTTL loads.



FUNCTIONAL DIAGRAM

Package Specifications

See Section 11, Fig. 15