Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

74F258A

FEATURES

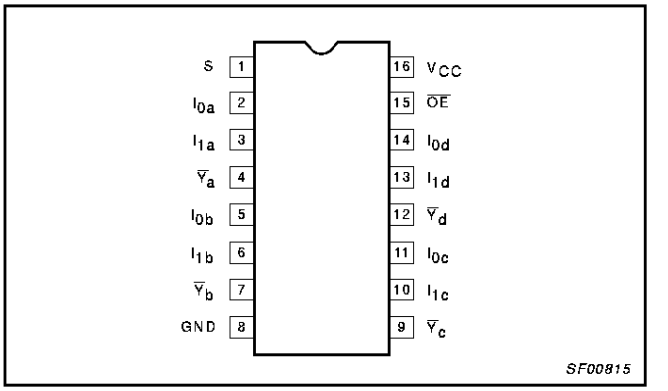
- Multifunction capability
- Non-inverting data path
- 3-State outputs
- See 74F257A for non-inverting version

DESCRIPTION

The 74F258A has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Select (S) input. The I_{0n} inputs are selected when the Select input is Low and the I_{1n} inputs are selected when the Select input is High. Data appears at the outputs in inverted form.

The 74F258A is the logical implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic level supplied to the Select input. Outputs are forced to a High impedance "off" state when the Output Enable input ($\overline{OE}$) is High. All but one device must be in the High impedance state to avoid currents that would exceed the maximum ratings if outputs are tied together. Design of the output signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F258A	3.5ns	14mA

ORDERING INFORMATION

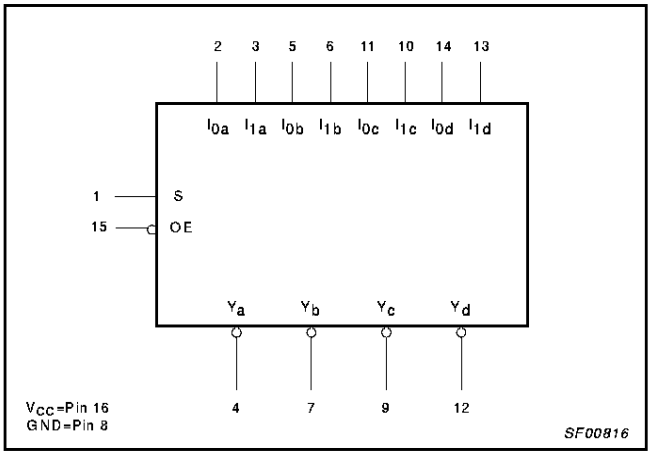
DESCRIPTION	ORDER CODE	PKG. DWG. #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic DIP	N74F258AN	SOT38-4
16-pin plastic SO	N74F258AD	SOT162-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

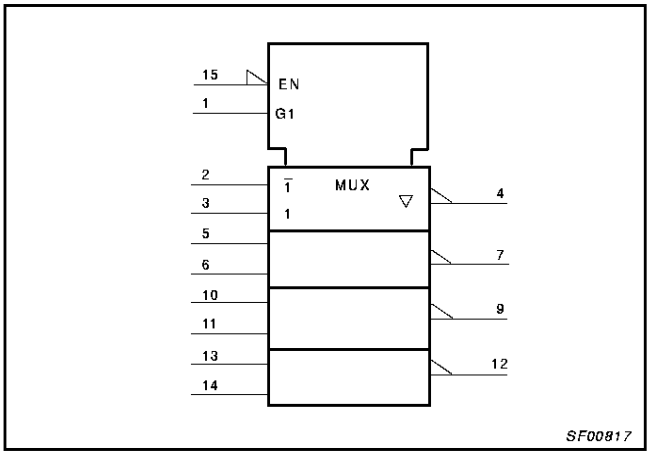
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0n}, I_{1n}	Data inputs	1.0/1.0	20µA/0.6mA
S	Common select input	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Y}_a$ - $\overline{Y}_d$	Data outputs	150/40	3.0mA/24mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



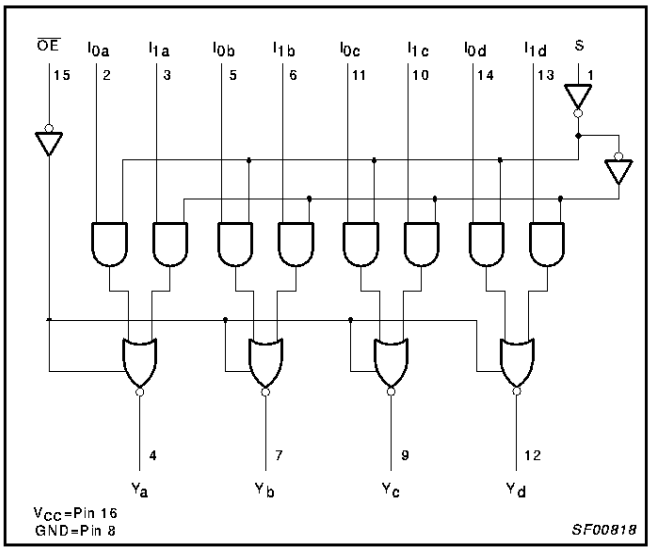
LOGIC SYMBOL (IEEE/IEC)



Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

74F258A

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–3	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.4			V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX	I_{1n}=4.5V, $\overline{OE}$=I_{0n}=S=GND		8.5	11.5	mA
	Supply current (total) I_{CCL}	V_{CC} = MAX	I_{1n}=S=4.5V, $\overline{OE}$=I_{0n}=GND		17	23	mA
	Supply current (total) I_{CCZ}	V_{CC} = MAX	I_{1n}=$\overline{OE}$=4.5V,I_{0n}=S=GND		16	22	mA

NOTES:

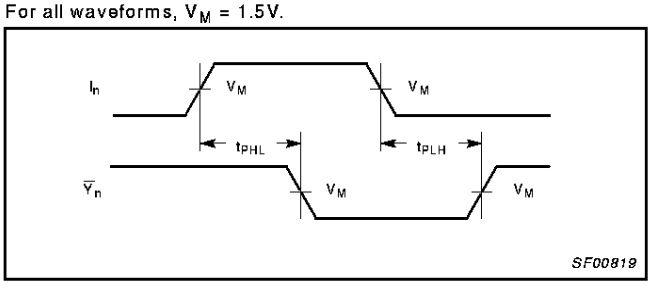
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

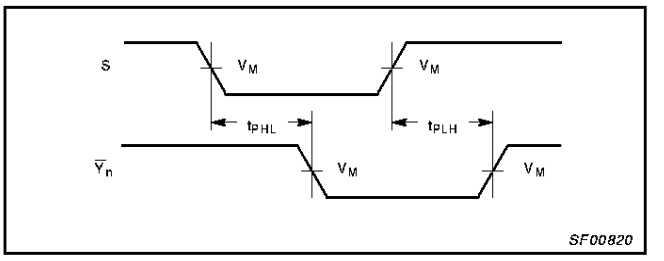
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_{amb}= +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω MIN	TYP	MAX	LIMITS T_{amb} = –55°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω MIN	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	Waveform 1	3.0 1.0	4.5 2.5	6.0 4.0	2.5 1.0	7.0 4.5	ns ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}_n$	Waveform 2	3.5 2.5	6.5 6.0	8.0 8.0	3.5 2.5	9.0 9.0	ns ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 3 Waveform 4	4.0 4.0	6.0 5.5	7.5 7.5	3.5 3.5	8.5 8.5	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 3 Waveform 4	2.0 2.0	3.5 3.5	5.5 5.5	2.0 2.0	6.5 6.0	ns ns

AC WAVEFORMS

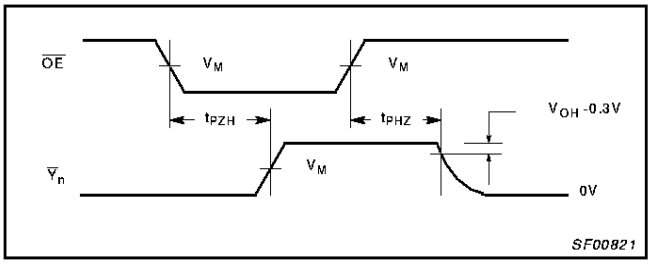
For all waveforms, V_M = 1.5V.



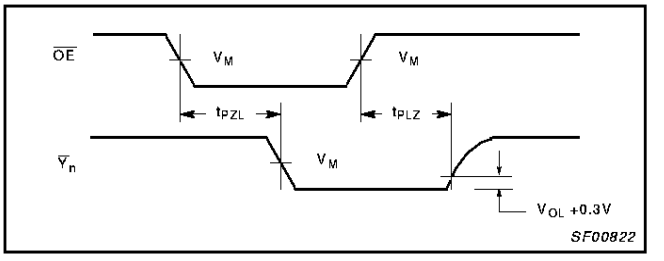
Waveform 1. Propagation Delay Data and Select to Output



Waveform 2. Propagation Delay Select to Output

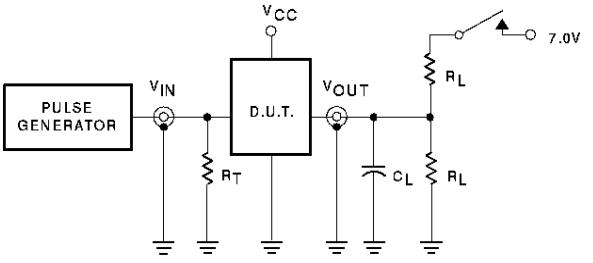


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

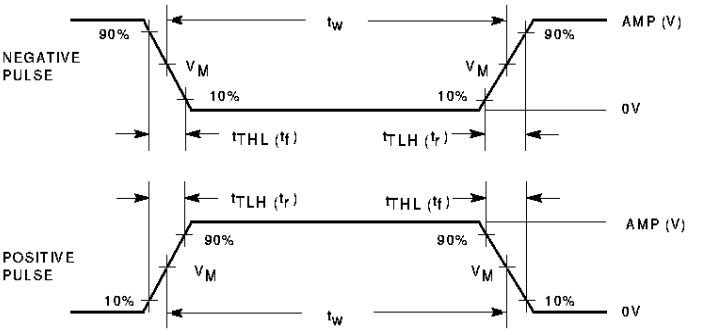


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777