TMS416169, TMS416169P, TMS418169, TMS418169P
TMS426169, TMS426169P, TMS428169, TMS428169P
1048576-WORD BY 16-BIT EXTENDED DATA OUT HIGH-SPEED DRAMS

SMKS886A – APRIL 1995 – REVISED JUNE 1995

- **Organization . . . 1 048 576 × 16**
- **Single Power Supply (5 V or 3.3 V)**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR EDO CYCLE MIN
'4xx169/P-60	60 ns	15 ns	30 ns	25 ns
'4xx169/P-70	70 ns	18 ns	35 ns	30 ns
'4xx169/P-80	80 ns	20 ns	40 ns	35 ns

- **Extended Data Out (EDO) Operation**
- **$\overline{xCAS}$-Before-$\overline{RAS}$ (xCBR) Refresh**
- **Long Refresh Period and Self-Refresh Option (TMS4xx169P)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **High-Reliability Plastic 42-Lead (DZ Suffix) 400-Mil-Wide Surface-Mount (SOJ) Package and 44/50-Lead (DGE Suffix) Surface-Mount Thin Small-Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Texas Instrument Enhanced Performance Implanted CMOS (EPIC™) Process**

AVAILABLE OPTIONS

DEVICE	POWER SUPPLY	SELF REFRESH, BATTERY BACKUP	REFRESH CYCLES
TMS416169	5 V	—	4096 in 64 ms
TMS416169P	5 V	Yes	4096 in 128 ms
TMS418169	5 V	—	1024 in 16 ms
TMS418169P	5 V	Yes	1024 in 128 ms
TMS426169	3.3 V	—	4096 in 64 ms
TMS426169P	3.3 V	Yes	4096 in 128 ms
TMS428169	3.3 V	—	1024 in 16 ms
TMS428169P	3.3 V	Yes	1024 in 128 ms

DZ PACKAGE (TOP VIEW)

V_{CC}	1	42	V_{SS}
DQ0	2	41	DQ15
DQ1	3	40	DQ14
DQ2	4	39	DQ13
DQ3	5	38	DQ12
V_{CC}	6	37	V_{SS}
DQ4	7	36	DQ11
DQ5	8	35	DQ10
DQ6	9	34	DQ9
DQ7	10	33	DQ8
NC	11	32	NC
NC	12	31	$\overline{LCAS}$
$\overline{W}$	13	30	$\overline{UCAS}$
$\overline{RAS}$	14	29	$\overline{OE}$
A11†	15	28	A9
A10†	16	27	A8
A0	17	26	A7
A1	18	25	A6
A2	19	24	A5
A3	20	23	A4
V_{CC}	21	22	V_{SS}

DGE PACKAGE (TOP VIEW)

V_{CC}	1	50	V_{SS}
DQ0	2	49	DQ15
DQ1	3	48	DQ14
DQ2	4	47	DQ13
DQ3	5	46	DQ12
V_{CC}	6	45	V_{SS}
DQ4	7	44	DQ11
DQ5	8	43	DQ10
DQ6	9	42	DQ9
DQ7	10	41	DQ8
NC	11	40	NC
NC	15	36	NC
NC	16	35	$\overline{LCAS}$
$\overline{W}$	17	34	$\overline{UCAS}$
$\overline{RAS}$	18	33	$\overline{OE}$
A11†	19	32	A9
A10†	20	31	A8
A0	21	30	A7
A1	22	29	A6
A2	23	28	A5
A3	24	27	A4
V_{CC}	25	26	V_{SS}

† A10 and A11 are NC for TMS4x8169 and TMS4x8169P.

PIN NOMENCLATURE

A0–A11	Address Inputs
DQ0–DQ15	Data In/Data Out
$\overline{LCAS}$	Lower Column-Address Strobe
$\overline{UCAS}$	Upper Column-Address Strobe
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V or 3.3-V Supply‡
V_{SS}	Ground
$\overline{W}$	Write Enable

‡ See Available Options Table.

PRODUCT PREVIEW

description

The TMS4xx169 series is a set of high-speed, 16777216-bit dynamic random-access memories (DRAMs) organized as 1048576 words of 16 bits each. The TMS4xx169P series is a similar set of high-speed, low-power, self-refresh, 16777216-bit DRAMs organized as 1048576 words of 16 bits each. Both sets employ state-of-the-art EPIC™ technology for high performance, reliability, and low power at low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS4xx169 and TMS4xx169P are offered in a 44/50-lead plastic surface-mount TSOP (DGE suffix) and a 42-lead plastic surface-mount SOJ (DZ suffix) package. These packages are characterized for operation from 0°C to 70°C.

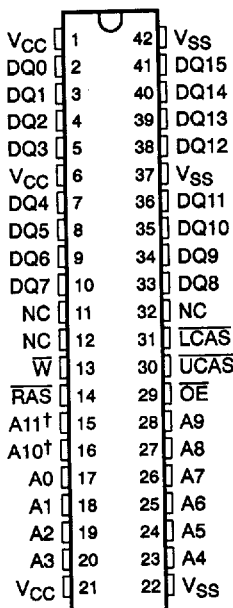EPIC is a trademark of Texas Instruments Incorporated.

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logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
  The pin numbers shown correspond to the DZ package.
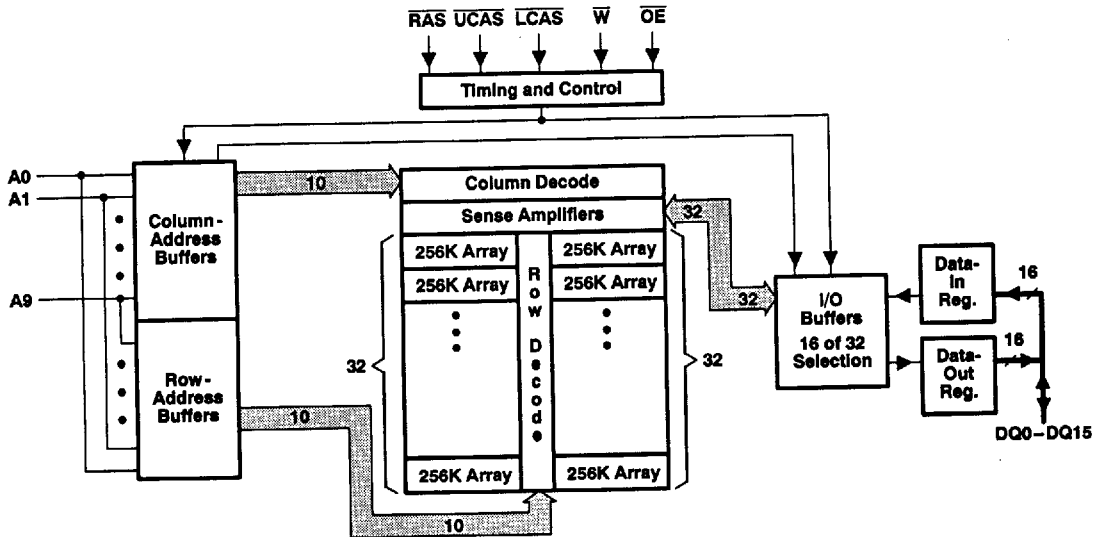‡ A10 and A11 are NC for TMS4x8169 and TMS4x8169P.

PRODUCT PREVIEW

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functional block diagram (TMS4x6169/P)
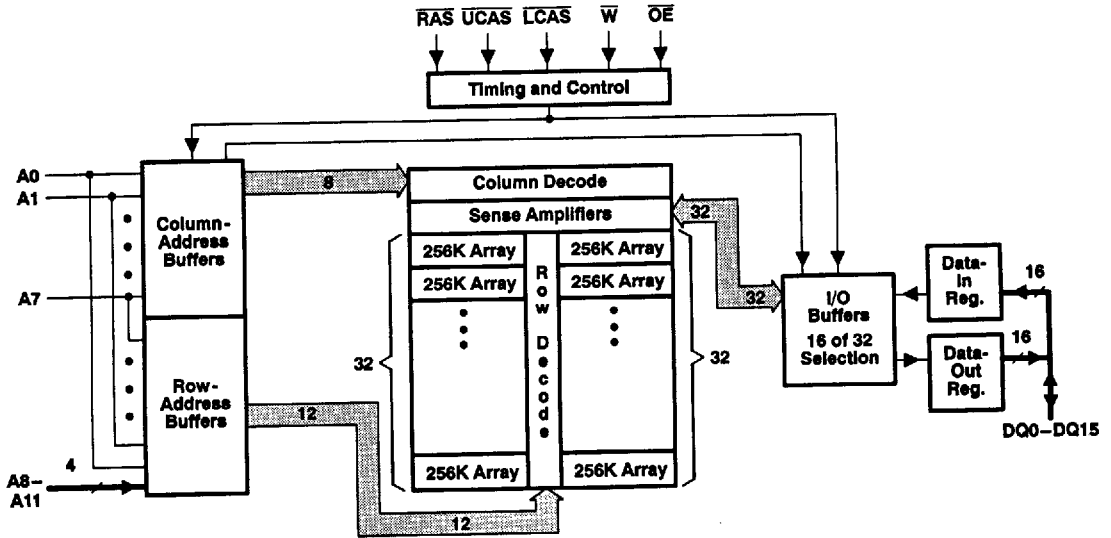
(a) TMS4x6169, TMS4x6169P

functional block diagram (TMS4x8169/P)

(b) TMS4x8169, TMS4x8169P

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operation

dual $\overline{CAS}$

Two $\overline{CAS}$ pins ($\overline{LCAS}$ and $\overline{UCAS}$) are provided to give independent control of the 16 data-I/O pins (DQ0–DQ15), with $\overline{LCAS}$ corresponding to DQ0–DQ7 and $\overline{UCAS}$ corresponding to DQ8–DQ15. For read or write cycles, the column address is latched on the first $\overline{xCAS}$ falling edge. Each $\overline{xCAS}$ going low enables its corresponding DQx pin with data associated with the column address latched on the first falling $\overline{xCAS}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{xCAS}$ edge. The delay time from $\overline{xCAS}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{xCAS}$ to its corresponding DQx pin.

In order to latch in a new column address, both $\overline{xCAS}$ pins must be brought high. The column-precharge time (see parameter t_{CP}) is measured from the last $\overline{xCAS}$ rising edge to the first $\overline{xCAS}$ falling edge of the new cycle. Keeping a column address valid while toggling $\overline{xCAS}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{xCAS}$ must be brought low before the other $\overline{xCAS}$ is taken high.

For early-write cycles, the data is latched on the first $\overline{xCAS}$ falling edge. Only the DQs that have the corresponding $\overline{xCAS}$ low are written into. Each $\overline{xCAS}$ must meet t_{CAS} minimum in order to ensure writing into the storage cell. To latch a new address and new data, all $\overline{xCAS}$ pins must be high and meet t_{CP}.

extended data out

Extended data out (EDO) allows for data output rates of up to 40 MHz for 60-ns devices. When keeping the same row address while selecting random column addresses, the time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by t_{RASP}, the maximum $\overline{RAS}$ low time.

EDO does not enter the DQs into the high-impedance state with the rising edge of $\overline{xCAS}$. The output remains valid for the system to latch the data. After $\overline{xCAS}$ goes high, the DRAM is decoding the next address. $\overline{OE}$ and $\overline{W}$ can be used to control the output impedance. Descriptions of $\overline{OE}$ and $\overline{W}$ further explain EDO operation benefit.

address: A0–A11 (TMS4x6169, TMS4x6169P) and A0–A9 (TMS4x8169, TMS4x8169P)

Twenty address bits are required to decode a single one of the 1048576 storage cell locations. For the TMS4x6169 and TMS4x6169P, 12 row-address bits are set up on A0 through A11 and latched onto the chip by $\overline{RAS}$. Eight column-address bits are set up on A0 through A7 and latched on the chip by the first $\overline{xCAS}$. For the TMS4x8169 and TMS4x8169P, 10 row-address bits are set up on A0–A9 and latched on the chip by $\overline{RAS}$. Ten column-address bits are set up on A0–A9 and latched on the chip by the first $\overline{xCAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{xCAS}$. $\overline{RAS}$ is similar to a chip-enable in that it activates the sense amplifiers as well as the row decoder. $\overline{xCAS}$ is used as a chip-select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{xCAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation independent of the state of $\overline{OE}$. This permits early-write operation to be completed with $\overline{OE}$ grounded. If $\overline{W}$ goes low in an extended-data-out read cycle, the DQs go into the high-impedance state as long as $\overline{xCAS}$ is high.

data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{xCAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{xCAS}$ and the data is strobed in by the first occurring $\overline{xCAS}$ with setup and hold times referenced to this signal. In a

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data in (DQ0–DQ15) (continued)

delayed-write or read-modify-write cycle, $\overline{xCAS}$ is already low and the data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines.

data out (DQ0–DQ15)

Data out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{xCAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{xCAS}$) as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. While $\overline{xCAS}$ and $\overline{RAS}$ are low and $\overline{W}$ is high, $\overline{OE}$ can be brought low or high and the DQs transition between valid data and high impedance. There are two methods for placing the DQs into the high-impedance state and keeping them that way during $\overline{xCAS}$ high time using $\overline{OE}$. The first method is to transition $\overline{OE}$ high before $\overline{xCAS}$ transitions high and keep $\overline{OE}$ high for t_{CHO} past the $\overline{CAS}$ transition. This disables the DQs and they remain in the high-impedance state, regardless of $\overline{OE}$, until $\overline{xCAS}$ falls again. The second method is to have $\overline{OE}$ low as $\overline{xCAS}$ transitions high. Then $\overline{OE}$ can pulse high for a minimum of t_{OEP} anytime during $\overline{CAS}$ high time disabling the DQs regardless of further transitions on $\overline{OE}$ until $\overline{CAS}$ falls again.

$\overline{RAS}$-only refresh

TMS4x6169, TMS4x6169P

A refresh operation must be performed at least once every 64 ms (256 ms for TMS4x6169P) to retain data. This is achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding both $\overline{xCAS}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

TMS4x8169, TMS4x8169P

A refresh operation must be performed at least once every 16 ms (128 ms for TMS4x8169P) to retain data. This is achieved by strobing each of the 1024 rows (A0–A9). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding both $\overline{xCAS}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pins. This is accomplished by holding $\overline{xCAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored and the refresh address is generated internally.

$\overline{xCAS}$-before-$\overline{RAS}$ (xCBR) refresh

xCBR refresh is achieved by bringing at least one $\overline{xCAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive xCBR refresh cycles, $\overline{xCAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

battery-backup refresh

TMS4x6169P

A low-power battery-backup refresh mode that requires less than 600 µA (5 V) or 350 µA (3.3 V) refresh current is available on the TMS4x6169P. Data integrity is maintained using xCBR refresh with a period of 31.25 µs while holding $\overline{RAS}$ low for less than 300 ns. To minimize current consumption, all input levels must be at CMOS levels ($V_{IL} < 0.2$ V, $V_{IH} > V_{CC} - 0.2$ V).

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TMS4x8169P

A low-power battery-backup refresh mode that requires less than 600 µA (5 V) or 350 µA (3.3 V) refresh current is available on the TMS4x8169P. Using xCBR refresh with a period of 125 µs while holding $\overline{RAS}$ low for less than 300 ns maintains data integrity. To minimize current consumption, all input levels must be at CMOS levels (V_{IL} < 0.2 V, V_{IH} > V_{CC} − 0.2 V).

self-refresh (TMS4xx169P)

The self-refresh mode is entered by dropping $\overline{xCAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{xCAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 µs. The chip is then refreshed internally by an on-board oscillator. No external address is required because the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{xCAS}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

power-up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after power-up to the full V_{CC} level. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or xCBR) cycle.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}:	TMS41x169, TMS41x169P	− 1 V to 7 V
	TMS42x169, TMS42x169P	− 0.5 V to 4.6 V
Voltage range on any pin (see Note 1):	TMS41x169, TMS41x169P	− 1 V to 7 V
	TMS42x169, TMS42x169P	− 0.5 V to 4.6 V
Short-circuit output current		50 mA
Power dissipation		1 W
Operating free-air temperature range, T_A		0°C to 70°C
Storage temperature range, T_{stg}		− 55°C to 125°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		'41x169			'42x169			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	3	3.3	3.6	V
V_{SS}	Supply voltage		0			0		V
V_{IH}	High-level input voltage	2.4		6.5	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	− 1		0.8	− 0.3		0.8	V
T_A	Operating free-air temperature	0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

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TMS416169/P

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'416169-60 '416169P-60		'416169-70 '416169P-70		'416169-80 '416169P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	$I_{OH} = -5$ mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	$I_{OL} = 4.2$ mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	$V_{CC} = 5.5$ V, $V_I = 0$ V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	μA
I_O	Output current (leakage)	$V_{CC} = 5.5$ V, $V_O = 0$ V to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	μA
I_{CC1}‡§	Read- or write-cycle current	$V_{CC} = 5.5$ V, Minimum cycle			90		80		70	mA
I_{CC2}	Standby current	$V_{IH} = 2.4$ V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			2		2		2	mA
		$V_{IH} = V_{CC} - 0.2$ V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'416169		1		1		1	mA
			'416169P		500		500		500	μA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	$V_{CC} = 5.5$ V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			90		80		70	mA
I_{CC4}‡¶	Average EDO current	$V_{CC} = 5.5$ V, $t_{HPC} = $ MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			100		90		80	mA
I_{CC6}#	Self-refresh current	$\overline{xCAS} < 0.2$ V, $\overline{RAS} < 0.2$ V, Measured after t_{RASS} min			500		500		500	μA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms); CBR only	$t_{RC} = 31.25$ μs, $t_{RAS} \le 300$ ns, $V_{CC} - 0.2$ V $\le V_{IH} \le 6.5$ V, 0 V $\le V_{IL} \le 0.2$ V, $\overline{W}$ and $\overline{OE} = V_{IH}$, Address and data stable			600		600		600	μA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS} = V_{IL}$
¶ Measured with a maximum of one address change while $\overline{xCAS} = V_{IH}$
# For TMS416169P only

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TMS418169/P

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

	PARAMETER	TEST CONDITIONS†		'418169-60 '418169P-60		'418169-70 '418169P-70		'418169-80 '418169P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	$I_{OH} = -5$ mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	$I_{OL} = 4.2$ mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	$V_{CC} = 5.5$ V, $V_I = 0$ V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	μA
I_O	Output current (leakage)	$V_{CC} = 5.5$ V, $V_O = 0$ V to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	μA
I_{CC1}‡§	Read- or write-cycle current	$V_{CC} = 5.5$ V, Minimum cycle			190		180		170	mA
I_{CC2}	Standby current	$V_{IH} = 2.4$ V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			2		2		2	mA
		$V_{IH} = V_{CC} - 0.2$ V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'418169		1		1		1	mA
			'418169P		500		500		500	μA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	$V_{CC} = 5.5$ V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			190		180		170	mA
I_{CC4}‡¶	Average EDO current	$V_{CC} = 5.5$ V, $\overline{RAS}$ low, $t_{HPC} = $ MIN, $\overline{xCAS}$ cycling			100		90		80	mA
I_{CC6}#	Self-refresh current	$\overline{xCAS} < 0.2$ V, $\overline{RAS} < 0.2$ V, Measured after t_{RASS} min			500		500		500	μA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms); CBR only	$t_{RC} = 125$ μs, $t_{RAS} \leq 300$ ns, $V_{CC} - 0.2$ V ≤ $V_{IH} \leq 6.5$ V, 0 V ≤ $V_{IL} \leq 0.2$ V, $\overline{W}$ and $\overline{OE} = V_{IH}$, Address and data stable			600		600		600	μA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS} = V_{IL}$
¶ Measured with a maximum of one address change while $\overline{xCAS} = V_{IH}$
# For TMS418169P only

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TMS426169/P

electrical characteristics over recommended ranges of supply voltage and operating free-air conditions (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†		'426169-60 '426169P-60		'426169-70 '426169P-70		'426169-80 '426169P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	$I_{OH} = -2$ mA	LVTTL	2.4		2.4		2.4		V
		$I_{OH} = -100$ µA	LVCMOS	$V_{CC}-0.2$		$V_{CC}-0.2$		$V_{CC}-0.2$		
V_{OL}	Low-level output voltage	$I_{OL} = 2$ mA	LVTTL		0.4		0.4		0.4	V
		$I_{OL} = 100$ µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	$V_{CC} = 3.6$ V, $V_I = 0$ V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	$V_{CC} = 3.6$ V, $V_O = 0$ V to V_{CC}, xCAS high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	$V_{CC} = 3.6$ V, Minimum cycle			90		80		70	mA
I_{CC2}	Standby current	$V_{IH} = 2$ V (LVTTL), After 1 memory cycle, $\overline{RAS}$ and xCAS high			1		1		1	mA
		$V_{IH} = V_{CC} - 0.2$ V (LVCMOS), After 1 memory cycle, $\overline{RAS}$ and xCAS high	'426169		500		500		500	µA
			'426169P		200		200		200	µA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	$V_{CC} = 3.6$ V, Minimum cycle, $\overline{RAS}$ cycling, xCAS high ($\overline{RAS}$-only refresh) $\overline{RAS}$ low after xCAS low (CBR)			90		80		70	mA
I_{CC4}‡¶	Average EDO current	$V_{CC} = 3.6$ V, t_{HPC} = MIN, $\overline{RAS}$ low, xCAS cycling			100		90		80	mA
I_{CC6}#	Self-refresh current	xCAS < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			250		250		250	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms), CBR only	$t_{RC} = 31.25$ µs, $t_{RAS} ≤ 300$ ns, $V_{CC} - 0.2$ V ≤ $V_{IH} ≤ 3.9$ V, 0 V ≤ $V_{IL} ≤ 0.2$ V, $\overline{W}$ and $\overline{OE} = V_{IH}$, Address and data stable			350		350		350	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while xCAS = V_{IH}
# For TMS426169P only

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TMS416169, TMS416169P, TMS418169, TMS418169P
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1048576-WORD BY 16-BIT EXTENDED DATA OUT HIGH-SPEED DRAMS

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TMS428169/P

electrical characteristics over recommended ranges of supply voltage and operating free-air conditions (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†		'428169-60 '428169P-60 MIN	MAX	'428169-70 '428169P-70 MIN	MAX	'428169-80 '428169P-80 MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2$ mA	LVTTL	2.4		2.4		2.4		V
		$I_{OH} = -100$ µA	LVCMOS	$V_{CC}-0.2$		$V_{CC}-0.2$		$V_{CC}-0.2$		
V_{OL}	Low-level output voltage	$I_{OL} = 2$ mA	LVTTL		0.4		0.4		0.4	V
		$I_{OL} = 100$ µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	$V_{CC} = 3.6$ V, $V_I = 0$ V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	$V_{CC} = 3.6$ V, $V_O = 0$ V to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	$V_{CC} = 3.6$ V, Minimum cycle			190		180		170	mA
I_{CC2}	Standby current	$V_{IH} = 2$ V (LVTTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			1		1		1	mA
		$V_{IH} = V_{CC} - 0.2$ V (LVCMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'428169		500		500		500	µA
			'428169P		200		200		200	µA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	$V_{CC} = 3.6$ V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$-only refresh) $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			190		180		170	mA
I_{CC4}‡¶	Average EDO current	$V_{CC} = 3.6$ V, $\overline{RAS}$ low, $t_{HPC} = $ MIN, $\overline{xCAS}$ cycling			100		90		80	mA
I_{CC6}#	Self-refresh current	$\overline{xCAS} < 0.2$ V, $\overline{RAS} < 0.2$ V, Measured after t_{RASS} min			250		250		250	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms), CBR only	$t_{RC} = 125$ µs, $t_{RAS} ≤ 300$ ns, $V_{CC} - 0.2$ V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE} = V_{IH}$, Address and data stable			350		350		350	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS} = V_{IL}$
¶ Measured with a maximum of one address change while $\overline{xCAS} = V_{IH}$
# For TMS428169P only

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capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A11		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, x$\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_O	Output capacitance		7	pF

NOTE 3: V_{CC} = 5 V ± 0.5 V or 3.3 V ± 0.3 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'4xx169-60 '4xx169P-60		'4xx169-70 '4xx169P-70		'4xx169-80 '4xx169P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address (see Note 4)		30		35		40	ns
t_{CAC}	Access time from x$\overline{CAS}$ low (see Note 4)		15		18		20	ns
t_{CPA}	Access time from column precharge (see Note 4)		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low (see Note 4)		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low (see Note 4)		15		18		20	ns
t_{CLZ}	Delay time, x$\overline{CAS}$ low to output in low-impedance state	0		0		0		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 5)	3	15	3	18	3	20	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high (see Note 5)	3	15	3	18	3	20	ns
t_{CEZ}	Output disable time after $\overline{CAS}$ high (see Note 5)	3	15	3	18	3	20	ns
t_{WEZ}	Output disable time after $\overline{W}$ low (see Note 5)	3	15	3	18	3	20	ns

NOTES: 4. Access times for TMS42x169 are measured with output reference levels of V_{OH} = 2 V and V_{OL} = 0.8 V.
        5. Maximum t_{REZ}, t_{CEZ}, t_{WEZ} and t_{OEZ} are specified when the output is no longer driven.

EDO timing requirements over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	'4xx169-60		'4xx169-70		'4xx169-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{HPC}	Cycle time, EDO page-mode read or write	25		30		35		ns
t_{PRWC}	Cycle time, EDO read-write	80		90		100		ns
t_{CSH}	Hold time, x$\overline{CAS}$ from $\overline{RAS}$	50		55		60		ns
t_{CHO}	Hold time, $\overline{OE}$ from x$\overline{CAS}$	10		10		10		ns
t_{DOH}	Hold time, output from x$\overline{CAS}$	3		3		3		ns
t_{CAS}	Pulse duration, x$\overline{CAS}$	10	10000	12	10000	15	10000	ns
t_{WPE}	Pulse duration, $\overline{W}$ (output disable only)	5		5		5		ns
t_{OCH}	Setup time, $\overline{OE}$ before x$\overline{CAS}$	10		10		10		ns
t_{CP}	Precharge time, x$\overline{CAS}$	5		5		5		ns
t_{OEP}	Precharge time, $\overline{OE}$	5		5		5		ns

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timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4xx169-60 '4xx169P-60		'4xx169-70 '4xx169P-70		'4xx169-80 '4xx169P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read (see Note 6)	110		130		150		ns
t_{WC}	Cycle time, write (see Note 6)	110		130		150		ns
t_{RWC}	Cycle time, read-write (see Note 6)	150		175		200		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 7)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 7)	60	10 000	70	10 000	80	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{xCAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 8)	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{xCAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{xCAS}$ high	10		12		15		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	10		12		15		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{xCAS}$ low (early-write operation only)	0		0		0		ns
t_{CAH}	Hold time, column address after $\overline{xCAS}$ low	10		15		15		ns
t_{DH}	Hold time, data (see Note 8)	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{xCAS}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 9)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{xCAS}$ low (early-write operation only)	10		15		15		ns
t_{CLCH}	Hold time, $\overline{xCAS}$ low to $\overline{xCAS}$ high	5		5		5		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{xCAS}$ precharge	35		40		45		ns
t_{OEH}	Hold time, $\overline{OE}$ command	15		18		20		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	10		10		10		ns
t_{CHS}	Hold time, $\overline{xCAS}$ low after $\overline{RAS}$ high (self refresh)	– 50		– 50		– 50		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)	55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ high (xCBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{xCAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ high	50		55		60		ns
t_{CSR}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ low (xCBR refresh only)	5		5		5		ns
t_{CWD}	Delay time, $\overline{xCAS}$ low to $\overline{W}$ low (read-write operation only)	40		46		50		ns
t_{OED}	Delay time, $\overline{OE}$ to data	15		18		20		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{xCAS}$ high	20		25		30		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ low (see Note 10)	20	45	20	52	20	60	ns

NOTES: 6. All cycle times assume t_T = 5 ns.
7. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
8. Referenced to the later of $\overline{xCAS}$ or $\overline{W}$ in write operations
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. The maximum value is specified only to assure access time.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

			'4xx169-60 '4xx169P-60		'4xx169-70 '4xx169P-70		'4xx169-80 '4xx169P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{RPC}	Delay time, $\overline{RAS}$ high to $x\overline{CAS}$ low		0		0		0		ns
t_{RSH}	Delay time, $x\overline{CAS}$ low to $\overline{RAS}$ high		10		12		15		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)		85		98		110		ns
t_{CPW}	Delay time, $\overline{W}$ low after $x\overline{CAS}$ precharge (read-write operation only)		60		68		75		ns
t_{RASS}	Pulse duration, self-refresh entry from $\overline{RAS}$ low		100		100		100		µs
t_{RPS}	Pulse duration, $\overline{RAS}$ precharge after self refresh		110		130		150		ns
t_{REF}	Refresh time interval	'4x6169		64		64		64	ms
		'4x6169P		128		128		128	
		'4x8169		16		16		16	ms
		'4x8169P		128		128		128	
t_T	Transition time		2	30	2	30	2	30	ns

PARAMETER MEASUREMENT INFORMATION

(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT
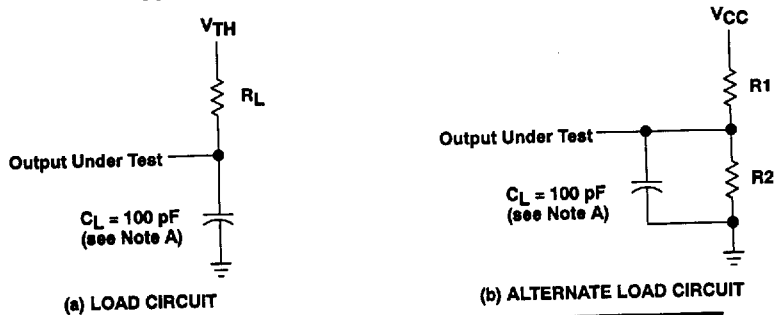
DEVICE	V_{CC} (V)	R1 (Ω)	R2 (Ω)	V_{TH} (V)	R_L (Ω)
41x169/P	5	828	295	1.31	218
42x169/P	3.3	1178	868	1.4	500

NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

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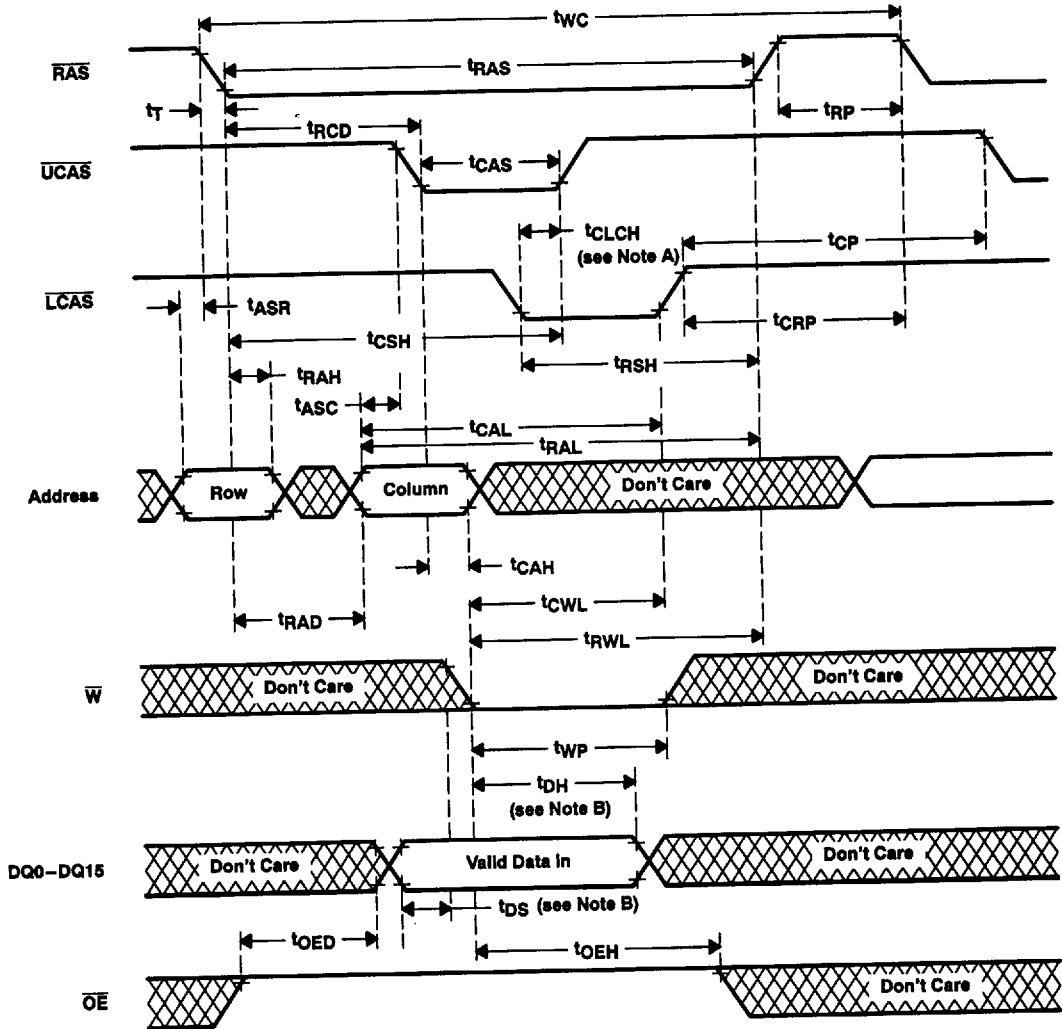8961725 0085071 745

PARAMETER MEASUREMENT INFORMATION

PRODUCT PREVIEW
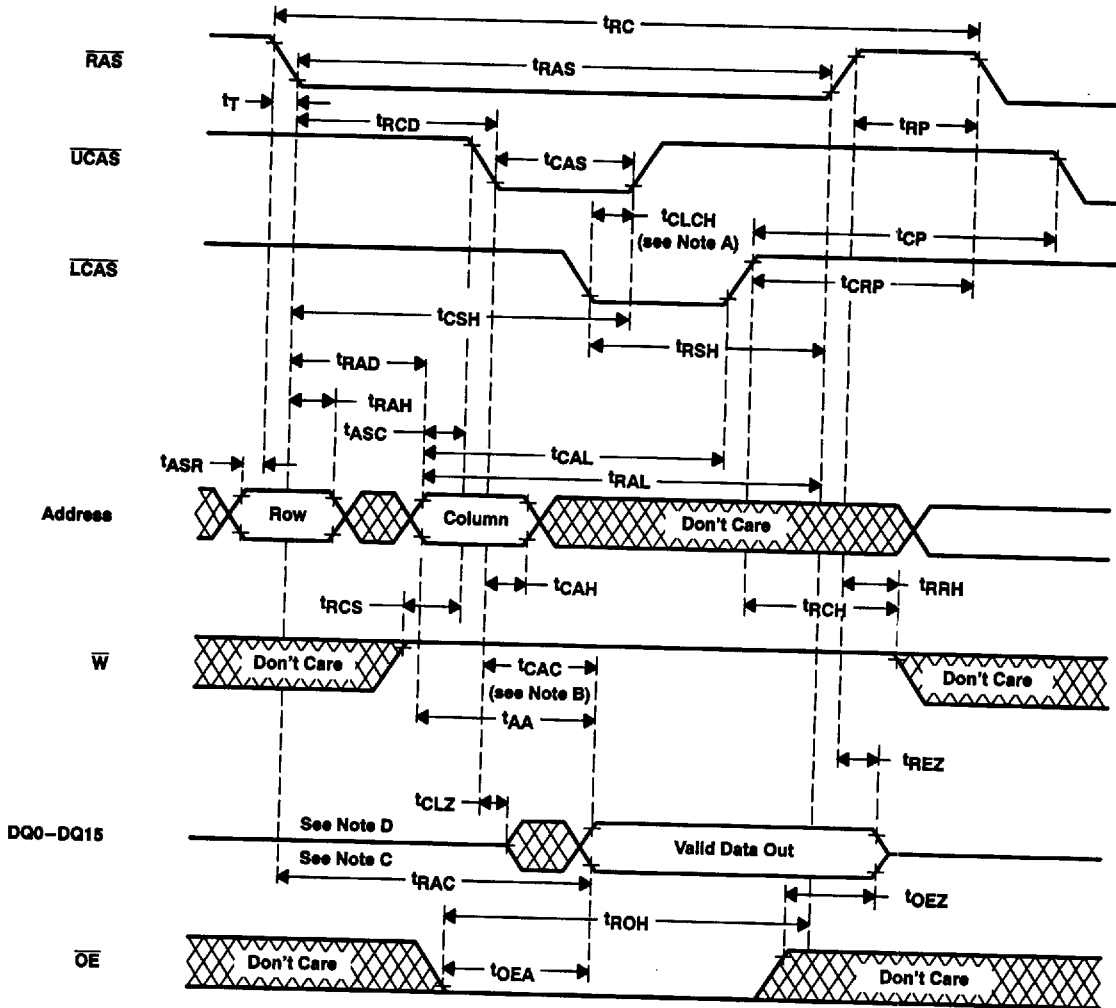
NOTES: B. To hold the address latched by the first xCAS going low, the parameter t_{CLCH} must be met.
C. t_{CAC} is measured from xCAS to its corresponding DQx.
D. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
E. xCAS order is arbitrary.

Figure 2. Read-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

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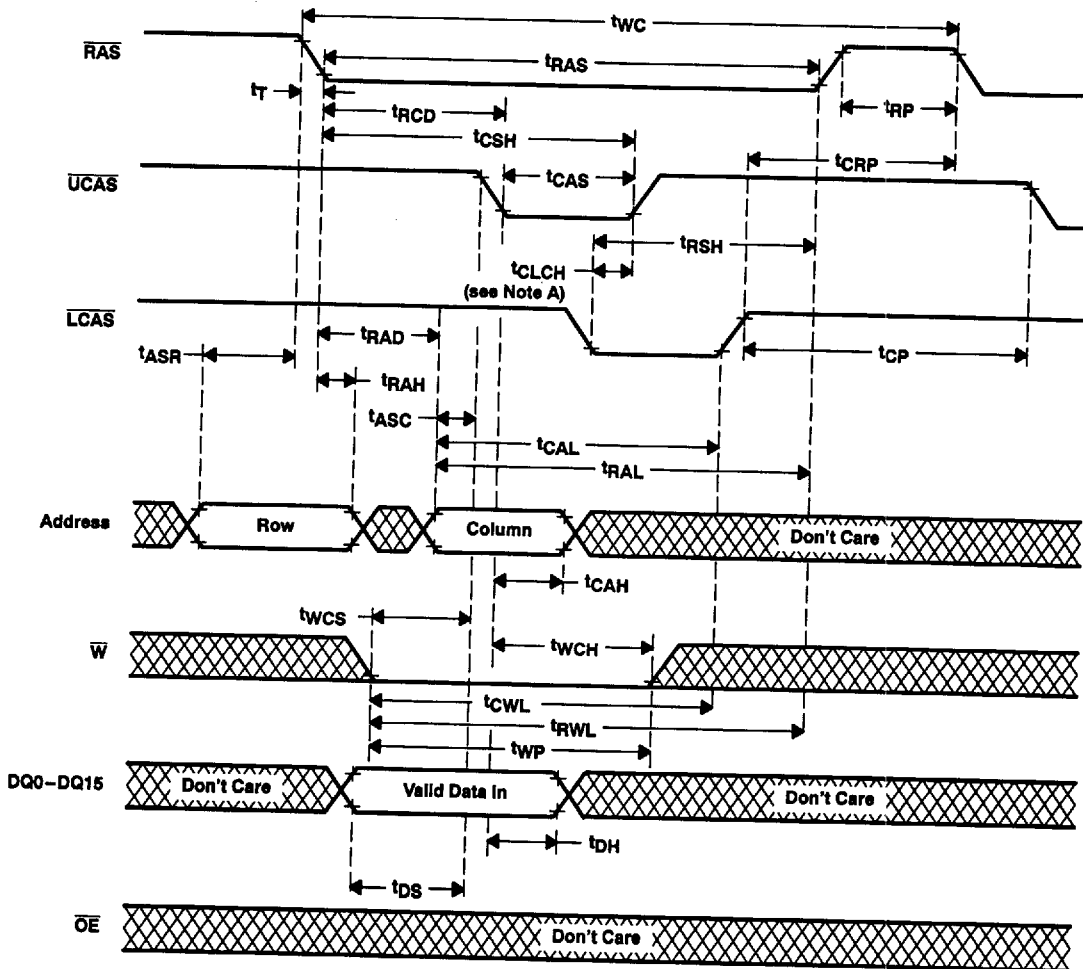

Figure 3. Write-Cycle Timing

NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Referenced to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last
C. $\overline{xCAS}$ order is arbitrary.

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PARAMETER MEASUREMENT INFORMATION

NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 4. Early-Write-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

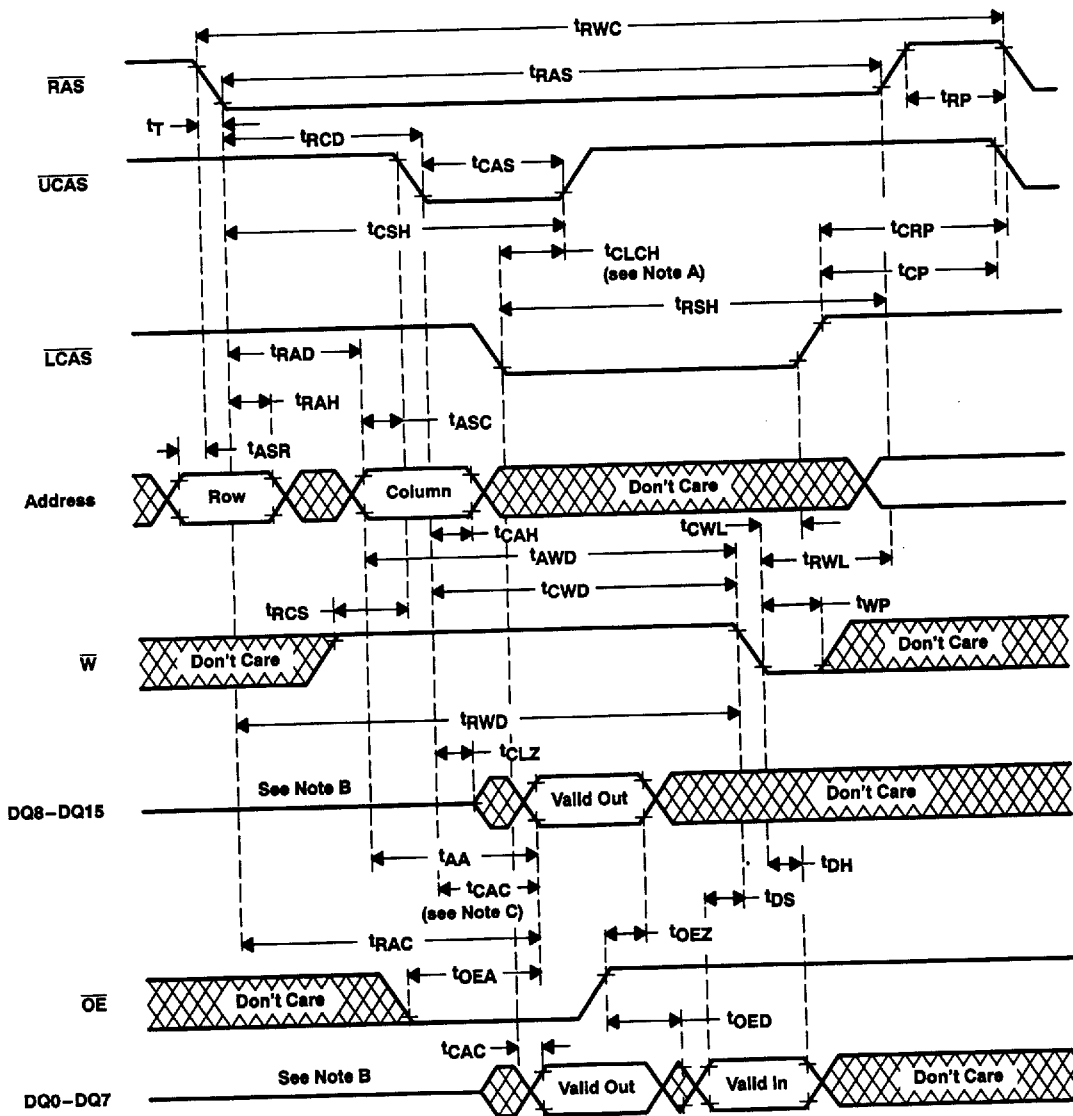**NOTES:**
A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
C. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
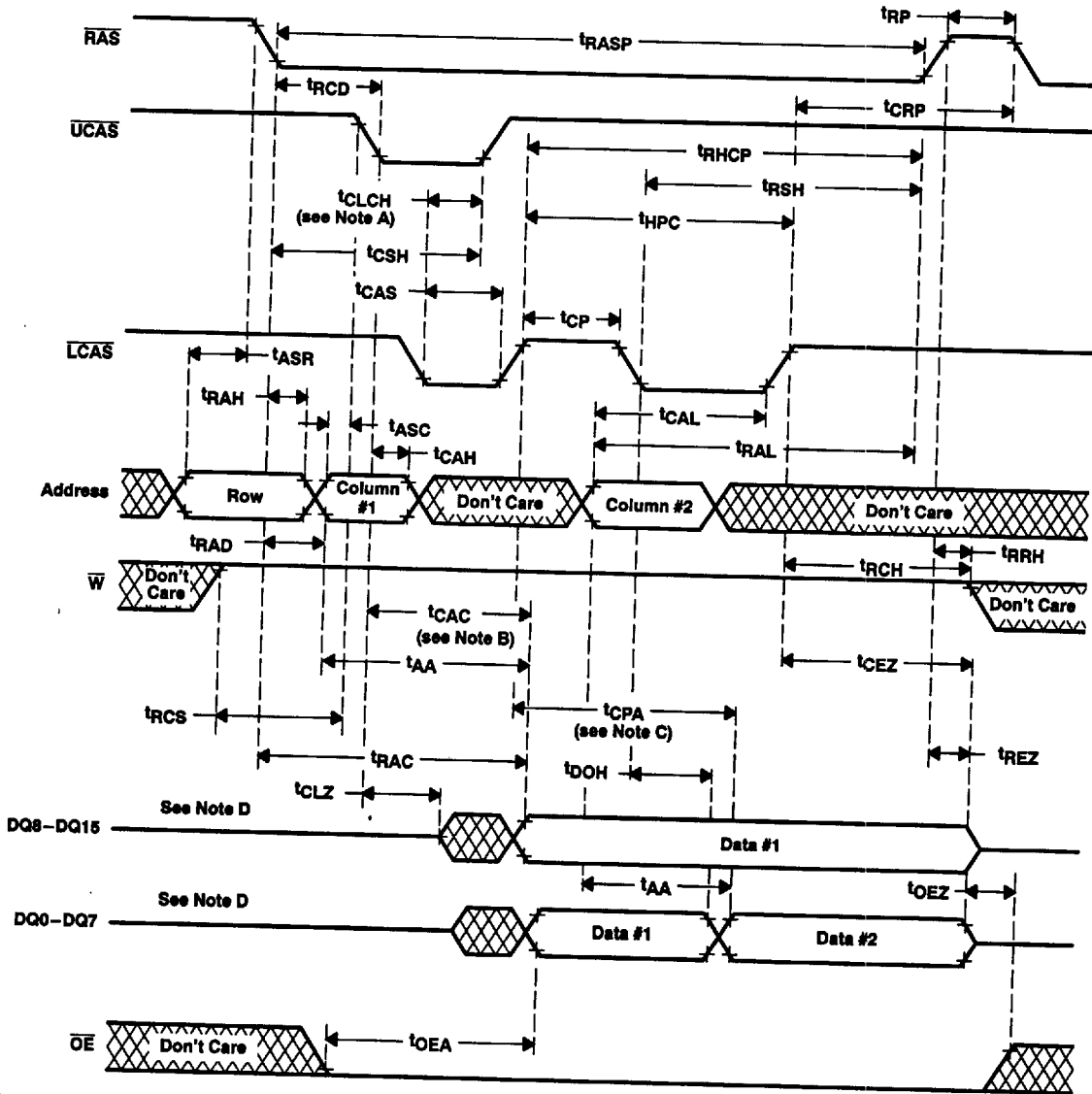D. $\overline{xCAS}$ order is arbitrary.

Figure 5. Read-Modify-Write-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION
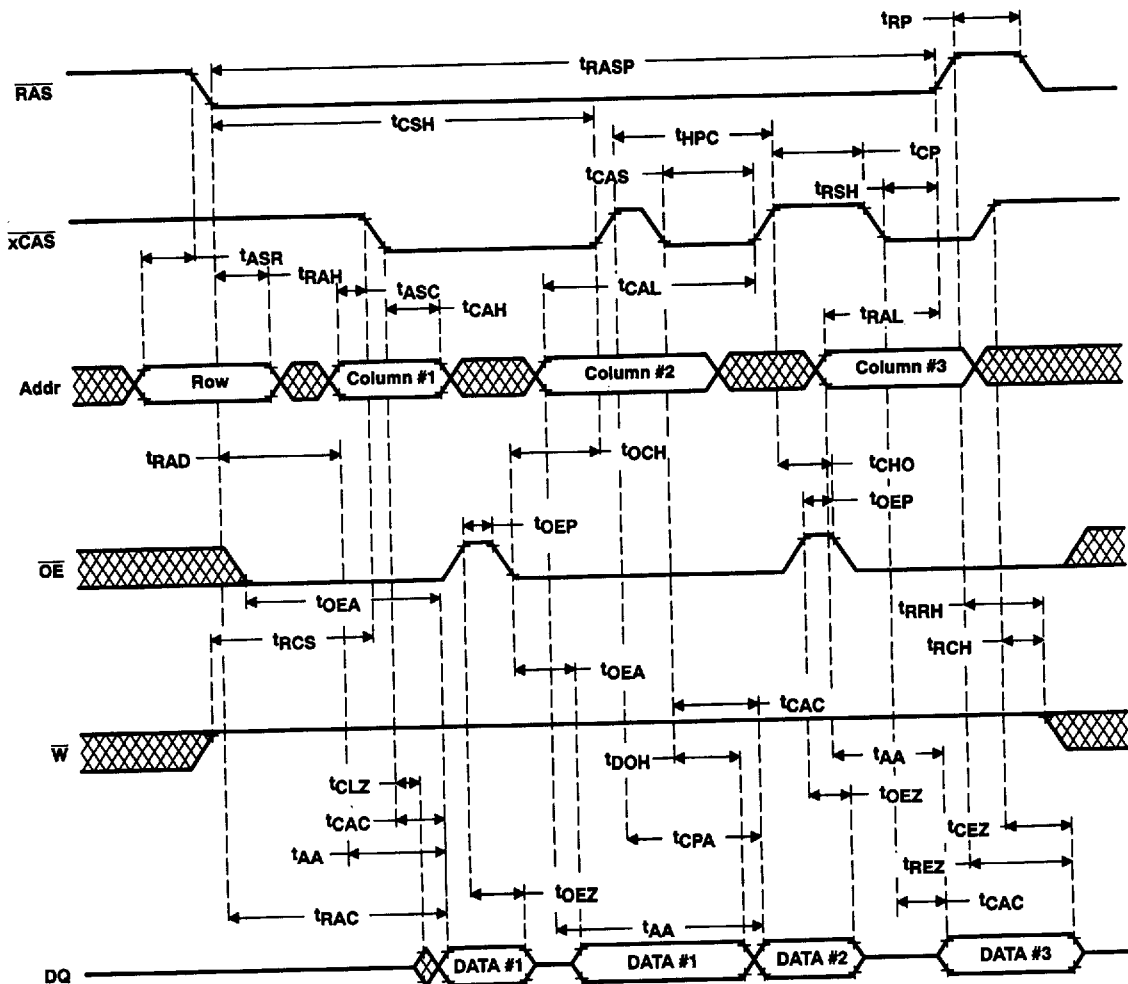
PRODUCT PREVIEW

NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. Access time is t_{CPA} or t_{AA} dependent.
D. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
E. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write- and read-modify-write-timing specifications are not violated.
F. $\overline{xCAS}$ order is arbitrary.

Figure 6. Extended-Data-Out Read-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

Figure 7. Extended-Data-Out Read-Cycle Timing With $\overline{OE}$ Control

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PARAMETER MEASUREMENT INFORMATION
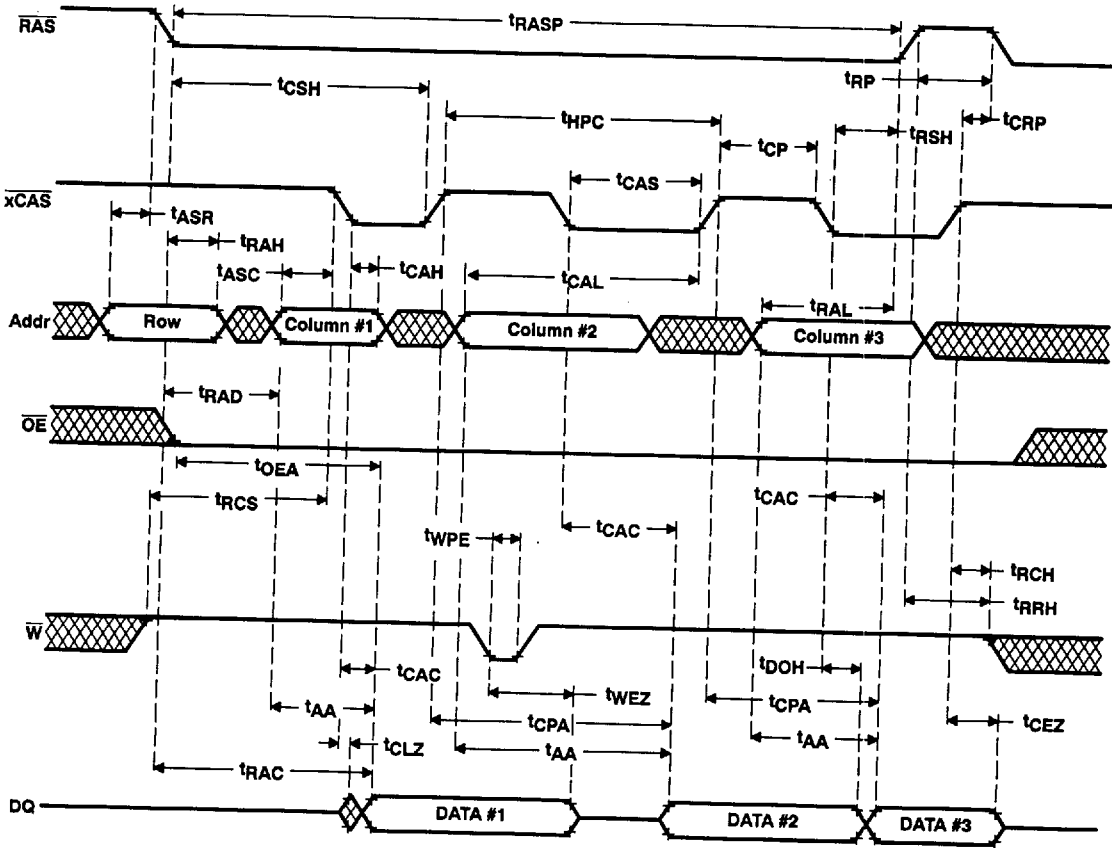
Figure 8. Extended-Data-Out Read-Cycle Timing With $\overline{W}$ Control

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PARAMETER MEASUREMENT INFORMATION

Figure 9. Extended-Data-Out Write-Cycle Timing
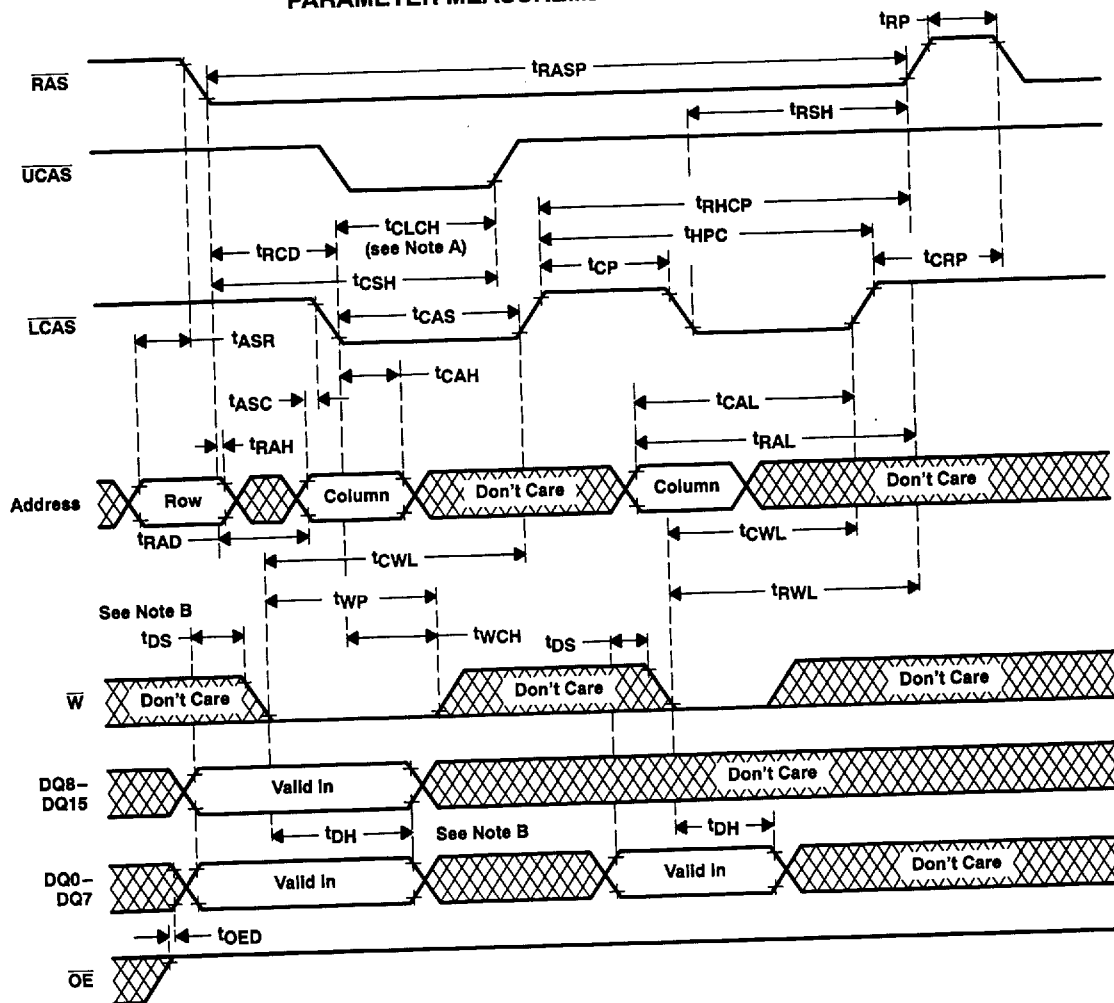
PRODUCT PREVIEW

NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
   B. Referenced to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last
   C. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read- and read-modify-write-timing specifications are not violated.
   D. $\overline{xCAS}$ order is arbitrary.

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PARAMETER MEASUREMENT INFORMATION
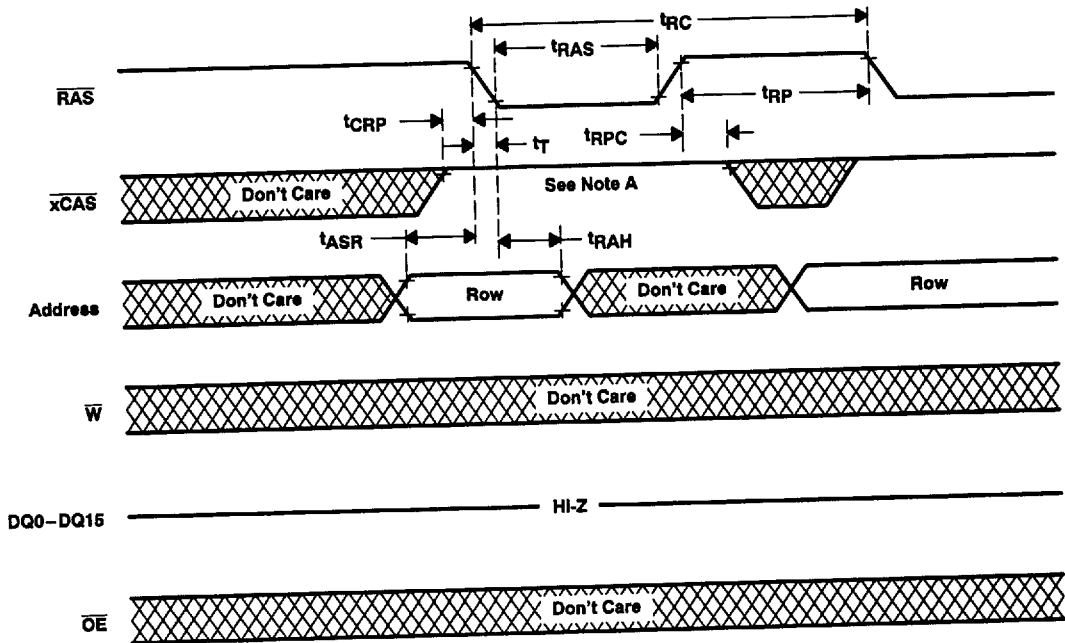
PRODUCT PREVIEW

NOTES:
A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. Access time is t_{CPA}- or t_{AA}-dependent.
C. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
D. $\overline{\text{xCAS}}$ order is arbitrary.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read- and write-cycle timing specifications are not violated.
F. t_{CAC} is measured from $\overline{\text{xCAS}}$ to its corresponding DQx.

Figure 10. Extended-Data-Out Read-Modify-Write-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

NOTE A: All xCAS must be high.

Figure 11. RAS-Only Refresh-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

Figure 12. Hidden-Refresh-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

NOTE A: Any $\overline{xCAS}$ can be used.

Figure 13. Automatic-xCBR-Refresh-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

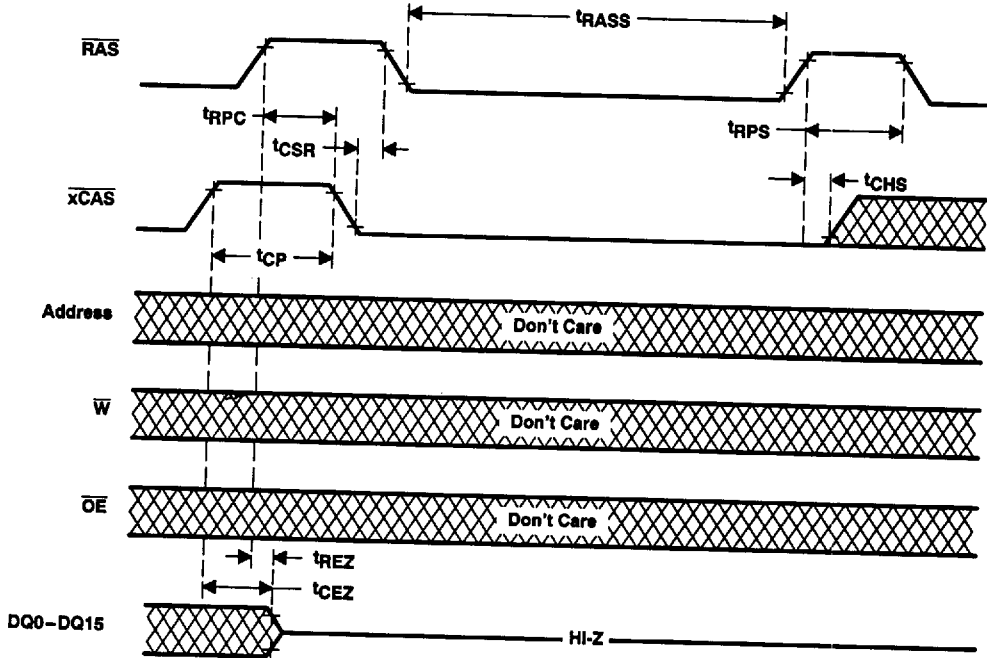Figure 14. Self-Refresh-Cycle Timing

device symbolization (TMS416169P illustrated)

- Speed (-60, -70, -80)
- Low-Power/Self-Refresh Designator (Blank or P)
- Package Code
- Assembly Site Code
- Lot Traceability Code
- Month Code
- Year Code
- Die Revision Code
- Wafer Fab Code

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