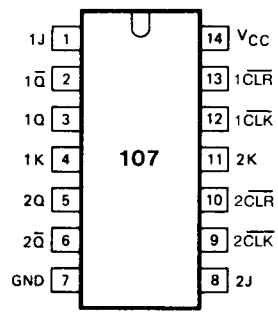
GD54/74HC107, GD54/74HCT107

DUAL J-K FLIP-FLOPS WITH CLEAR

General Description

These devices are identical in pinout to the 54/74LS107. They consist of two J-K flip-flops with individual J, K, clock, and clear inputs. These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Both Q and $\overline{Q}$ outputs are available from each flip-flow clear is independent of the clock and accomplished by a low on the input. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
  for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 40μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODE	INPUTS				OUTPUTS	
	n$\overline{CLR}$	n$\overline{CLK}$	J	K	Q	$\overline{Q}$
asynchronous reset	L	X	X	X	L	H
toggle	H	↓	h	h	q	$\overline{q}$
load "0" (reset)	H	↓	l	h	L	H
load "1" (set)	H	↓	h	l	H	L
hold "no change"	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CLK transition
X = don't care
↓ = HIGH-to-LOW CLK transition

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		−0.5	+7	V
I_{IK} I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		|20|	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		|25|	mA
I_{CC}	DC V_{CC} or GND current			|50|	mA
T_{stg}	Storage temperature range		−65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW K^{-1}		500	mW
T_L	Lead temperature	At distance 1.16±1.32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC}: GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A: GD74 Types GD54 Types	−40 −55	+85 +125	°C
Input Rise and Fall times t_r, t_f: GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

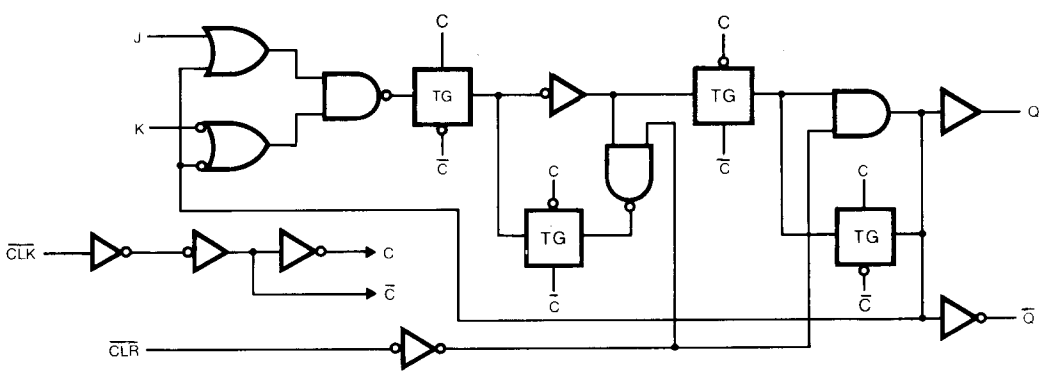


Fig. 1 Logic diagram (one flip flop)

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION		V_{CC} (V)	T_A=25°C			GD74HC107		GD54HC107		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage			2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V_{IL}	LOW level input voltage			2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V_{OH}	HIGH level output voltage	V_{IN}=V_{IH} or V_{IL}	I_{OH}=−20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
			I_{OH}=−4mA I_{OH}=−5.2mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
V_{OL}	LOW level output voltage	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
			I_{OL}=4mA I_{OL}=5.2mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4	
$\|I_{IN}\|$	Input leakage Current	V_{IN}=V_{CC} or GND		6.0			0.1		1.0		1.0	μA
I_{CC}	Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{out}=0μA		6.0			4		40		80	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION		V_{CC} (V)	T_A=25°C			GD74HCT107		GD54HCT107		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage			4.5 to 5.5	2.0			2.0		2.0		V
V_{IL}	LOW level input voltage			4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	HIGH level output voltage	V_{IN}=V_{IH} or V_{IL}	I_{OH}=−20μA	4.5	4.4	4.5		4.4		4.4		V
			I_{OH}=−4mA	4.5	3.98	4.3		3.84		3.7		
V_{OL}	LOW level output voltage	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	4.5			0.1		0.1		0.1	V
			I_{OL}=4mA	4.5		0.17	0.26		0.33		0.4	
$\|I_{IN}\|$	Input leakage Current	V_{IN}=V_{CC}or GND		5.5			0.1		1.0		1.0	μA
I_{CC}	Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{out}=0μA		5.5			4		40		80	μA

Timing Requirements for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25°C$ MIN.	$T_A=25°C$ TYP.	$T_A=25°C$ MAX.	GD74HC107 MIN.	GD74HC107 MAX.	GD54HC107 MIN.	GD54HC107 MAX.	UNIT
t_w	Pulse width	$\overline{CLR}$ (low)	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
		$\overline{CLK}$ (high or low)	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Set up Time	Data to $\overline{CLK}$↑	2.0	60	30		80		100		ns
			4.5	15	10		18		20		
			6.0	14	8		16		18		
t_{rec}	Recovery time	$\overline{CLR}$ to $\overline{CLK}$	2.0	5	0		5		5		ns
			4.5	5	0		5		5		
			6.0	5	0		5		5		
t_h	Hold Time	Data to $\overline{CLK}$↑	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25°C$ MIN.	$T_A=25°C$ TYP.	$T_A=25°C$ MAX.	GD54HC107 MIN.	GD54HC107 MAX.	GD74HC107 MIN.	GD74HC107 MAX.	UNIT
f_{max}	Maximum Clock Pulse Frequency	2.0	6	20		5		4		MHz
		4.5	30	65		25		20		
		6.0	35	75		30		25		
t_{PLH} / t_{PHL}	Propagation Delay Time $n\overline{CLK}$ to nQ	2.0		46	160		200		240	ns
		4.5		15	30		40		50	
		6.0		14	28		35		45	
t_{PLH} / t_{PHL}	Propagation Delay Time $n\overline{CLK}$ to $n\overline{Q}$	2.0		50	160		200		240	ns
		4.5		17	30		40		50	
		6.0		16	28		35		45	
t_{PLH} / t_{PHL}	Propagation Delay time $n\overline{CLR}$ to nQ, $n\overline{Q}$	2.0		45	155		190		230	ns
		4.5		15	28		38		45	
		6.8		14	26		34		40	
t_{TLH} / t_{THL}	Output Transition time	2.0		25	70		85		100	ns
		4.5		8	15		18		22	
		6.0		7	13		16		19	

Timing Requirements for HCT: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25°C$			GD74HCT107		GD54HCT107		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{CLR}$ (low)	4.5	18	10		20		25		ns
		$\overline{CLK}$ (high or low)	4.5	10	10		20		25		ns
t_{su}	Set up Time	Data to $\overline{CLK}$↑	4.5	15	10		18		20		ns
t_{rec}	Recovery time	$\overline{CLR}$ to $\overline{CLK}$	4.5	5	0		5		5		ns
t_h	Hold Time	Data to $\overline{CLK}$↑	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25°C$			GD74HCT107		GD54HCT107		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	27	54		22		18		MHz
t_{PLH} / t_{PHL}	Propagation Delay Time $n\overline{CLK}$ to nQ	4.5		17	30		40		50	ns
t_{PLH} / t_{PHL}	Propagation Delay Time $n\overline{CLK}$ to $n\overline{Q}$	4.5		17	30		40		50	ns
t_{PLH} / t_{PHL}	Propagation Delay Time $n\overline{CLR}$ to nQ, $n\overline{Q}$	4.5		15	28		38		45	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		8	15		18		22	ns

AC Waveforms

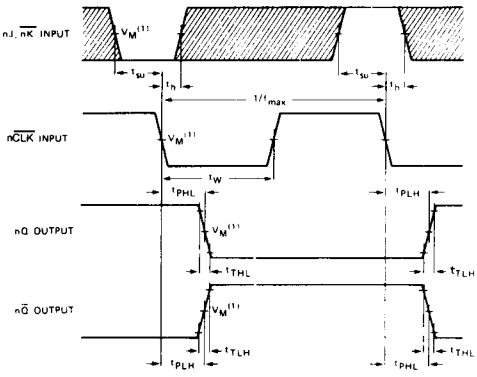


Fig. 2 Waveforms showing the clock (nCLK) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nJ, nK to nCLK set-up, the nCLK to nJ, nK hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 2
The shaded areas indicate when the input is permitted to change for predictable output performance.

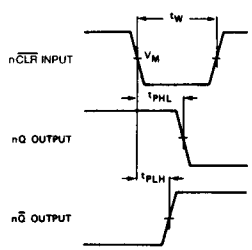


Fig. 3 Waveforms showing the clear (nCLR) input to ouput (nQ, nQ̄) propagation delays and the clear pulse width.

Note to AC waveforms

(1) HC : V_M=50%; V_I=GND to V_{CC}.
HCT : V_M=1.3V; V_I=GND to 3V.