



# FAST CMOS 16-BIT LATCHED TRANSCEIVER

**IDT54/74FCT16543T/AT/CT/ET**

## FEATURES:

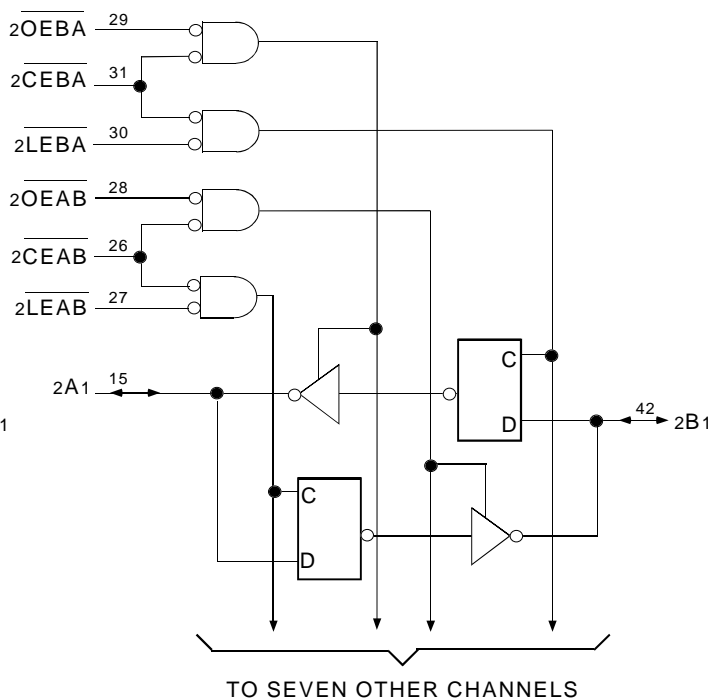
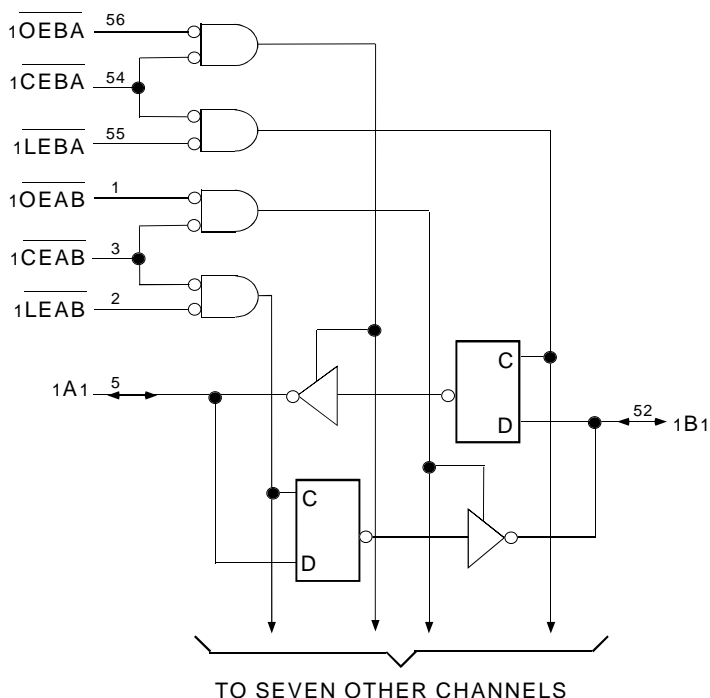
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical tsk(o) (Output Skew) < 250ps
- Low input and output leakage ≤ 1μA (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- VCC = 5V ± 10%
- High drive outputs (-32mA IOH, 64mA IOL)
- Power off disable outputs permit "live insertion"
- Typical VOLP (Output Ground Bounce) < 1.0V at VCC = 5V, TA = 25°C
- Available in the following packages:
  - Industrial: SSOP, TSSOP, TVSOP
  - Military: CERPACK

## DESCRIPTION:

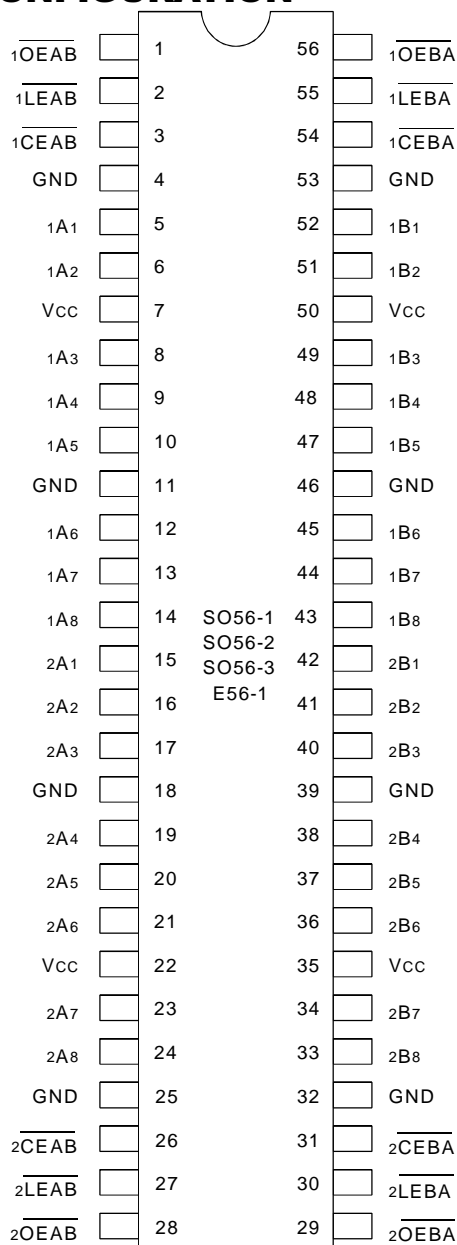
The FCT16543T 16-bit latched transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type latched transceivers with separate input and output control to permit independent control of data flow in either direction. For example, the A-to-B Enable (xCEAB) must be low in order to enter data from the A port or to output data from the B port. xLEAB controls the latch function. When xLEAB is low, the latches are transparent. A subsequent low-to-high transition of xLEAB signal puts the A latches in the storage mode. xOEAB performs output enable function on the B port. Data flow from the B port to the A port is similar but requires using xCEBA, xLEBA, and xOEBA inputs. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16543T is ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP/ CERPACK  
TOP VIEW

## PIN DESCRIPTION

Pin Names	Description
$\overline{xOEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{xOEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{xCEAB}$	A-to-B Enable Input (Active LOW)
$\overline{xCEBA}$	B-to-A Enable Input (Active LOW)
$\overline{xLEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{xLEBA}$	B-to-A Latch Enable Input (Active LOW)
$xAx$	A-to-B Data Inputs or B-to-A 3-State Outputs
$xBx$	B-to-A Data Inputs or A-to-B 3-State Outputs

## ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{CC}+0.5$	V
TSTG	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-60 to +120	mA

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### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXX Output and I/O terminals.
- Output and I/O terminals for FCT162XXX.

## CAPACITANCE ( $T_A = +25^\circ\text{C}$ , $f = 1.0\text{MHz}$ )

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	$V_{IN} = 0V$	3.5	6	pF
C <sub>OUT</sub>	Output Capacitance	$V_{OUT} = 0V$	3.5	8	pF

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### NOTE:

- This parameter is measured at characterization but not tested.

## FUNCTION TABLE<sup>(1,2)</sup>

For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$\overline{xCEAB}$	$\overline{xLEAB}$	$\overline{xOEAB}$	$xAx$ to $xBx$	$xBx$
H	X	X	Storing	High Z
X	H	X	Storing	X
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs
L	L	H	Transparent	High Z
L	H	H	Storing	High Z

### NOTES:

- \* Before  $\overline{xLEAB}$  LOW-to-HIGH Transition  
H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care
- A-to-B data flow shown; B-to-A flow control is the same, except using  $\overline{xCEBA}$ ,  $\overline{xLEBA}$  and  $\overline{xOEBA}$ .

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$ ; Military:  $T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current (Input pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
	Input HIGH Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{IL}$	Input LOW Current (Input pins) <sup>(5)</sup>		$V_I = \text{GND}$	—	—	$\pm 1$	
	Input LOW Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{OZH}$	High Impedance Output Current	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$	(3-State Output pins) <sup>(5)</sup>		$V_O = 0.5\text{V}$	—	—	$\pm 1$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-80	-140	-250	mA
$V_H$	Input Hysteresis	—		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	5	500	$\mu\text{A}$

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## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_O$	Output Drive Current	$V_{CC} = \text{Max.}, V_O = 2.5\text{V}^{(3)}$		-50	—	-180	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -12\text{mA MIL}$	2.4	3.5	—	V
			$I_{OH} = -15\text{mA IND}$				
			$I_{OH} = -24\text{mA MIL}$ $I_{OH} = -32\text{mA IND}^{(4)}$	2	3	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 48\text{mA MIL}$ $I_{OL} = 64\text{mA IND}$	—	0.2	0.55	V
$I_{OFF}$	Input/Output Power Off Leakage <sup>(5)</sup>	$V_{CC} = 0\text{V}, V_{IN} \text{ or } V_O \leq 4.5\text{V}$		—	—	$\pm 1$	$\mu\text{A}$

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^{\circ}\text{C}$ .

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open $\overline{xCEAB}$ and $\overline{xOEAB} = \text{GND}$ $\overline{xCEBA} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	$\mu\text{A}/\text{MHz}$
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xLEAB}$ , $\overline{xCEAB}$ and $\overline{xOEAB} = \text{GND}$ $\overline{xCEBA} = V_{CC}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	1.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	0.9	2.3	
		$V_{CC} = \text{Max.}$ , Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xLEAB}$ , $\overline{xCEAB}$ and $\overline{xOEAB} = \text{GND}$ $\overline{xCEBA} = V_{CC}$ Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2.4	4.5 <sup>(5)</sup>	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.4	16.5 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or  $\text{GND}$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V)$   
 $D_H = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } D_H$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition <sup>(1)</sup>	FCT16543T				FCT16543AT				Unit
			Ind.		Mil.		Ind.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPLH tPHL	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50pF RL = 500Ω	1.5	8.5	1.5	10	1.5	6.5	1.5	7.5	ns
tPLH tPHL	Propagation Delay xLEBA to xAx, xLEAB to xBx		1.5	12.5	1.5	14	1.5	8	1.5	9	ns
tpZH tpZL	Output Enable Time xOEBA or xOEAB to xAx or xBx xCEBA or xCEAB to xAx or xBx		1.5	12	1.5	14	1.5	9	1.5	10	ns
tPHZ tPLZ	Output Disable Time xOEBA or xOEAB to xAx or xBx xCEBA or xCEAB to xAx or xBx		1.5	9	1.5	13	1.5	7.5	1.5	8.5	ns
tsu	Set-up Time HIGH or LOW xAx or xBx to xLEBA or xLEAB		2	—	3	—	2	—	2	—	ns
th	Hold Time HIGH or LOW xAx or xBx to xLEBA or xLEAB		2	—	2	—	2	—	2	—	ns
tw	xLEBA or xLEAB Pulse Width LOW		4	—	5	—	4	—	5	—	ns
tsk(o)	Output Skew <sup>(3)</sup>		—	0.5	—	0.5	—	0.5	—	0.5	ns

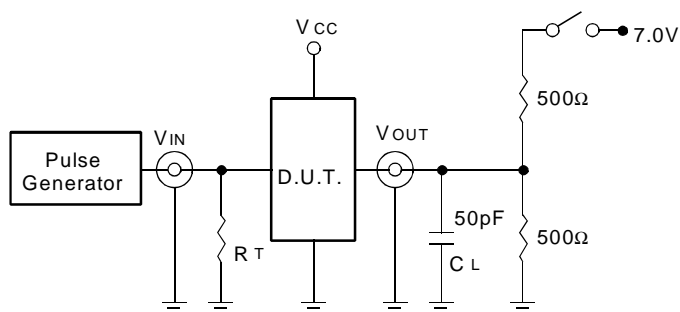
Symbol	Parameter	Condition <sup>(1)</sup>	FCT16543CT				FCT16543ET				Unit
			Ind.		Mil.		Ind.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPLH tPHL	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50pF RL = 500Ω	1.5	5.1	1.5	6.1	1.5	3.4	—	—	ns
tPLH tPHL	Propagation Delay xLEBA to xAx, xLEAB to xBx		1.5	5.6	1.5	8	1.5	3.7	—	—	ns
tpZH tpZL	Output Enable Time xOEBA or xOEAB to xAx or xBx xCEBA or xCEAB to xAx or xBx		1.5	7.8	1.5	9	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time xOEBA or xOEAB to xAx or xBx xCEBA or xCEAB to xAx or xBx		1.5	6.5	1.5	7.5	1.5	4	—	—	ns
tsu	Set-up Time, HIGH or LOW xAx or xBx to xLEBA or xLEAB		2	—	2	—	1	—	—	—	ns
th	Hold Time HIGH or LOW xAx or xBx to xLEBA or xLEAB		2	—	2	—	1	—	—	—	ns
tw	xLEBA or xLEAB Pulse Width LOW		4	—	5	—	3 <sup>(4)</sup>	—	—	—	ns
tsk(o)	Output Skew <sup>(3)</sup>		—	0.5	—	0.5	—	0.5	—	—	ns

### NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

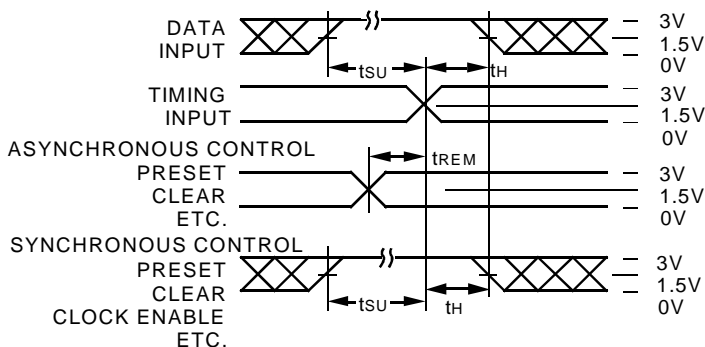
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#### DEFINITIONS:

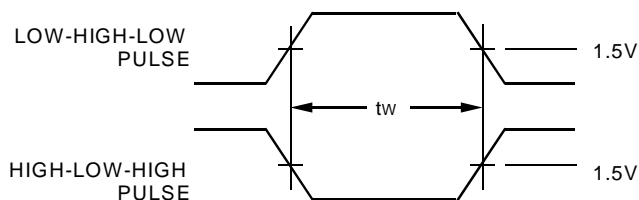
CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

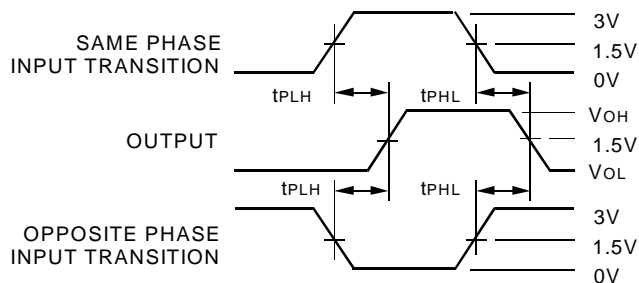
### SET-UP, HOLD, AND RELEASE TIMES



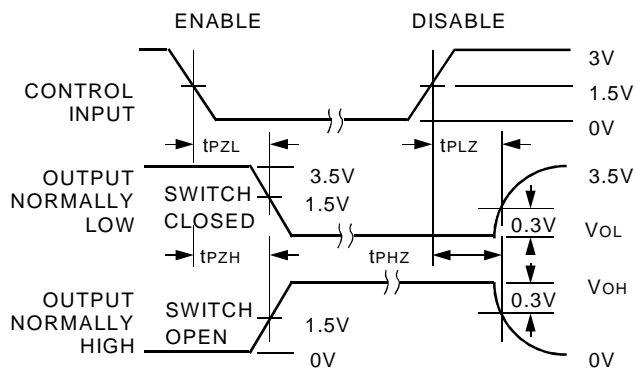
### PULSE WIDTH



### PROPAGATION DELAY



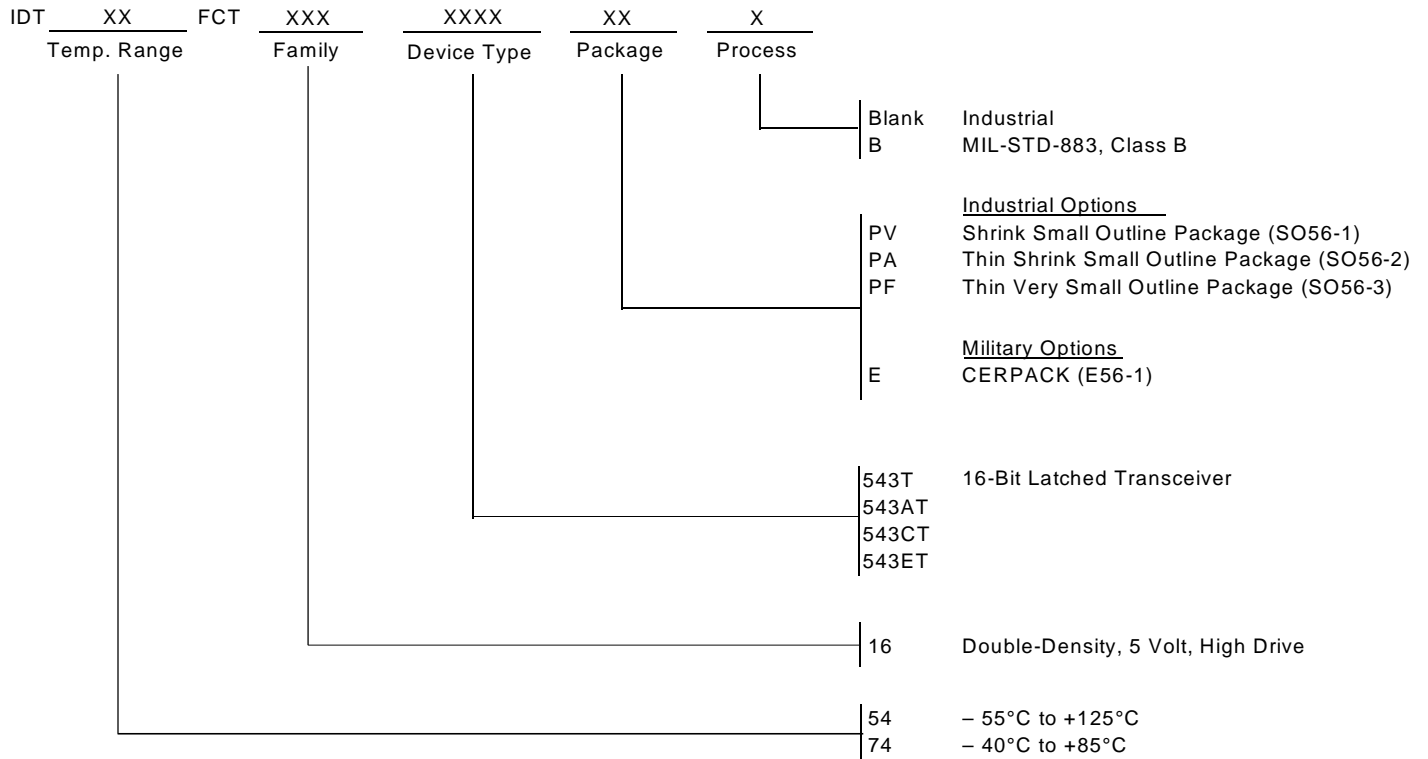
### ENABLE AND DISABLE TIMES



#### NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_f \leq 2.5\text{ns}$ ;  $t_r \leq 2.5\text{ns}$ .

**ORDERING INFORMATION**



**CORPORATE HEADQUARTERS**  
 2975 Stender Way  
 Santa Clara, CA 95054

**for SALES:**  
 800-345-7015 or 408-727-6116  
 fax: 408-492-8674  
 www.idt.com\*

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