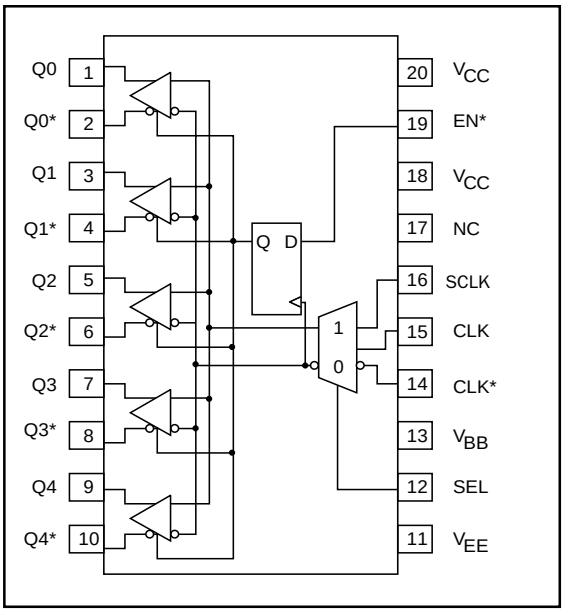
Description

The SK10/100EL14W is a 1:5 Clock Distribution Chip designed specifically for low skew clock distribution applications. This device is fully compatible with MC100EL14 and MC100LVEL14.

The device can be driven by either differential or single-ended ECL/PECL input signals. The SK10/100EL14W provides a V_{BB} output for either single-ended use or DC bias for AC coupling to the device. V_{BB} is an output pin and should be used as a bias for the EL14W as its current sink/source capability is limited. Whenever used, V_{BB} should be bypassed to VCC via a 0.01 µF capacitor.

The EL14W features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input. The Common Enable pin (EN*) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids the chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip-flops are clocked on the falling edge of the input clock; therefore, all associated specification limits are referenced to the negative edge of the clock input.

Functional Block Diagram



Features

- Extended Supply Voltage Range: (VEE = –5.5V to –3.0V, VCC = 0V) or (VCC = + 3.0V to +5.5V, VEE=0V)
- High Bandwidth Output Transition
- Max. 50 ps Output-to-Output Skew (Typ. 30 ps)
- V_{BB} Output
- Synchronous Enable/Disable
- Multiplexed Clock Input
- Internal 75 KΩ Input Pulldown Resistors
- New Differential Input Common Mode Range
- Fully Compatible with MC100EL14 and MC100LVEL14
- ESD Protection of >4000 V
- Industrial Temperature Range: –40°C to +85°C
- Available in 20 Lead SOIC (150 mils) Package

Pin Descriptions

Pin	Function
CLK, CLK*	Differential Clock Inputs
SCLK	Scan Clock Input
EN*	Sync Enable
SEL	Clock Select Input
V_{BB}	Reference Output Voltage
Q0-Q4, Q0*-Q4*	Differential Clock Outputs

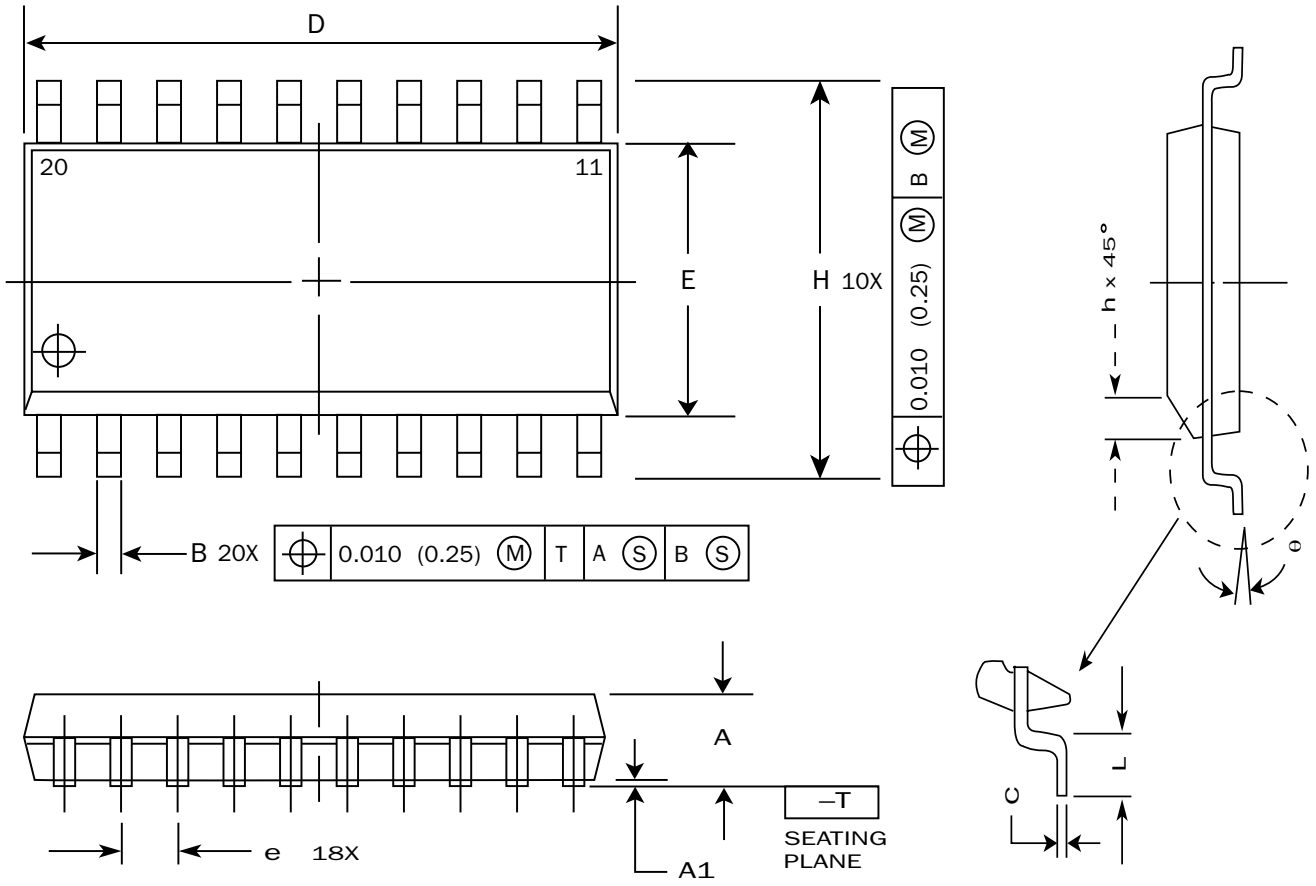
Function Table

CLK	SCLK	SEL	EN*	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

* On next negative transition of CLK or SCLK

Package Information

20 Pin SOIC Package



DIM	Millimeters	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

NOTES:
1. Dimensions and tolerances per ASME Y14.5M, 1994.
2. Controlling dimension: millimeters.
3. Dimensions D and E do not include mold protrusion.
4. Maximum mold protrusion 0.15 per side.
5. Dimension B does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.13 total in excess of B dimension at maximum material condition.

DC Characteristics

SK10/100EL14W DC Electrical Characteristics (Notes 1, 2, 7)

(V_{CC} – V_{EE} = +3.0V to +5.5V ; V_{OUT} loaded 50 Ω to V_{CC} – 2.0V)

Symbol	Characteristic	TA = -40°C			TA = 0°C			TA = + 25°C			TA = +85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply current 10EL 100EL	 22 22	 28 28	 38 38	 23 23	 30 30	 39 40	 24 24	 30 31	 40 41	 25 27	 32 34	 42 46	 mA mA
V_{BB}	Output Reference Voltage[3] 10EL 100EL	 - 1.43 - 1.38	 	 - 1.30 - 1.26	 - 1.38 - 1.38	 	 - 1.27 - 1.26	 - 1.35 - 1.38	 	 - 1.25 - 1.26	 -1.31 -1.38	 	 -1.19 -1.26	 V V
I_{IN}	Input Current (Diff) (SE)	- 150		150 150	- 150		150 150	- 150		150 150	- 150		150 150	µA µA

AC Characteristics

SK10/100EL14W AC Electrical Characteristics

(V_{CC} – V_{EE} = +3.0V to +5.5V ; V_{OUT} loaded 50 Ω to V_{CC} – 2.0V)

Symbol	Characteristic	TA = -40°C			TA = 0°C			TA = + 25°C			TA = +85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation Delay CLK to Q (Diff) CLK to Q (SE) SCLK to Q	 420 450 470	 565 550 555	 710 650 640	 480 475 490	 590 570 565	 700 665 640	 500 490 500	 610 585 580	 720 680 660	 560 530 550	 670 630 625	 780 730 700	 Ps Ps Ps
t_{skew}	Part-to-Part Skew Within Device Skew[4]			200 50			200 50			200 50			200 50	ps ps
t_S	Setup Time EN*	0			0			0			0			ps
t_H	Hold Time EN*	0			0			0			0			ps
V_{PP}	Minimum Input Swing CLK[5]	150		1000	150		1000	150		1000	150		1000	mV
V_{CMR}	Common Mode Range[6] VPP < 500 mV VPP > 500 mV	 VEE+1.3 VEE+1.5	 	 VCC-0.4 VCC-0.4	 VEE+1.3 VEE+1.5	 	 VCC-0.4 VCC-0.4	 VEE+1.3 VEE+1.5	 	 VCC-0.4 VCC-0.4	 VEE+1.3 VEE+1.5	 	 VCC-0.4 VCC-0.4	 V V
t_r , t_f	Output Rise/Fall Times (20% to 80%) Qn, Qn*	190	270	350	190	270	350	200	275	350	230	325	375	ps

Application Notes

AN1002 - Interfacing Between ECL / LVECL / PECL / LVPECL - to - TTL / LVTTL / CMOS / LVCMOS
AN1003 - Termination Techniques for ECL / LVECL / PECL / LVPECL Devices
AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL
AN1005 - Using ECL / LVECL Devices as PECL / LVPECL
AN1006 - Designing with 10K and 100K ECL / PECL Devices

AC Characteristics *(continued)*

Notes:

1. 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to VCC –2.0V.
2. 100K circuits are designed to meet the DC specification shown in the table where transverse airflow greater than 500 lfpm is maintained.
3. Voltages are referenced to VCC = 0V.
4. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
5. Minimum input swing for which AC parameters guaranteed.
6. CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between VPP(min) and 1V. The lower end of the CMR range varies 1:1 with VEE and is equal to VEE + 1.3V for VPP < 500 mV, and VEE + 1.5 for VPP > 500 mV.
7. For standard ECL DC specifications, refer to the ECL Logic Family Standard DC Specifications Data Sheet.
8. For part ordering descriptions, see HPP Part Ordering Information Data Sheet.

Ordering Information

Ordering Code	Package ID
SK10EL14WD	20-SOIC
SK10EL14WDT	20-SOIC
SK100EL14WD	20-SOIC
SK100EL14WDT	20-SOIC
SK10EL14WU	Die
SK100EL14WU	Die

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