

TYPES SN54LS113A, SN54S113, SN74LS113A, SN74S113 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

REVISED DECEMBER 1983

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs.
- Dependable Texas Instruments Quality and Reliability

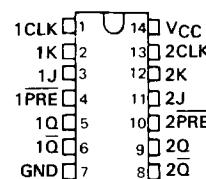
description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset input sets the outputs regardless of the levels of the other inputs. When preset (PRE) is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54LS113A and SN54S113 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS113A and SN74S112 are characterized for operation from 0°C to 70°C .

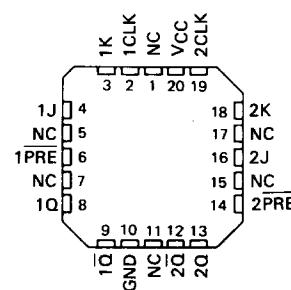
**SN54LS113A, SN54S113 ... J OR W PACKAGE
SN74LS113A, SN74S113 ... D, J OR N PACKAGE**

(TOP VIEW)



**SN54LS113A, SN54S113 ... FK PACKAGE
SN74LS113A, SN74S113 ... FN PACKAGE**

(TOP VIEW)



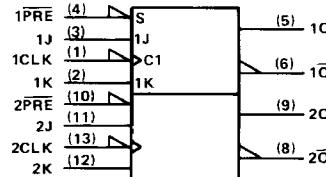
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NC - No internal connection

FUNCTION TABLE (each flip-flop)

INPUTS				OUTPUTS	
PRE	CLK	J	K	Q	\bar{Q}
L	X	X	X	H	L
H	↓	L	L	Q_0	\bar{Q}_0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	\bar{Q}_0

logic symbol



Pin numbers shown on logic notation are for D, J or N packages.

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PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

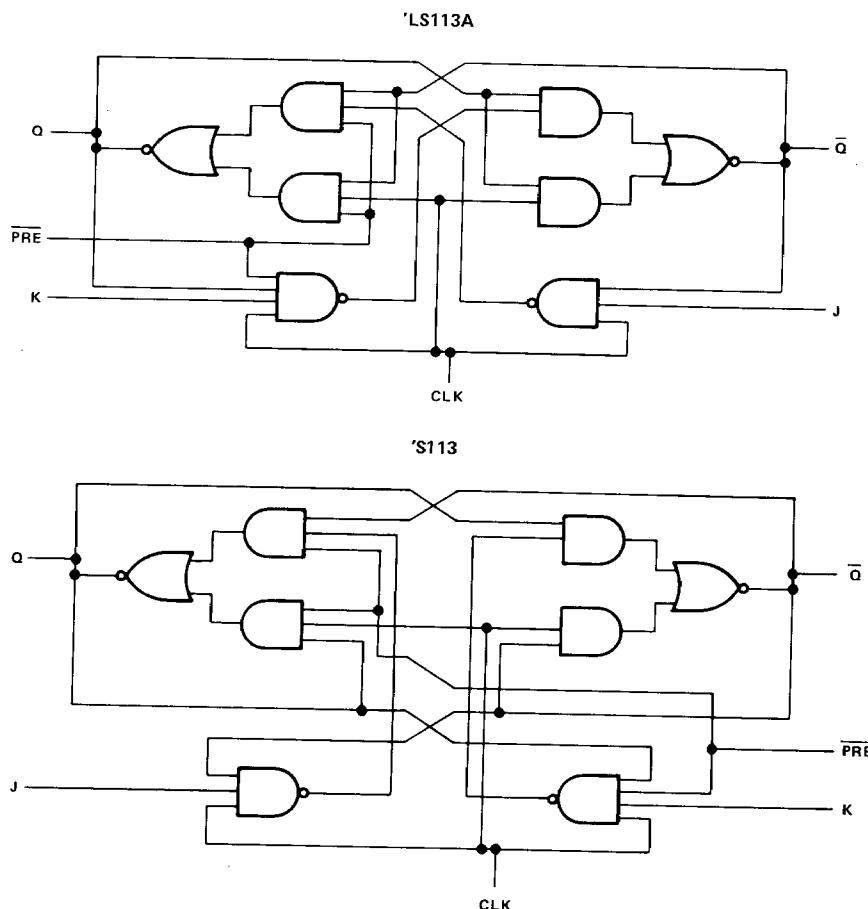
**TEXAS
INSTRUMENTS**

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**TYPES SN54LS113A, SN54S113, SN74LS113A, SN74S113
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET**

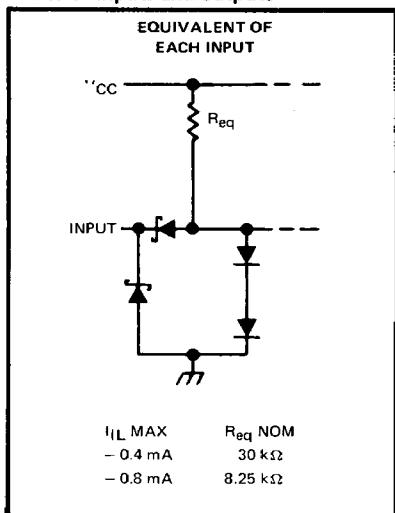
logic diagrams

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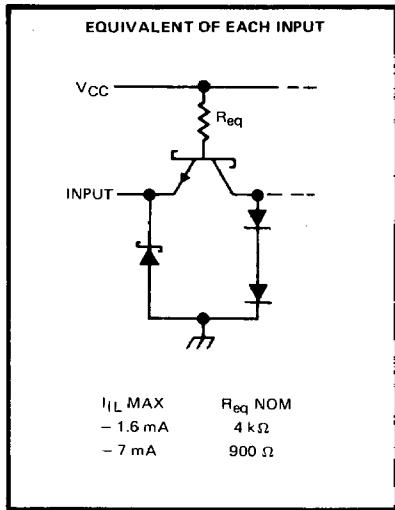
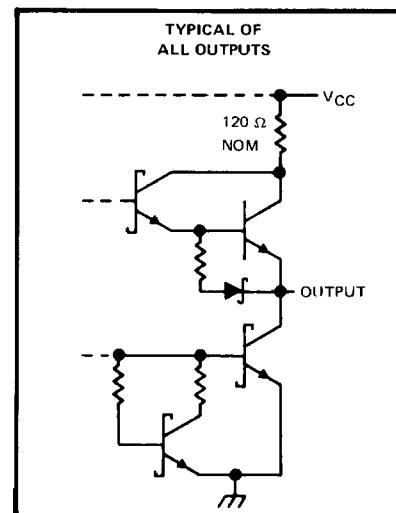


**TYPES SN54LS113A, SN54S113, SN74LS113A, SN74S113
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET**

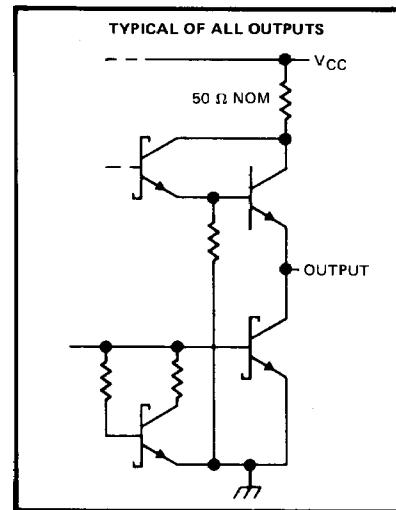
schematics of inputs and outputs



'LS113A'



'S113'



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage: 'LS113A'	7 V
'S113'	5.5 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54LS113A, SN74LS113A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

recommended operating conditions

		SN54LS113A			SN74LS113A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			4			8	mA
f _{clock}	Clock frequency	0	30	0	0	30	MHz	
t _w	Pulse duration	CLK high	20		20			ns
		PRE or CLR low	25		25			
t _{su}	Setup time before CLK ↓	data high or low	20		20			ns
		PRE inactive	20		20			
t _h	Hold time-data after CLK ↓		0		0	20		ns
T _A	Operating free-air temperature	-55	125	0	0	70	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]		SN54LS113A			SN74LS113A			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{JK}	V _{CC} = MIN,	I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN,	V _{IH} = 2 V,	V _{IL} = MAX,	2.5	3.4	2.7	3.4		V
V _{OL}	V _{CC} = MIN,	V _{IL} = MAX,	V _{IH} = 2 V,		0.25	0.4	0.25	0.4	V
	V _{CC} = MIN,	V _{IL} = MAX,	V _{IH} = 2 V,				0.35	0.5	
II	J or K				0.1		0.1		mA
	PRE	V _{CC} = MAX,	V _I = 7 V		0.3		0.3		
	CLK				0.4		0.4		
III	J or K				20		20		μA
	PRE	V _{CC} = MAX,	V _I = 2.7 V		60		60		
	CLK				80		80		
III	J or K				-0.4		-0.4		mA
	PRE or CLK	V _{CC} = MAX,	V _I = 0.4 V		-0.8		-0.8		
	I _{OS} [§]	V _{CC} = MAX,	see Note 4	-20	-100	-20	-100	-100	mA
ICC		V _{CC} = MAX,	see Note 2		4	6	4	6	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS			MIN	TYP	MAX	UNIT
f _{max}			R _L = 2 kΩ, C _L = 15 pF			30	45		MHz
t _{PLH}	PRE or CLK	Q or \bar{Q}				15	20		ns
t _{PHL}						15	20		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54S113, SN74S113
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

recommended operating conditions

		SN54S113			SN74S113			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		2			V
V_{IL}	Low-level input voltage			0.8		0.8		V
I_{OH}	High-level output current			-1		-1		mA
I_{OL}	Low-level output current			20		20		mA
t_w	CLK high	6			6			ns
	CLK low	6.5			6.5			
	PRE low	8			8			
t_{su}	Setup time before CLK I data high or low	3			3			ns
t_h	Hold time-data after CLK I	0			0			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]		SN54S113			SN74S113			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{IK}	$V_{CC} = \text{MIN}$,	$I_I = -18 \text{ mA}$				-1.2		-1.2	V	
V_{OH}	$V_{CC} = \text{MIN}$,	$V_{IH} = 2 \text{ V}$, $I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V	
V_{OL}	$V_{CC} = \text{MIN}$,	$V_{IH} = 2 \text{ V}$, $I_{OL} = 20 \text{ mA}$			0.5			0.5	V	
I_I	$V_{CC} = \text{MAX}$,	$V_I = 5.5 \text{ V}$			1			1	mA	
I_{IH}	J or K	$V_{CC} = \text{MAX}$,	$V_I = 2.7 \text{ V}$		50		50		μA	
	PRE or CLK				100		100			
I_{IL}	J or K	$V_{CC} = \text{MAX}$,	$V_I = 0.5 \text{ V}$		-1.6		-1.6		mA	
	PRE				-7		-7			
	CLK				-4		-4			
I_{OS} [§]	$V_{CC} = \text{MAX}$			-40	-100	-40	-100		mA	
I_{CC}	$V_{CC} = \text{MAX}$,	see Note 2			15	25		15	25	mA

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[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS			MIN	TYP	MAX	UNIT
f_{max}			$R_L = 280 \Omega$, $C_L = 15 \text{ pF}$			80	125		MHz
t_{PLH}	PRE	Q or \bar{Q}				4	7		ns
t_{PHL}	PRE (CLK high)	\bar{Q} or Q				5	7		
	PRE (CLK low)	\bar{Q} or Q				5	7		
t_{PLH}	CLK	Q or \bar{Q}				4	7		ns
t_{PHL}						5	7		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.