MICRON TECHNOLOGY, INC.

8Mb SYNCBURST™ SRAM

MT58L512L18D, MT58L256L32D, MT58L256L36D; MT58L512V18D, MT58L256V32D, MT58L256V36D

3.3V Supply, 3.3V or 2.5V I/O, Pipelined, Double-Cycle Deselect

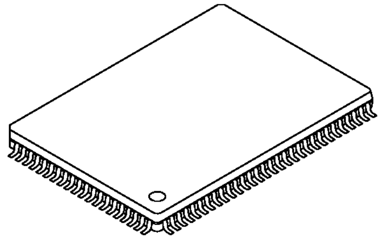
FEATURES

- Fast access times: 3.5ns, 3.8ns, 4.2ns, 4.5ns and 6ns
- Fast OE# access times: 3.5ns, 3.8ns, 4.2ns, 4.5ns and 5ns
- Single +3.3V +0.3V/-0.165V power supply (V_{DD})
- Separate +3.3V or +2.5V isolated output buffer supply ($V_{DD}Q$)
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- 119-bump BGA package
- Low capacitive bus loading
- x18, x32 and x36 versions available

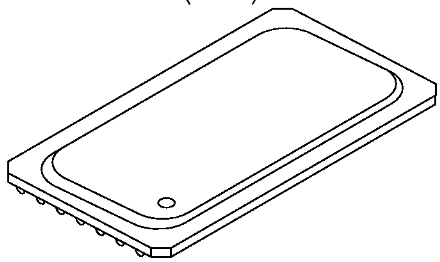
OPTIONS	MARKING
• Clock Cycle Timing	
5ns/200 MHz	-5
6ns/166 MHz	-6
6.6ns/150 MHz	-6.6
7.5ns/133 MHz	-7.5
10ns/100 MHz	-10
• Configurations	
3.3V I/O	
512K x 18	MT58L512L18D
256K x 32	MT58L256L32D
256K x 36	MT58L256L36D
2.5V I/O	
512K x 18	MT58L512V18D
256K x 32	MT58L256V32D
256K x 36	MT58L256V36D
• Packages	
100-pin TQFP	T
100-pin TQFP	Q
119-bump, 14mm x 22mm BGA	B

- Part Number Example: MT58L512V18DT-7.5

100-Pin TQFP*
(SA-1)



119-Bump BGA
(SB-1)



*JEDEC-standard MS-026 BHA (LQFP).

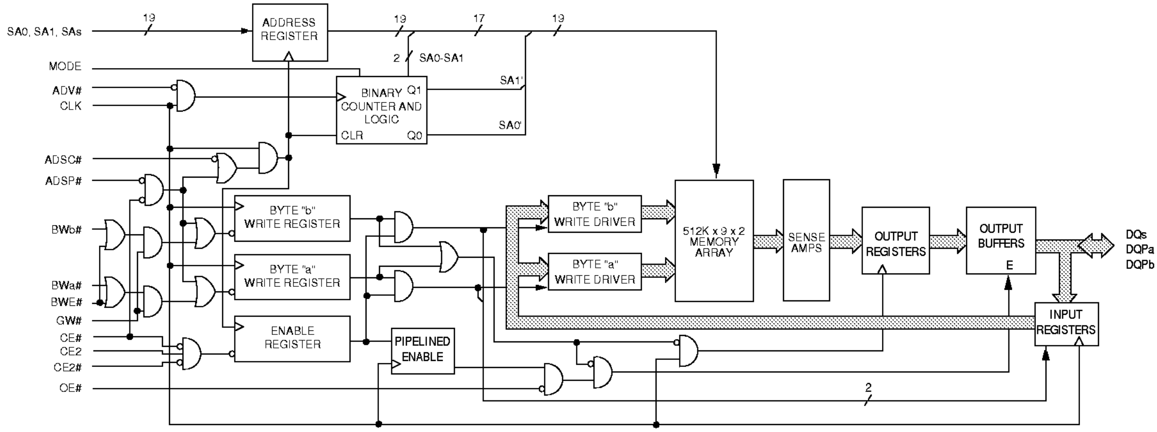
GENERAL DESCRIPTION

The Micron® SyncBurst™ SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

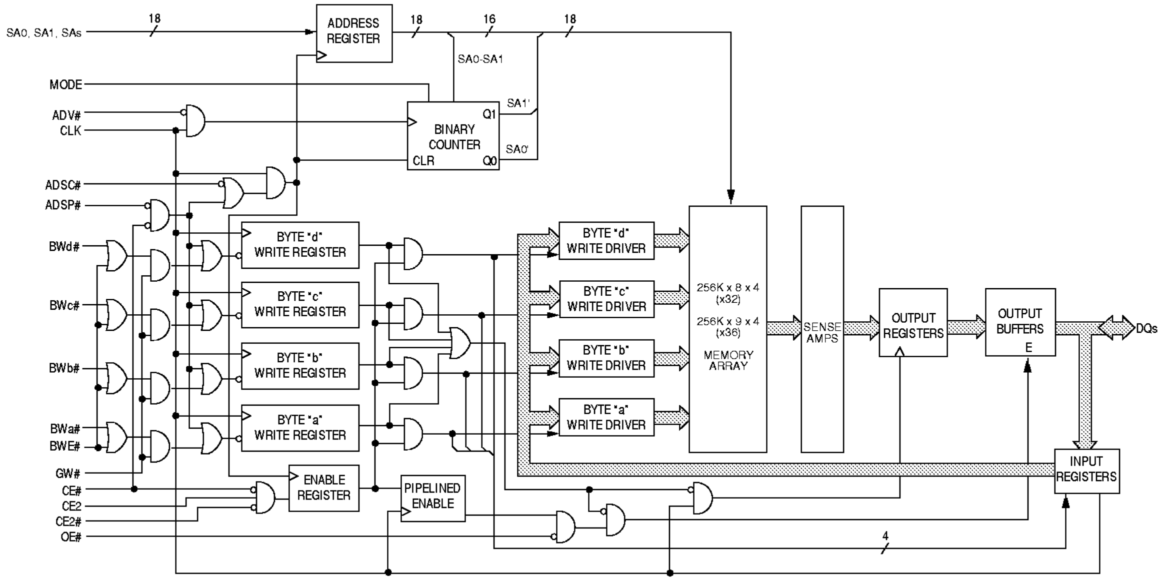
Micron's 8Mb SyncBurst SRAMs integrate a 512K x 18, 256K x 32, or 256K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single-clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#) and global write (GW#). Note that CE2# is not available on the T Version.

Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode input (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is

FUNCTIONAL BLOCK DIAGRAM
512K x 18



FUNCTIONAL BLOCK DIAGRAM
256K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

GENERAL DESCRIPTION (continued)

also asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), as controlled by the write control inputs.

Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) inputs. Subsequent burst addresses can be internally generated as controlled by the burst advance input (ADV#).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQPb. During WRITE cycles on the x32 and x36 devices, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQPb; BWc# controls DQc's and DQPc; BWd# controls DQd's and DQPd. GW# LOW causes all bytes to be written. Parity bits are only available on the x18 and x36 versions.

This device incorporates an additional pipelined enable register which delays turning off the output buffer an additional cycle when a deselect is executed. This feature allows depth expansion without penalizing system performance.

Micron's 8Mb SyncBurst SRAMs operate from a +3.3V VDD power supply, and all inputs and outputs are TTL-compatible. Users can choose either a 3.3V or 2.5V I/O version. The device is ideally suited for Pentium® and PowerPC™ pipelined systems and systems that benefit from a very wide, high-speed data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64- and 72-bit-wide applications.

Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest data sheet revisions.

TQFP Pinouts

At the time of the writing of this data sheet, there are two pinouts in the industry. Micron will support both pinouts for this part.

TQFP PIN ASSIGNMENT TABLE

PIN #	x18	x32/x36
1	NC	NC/DQPc*
2	NC	DQc
3	NC	DQc
4	VDDQ	
5	Vss	
6	NC	DQc
7	NC	DQc
8	DQb	DQc
9	DQb	DQc
10	Vss	
11	VDDQ	
12	DQb	DQc
13	DQb	DQc
14	VDD	
15	VDD	
16	NC	
17	Vss	
18	DQb	DQd
19	DQb	DQd
20	VDDQ	
21	Vss	
22	DQb	DQd
23	DQb	DQd
24	DQPb	DQd
25	NC	DQd

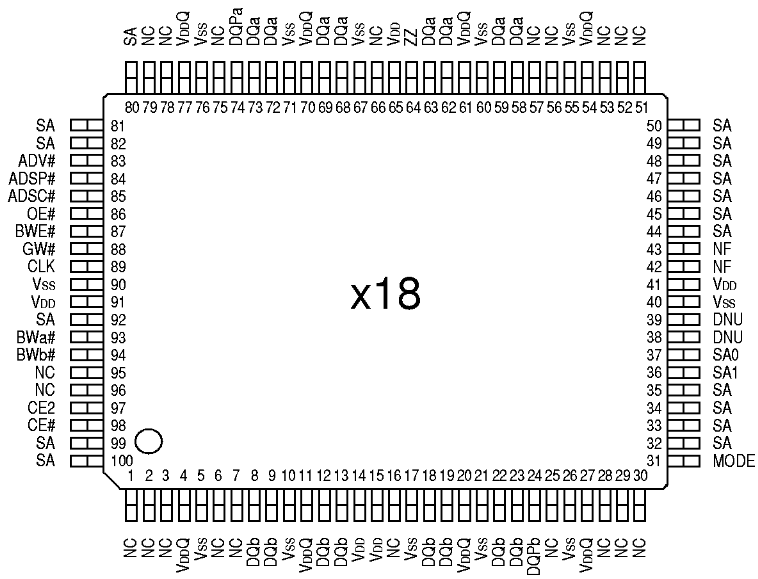
PIN #	x18	x32/x36
26	Vss	
27	VDDQ	
28	NC	DQd
29	NC	DQd
30	NC	NC/DQPd*
31	MODE	
32	SA	
33	SA	
34	SA	
35	SA	
36	SA1	
37	SA0	
38	DNU	
39	DNU	
40	Vss	
41	VDD	
42	NF	
43	NF (T Version) SA (Q Version)	
44	SA	
45	SA	
46	SA	
47	SA	
48	SA	
49	SA	
50	SA	

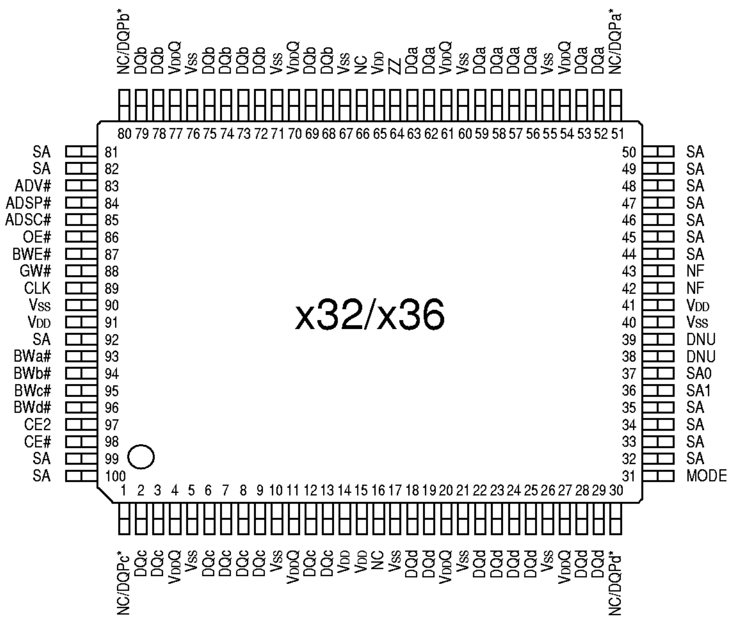
PIN #	x18	x32/x36
51	NC	NC/DQPa*
52	NC	DQa
53	NC	DQa
54	VDDQ	
55	Vss	
56	NC	DQa
57	NC	DQa
58	DQa	
59	DQa	
60	Vss	
61	VDDQ	
62	DQa	
63	DQa	
64	ZZ	
65	VDD	
66	NC	
67	Vss	
68	DQa	DQb
69	DQa	DQb
70	VDDQ	
71	Vss	
72	DQa	DQb
73	DQa	DQb
74	DQPa	DQb
75	NC	DQb

PIN #	x18	x32/x36
76	Vss	
77	VDDQ	
78	NC	DQb
79	NC	DQb
80	SA	NC/DQPb*
81	SA	
82	SA	
83	ADV#	
84	ADSP#	
85	ADSC#	
86	OE#	
87	BWE#	
88	GW#	
89	CLK	
90	Vss	
91	VDD	
92	SA (T Version) CE2# (Q Version)	
93	BWa#	
94	BWb#	
95	NC	BWc#
96	NC	BWd#
97	CE2	
98	CE#	
99	SA	
100	SA	

*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

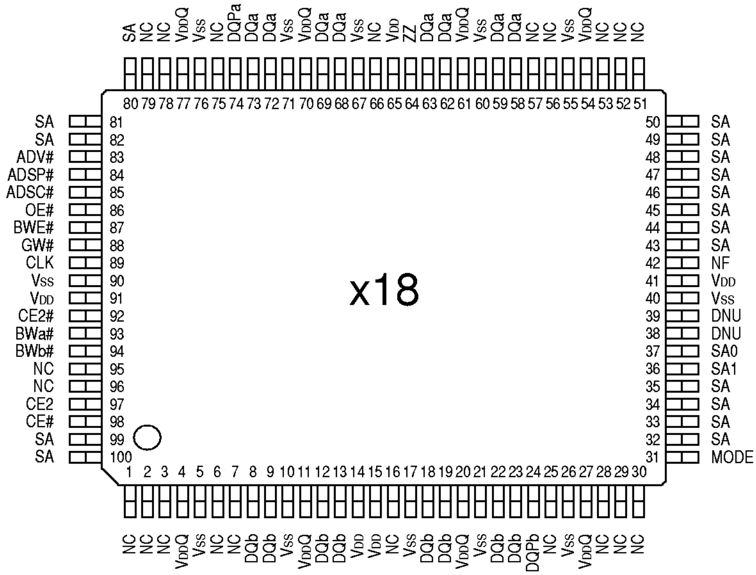
PIN ASSIGNMENT (Top View)
100-Pin TQFP, T Version
(SA-1)

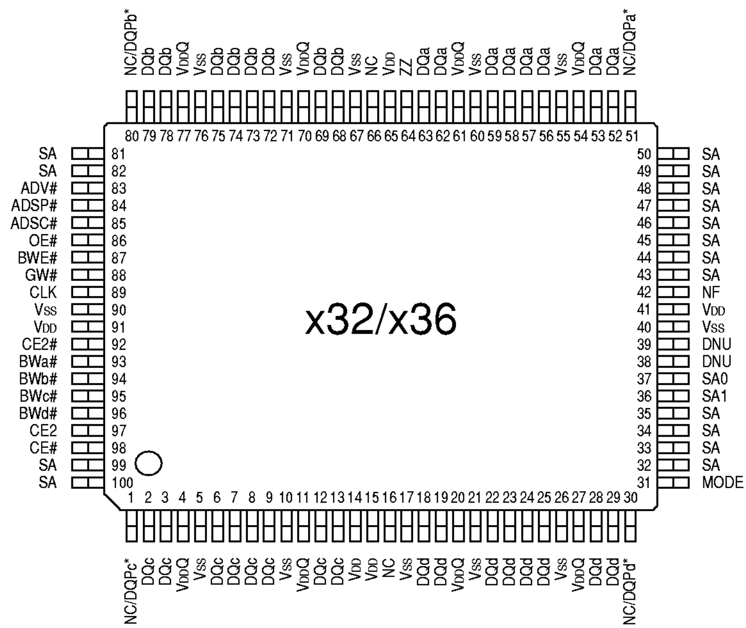




*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

PIN ASSIGNMENT (Top View)
100-Pin TQFP, Q Version
(SA-1)





*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

PIN ASSIGNMENT (Top View)
119-Bump BGA

x18

	1	2	3	4	5	6	7
A	VDDQ	SA	SA	ADSP#	SA	SA	VDDQ
B	NC	CE2	SA	ADSC#	SA	SA	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	DQb	NC	VSS	NC	VSS	DQPa	NC
E	NC	DQb	VSS	CE#	VSS	NC	DQa
F	VDDQ	NC	VSS	OE#	VSS	DQa	VDDQ
G	NC	DQb	BWb#	ADV#	VSS	NC	DQa
H	DQb	NC	VSS	GW#	VSS	DQa	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQb	VSS	CLK	VSS	NC	DQa
L	DQb	NC	VSS	NC	BWa#	DQa	NC
M	VDDQ	DQb	VSS	BWE#	VSS	NC	VDDQ
N	DQb	NC	VSS	SA1	VSS	DQa	NC
P	NC	DQPb	VSS	SA0	VSS	NC	DQa
R	NC	SA	MODE	VDD	VDD	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	VDDQ	DNU	DNU	DNU	DNU	NC	VDDQ

TOP VIEW

x32/x36

	1	2	3	4	5	6	7
A	VDDQ	SA	SA	ADSP#	SA	SA	VDDQ
B	NC	CE2	SA	ADSC#	SA	SA	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	DQc	NC/DQPc*	VSS	NC	VSS	NC/DQPb*	DQb
E	DQc	DQc	VSS	CE#	VSS	DQb	DQb
F	VDDQ	DQc	VSS	OE#	VSS	DQb	VDDQ
G	DQc	DQc	BWc#	ADV#	BWb#	DQb	DQb
H	DQc	DQc	VSS	GW#	VSS	DQb	DQb
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQd	DQd	VSS	CLK	VSS	DQa	DQa
L	DQd	DQd	BWd#	NC	BWa#	DQa	DQa
M	VDDQ	DQd	VSS	BWE#	VSS	DQa	VDDQ
N	DQd	DQd	VSS	SA1	VSS	DQa	DQa
P	DQd	NC/DQPd*	VSS	SA0	VSS	NC/DQPa*	DQa
R	NC	SA	MODE	VDD	VDD	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	VDDQ	DNU	DNU	DNU	DNU	NC	VDDQ

TOP VIEW

*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

TQFP PIN DESCRIPTIONS

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
37 36 32-35, 44-50, 80-82, 99, 100 92 (T Version) 43 (Q Version)	37 36 32-35, 44-50, 81, 82, 99, 100 92 (T Version) 43 (Q Version)	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. Two different pinouts are available for the TQFP package.
93 94 – –	93 94 95 96	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb. For the x32 and x36 versions, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb; BWc# controls DQc pins and DQPc; BWd# controls DQd pins and DQPd. Parity is only available on the x18 and x36 versions.
87	87	BWE#	Input	Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK.
88	88	GW#	Input	Global Write: This active LOW input allows a full 18-, 32- or 36-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CLK.
89	89	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	98	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP#. CE# is sampled only when a new external address is loaded.
92 (Q Version)	92 (Q Version)	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded. CE2# is only available on the Q Version.
64	64	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.
97	97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
86	86	OE#	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers.
83	83	ADV#	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV# must be HIGH at the rising edge of the first clock after an ADSP# cycle is initiated.

TQFP PIN DESCRIPTIONS (continued)

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
84	84	ADSP#	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC#, but dependent upon CE#, CE2 and CE2#. ADSP# is ignored if CE# is HIGH. Power-down state is entered if CE2 is LOW or CE2# is HIGH.
85	85	ADSC#	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE# is LOW. ADSC# is also used to place the chip into power-down state when CE# is HIGH.
31	31	MODE	Input	Mode: This input selects the burst sequence. A LOW on this pin selects "linear burst." NC or HIGH on this pin selects "interleaved burst." Do not alter input state while device is operating.
(a) 58, 59, 62, 63, 68, 69, 72, 73 (b) 8, 9, 12, 13, 18, 19, 22, 23	(a) 52, 53, 56-59, 62, 63 (b) 68, 69 72-75, 78, 79 (c) 2, 3, 6-9, 12, 13 (d) 18, 19, 22-25, 28, 29	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: For the x18 version, Byte "a" is DQa pins; Byte "b" is DQb pins. For the x32 and x36 versions, Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. Input data must meet setup and hold times around the rising edge of CLK.
74 24 – –	51 80 1 30	NC/DQPa NC/DQPb NC/DQPc NC/DQPd	NC/ I/O	No Connect/Parity Data I/Os: On the x32 version, these pins are No Connect (NC). On the x18 version, Byte "a" Parity is DQPa; Byte "b" Parity is DQPb. On the x36 version, Byte "a" Parity is DQPa; Byte "b" Parity is DQPb; Byte "c" Parity is DQPc; Byte "d" Parity is DQPd.
14, 15, 41, 65, 91	14, 15, 41, 65, 91	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
4, 11, 20, 27, 54, 61, 70, 77	4, 11, 20, 27, 54, 61, 70, 77	$V_{DD}Q$	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground: GND.
38, 39	38, 39	DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation.
1-3, 6, 7, 16, 25, 28-30, 51-53, 56, 57, 66, 75, 78, 79, 95, 96	16, 66	NC	–	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation.
42 43 (T Version)	42 43 (T Version)	NF	–	No Function: These pins are internally connected to the die and have the capacitance of an input pin. It is allowable to leave these pins unconnected or driven by signals. On the Q Version, pin 42 is reserved as an address upgrade pin for the 16Mb SyncBurst SRAM.

MICRON TECHNOLOGY, INC.

BGA BUMP DESCRIPTIONS

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
4P 4N 2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 2T, 3T, 5T, 6B, 6T	4P 4N 2A, 2C, 2R, 3A, 3B, 3C, 3T, 4T, 5A, 5B, 5C, 5T, 6A, 6B, 6C, 6R	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
5L 3G – –	5L 5G 3G 3L	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQPb. For the x32 and x36 versions, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQPb; BWc# controls DQc's and DQPc; BWd# controls DQd's and DQPd. Parity is only available on the x18 and x36 versions.
4M	4M	BWE#	Input	Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK.
4H	4H	GW#	Input	Global Write: This active LOW input allows a full 18-, 32- or 36-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CLK.
4K	4K	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
4E	4E	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP#. CE# is sampled only when a new external address is loaded.
7T	7T	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When active, all other inputs are ignored.
2B	2B	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
4F	4F	OE#	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers.
4G	4G	ADV#	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on ADV# effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV# must be HIGH at the rising edge of the first clock after an ADSP# cycle is initiated.

BGA BUMP DESCRIPTIONS (continued)

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
4A	4A	ADSP#	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC#, but dependent upon CE#, CE2 and CE2#. ADSP# is ignored if CE# is HIGH. Power-down state is entered if CE2 is LOW or CE2# is HIGH.
4B	4B	ADSC#	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE# is LOW. ADSC# is also used to place the chip into power-down state when CE# is HIGH.
3R	3R	MODE	Input	Mode: This input selects the burst sequence. A LOW on MODE selects “linear burst.” NC or HIGH on MODE selects “interleaved burst.” Do not alter input state while device is operating.
(a) 6F, 6H, 6L, 6N, 7E, 7G, 7K, 7P (b) 1D, 1H, 1L, 1N, 2E, 2G, 2K, 2M	(a) 6K, 6L, 6M, 6N, 7K, 7L, 7N, 7P (b) 6E, 6F, 6G, 6H, 7D, 7E, 7G, 7H (c) 1D, 1E, 1G, 1H, 2E, 2F, 2G, 2H (d) 1K, 1L, 1N, 1P, 2K, 2L, 2M, 2N	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: For the x18 version, Byte “a” is DQa pins; Byte “b” is DQb pins. For the x32 and x36 versions, Byte “a” is DQa pins; Byte “b” is DQb pins; Byte “c” is DQc pins; Byte “d” is DQd pins. Input data must meet setup and hold times around the rising edge of CLK.
6D 2P – –	6P 6D 2D 2P	NC/DQPa NC/DQPb NC/DQPc NC/DQPd	NC/ I/O	No Connect/Parity Data I/Os: On the x32 version, these are No Connect (NC). On the x18 version, Byte “a” Parity is DQPa; Byte “b” Parity is DQPb. On the x36 version, Byte “a” Parity is DQPa; Byte “b” Parity is DQPb; Byte “c” Parity is DQPc; Byte “d” Parity is DQPd.
2J, 4C, 4J, 4R, 5R, 6J	2J, 4C, 4J, 4R, 5R, 6J	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
1A, 1F, 1J, 1M, 1U, 7A, 7F, 7J, 7M, 7U	1A, 1F, 1J, 1M, 1U, 7A, 7F, 7J, 7M, 7U	$V_{DD}Q$	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
3D, 3E, 3F, 3H, 3K, 3L, 3M, 3N, 3P, 5D, 5E, 5F, 5G, 5H, 5K, 5M, 5N, 5P	3D, 3E, 3F, 3H, 3K, 3M, 3N, 3P, 5D, 5E, 5F, 5H, 5K, 5M, 5N, 5P	V_{SS}	Supply	Ground: GND.

BGA BUMP DESCRIPTIONS (continued)

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
2U, 3U, 4U, 5U	2U, 3U, 4U, 5U	DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation.
1B, 1C, 1E, 1G, 1K, 1P, 1R, 1T, 2D, 2F, 2H, 2L, 2N, 3J, 4D, 4L, 4T, 5J, 6E, 6G, 6K, 6M, 6P, 6U, 7B, 7C, 7D, 7H, 7L, 7N, 7R	1B, 1C, 1R, 1T, 2T, 3J, 4D, 4L, 5J, 6T, 6U, 7B, 7C, 7R	NC	–	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation.

INTERLEAVED BURST ADDRESS TABLE (MODE = NC OR HIGH)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = LOW)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PARTIAL TRUTH TABLE FOR WRITE COMMANDS (x18)

FUNCTION	GW#	BWE#	BWa#	BWb#
READ	H	H	X	X
READ	H	L	H	H
WRITE Byte "a"	H	L	L	H
WRITE Byte "b"	H	L	H	L
WRITE All Bytes	H	L	L	L
WRITE All Bytes	L	X	X	X

PARTIAL TRUTH TABLE FOR WRITE COMMANDS (x32/x36)

FUNCTION	GW#	BWE#	BWa#	BWb#	BWc#	BWd#
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE Byte "a"	H	L	L	H	H	H
WRITE All Bytes	H	L	L	L	L	L
WRITE All Bytes	L	X	X	X	X	X

NOTE: Using BWE# and BWa# through BWd#, any one or more bytes may be written.

TRUTH TABLE

OPERATION	ADDRESS USED	CE#	CE2#	CE2	ZZ	ADSP#	ADSC#	ADV#	WRITE#	OE#	CLK	DQ
Deselected Cycle, Power-Down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-Down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-Down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-Down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-Down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
SNOOZE MODE, Power-Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

NOTE:
1. X means “Don’t Care.” # means active LOW. H means logic HIGH. L means logic LOW.
2. For WRITE#, L means any one or more byte write enable signals (BWa#, BWb#, BWc# or BWd#) and BWE# are LOW or GW# is LOW. WRITE# = H for all BWx#, BWE#, GW# HIGH.
3. BWa# enables WRITEs to DQa’s and DQPa. BWb# enables WRITEs to DQb’s and DQPb. BWc# enables WRITEs to DQc’s and DQPc. BWd# enables WRITEs to DQd’s and DQPd. DQPa and DQPb are only available on the x18 and x36 versions. DQPc and DQPd are only available on the x36 version.
4. All inputs except OE# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, OE# must be HIGH before the input data setup time and held HIGH throughout the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. ADSP# LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE# LOW or GW# LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to V_{SS} .... -0.5V to +4.6V
Voltage on $V_{DD}Q$ Supply Relative to V_{SS} .... -0.5V to +4.6V
V_{IN} (DQx) .... -0.5V to $V_{DD}Q$ + 0.5V
V_{IN} (inputs) .... -0.5V to V_{DD} + 0.5V
Storage Temperature (plastic) .... -55°C to +150°C
Storage Temperature (BGA) .... -55°C to +125°C
Junction Temperature** .... +150°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See Micron Technical Note TN-05-14 for more information.

3.3V DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{DD}, $V_{DD}Q$ = +3.3V +0.3V/-0.165V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}	I_{LI}	-1.0	1.0	µA	3
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ V_{DD}	I_{LO}	-1.0	1.0	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4	–	V	1, 4
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}	–	0.4	V	1, 4
Supply Voltage		V_{DD}	3.135	3.6	V	1
Isolated Output Buffer Supply		$V_{DD}Q$	3.135	3.6	V	1, 5

NOTE:
1. All voltages referenced to V_{SS} (GND).
2. Overshoot: V_{IH} ≤ +4.6V for t ≤ $^tKC/2$ for I ≤ 20mA
   Undershoot: V_{IL} ≥ -0.7V for t ≤ $^tKC/2$ for I ≤ 20mA
   Power-up: V_{IH} ≤ +3.6V and V_{DD} ≤ 3.135V for t ≤ 200ms
3. MODE has an internal pull-up, and input leakage = ±10µA.
4. The load used for V_{OH}, V_{OL} testing is shown in Figure 2 for 3.3V I/O. AC load current is higher than the stated DC values. AC I/O curves are available upon request.
5. $V_{DD}Q$ should never exceed V_{DD}. V_{DD} and $V_{DD}Q$ can be connected together.

2.5V DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{DD} = +3.3V +0.3V/-0.165V; V_{DDQ} = +2.5V +0.4V/-0.125V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data bus (DQx)	V_{IHQ}	1.7	V_{DDQ} + 0.3	V	1, 2
	Inputs	V_{IH}	1.7	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}	IL_I	-1.0	1.0	µA	3
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ V_{DDQ} (DQx)	IL_O	-1.0	1.0	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	1.7	–	V	1
	I_{OH} = -1.0mA	V_{OH}	2.0	–	V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}	–	0.7	V	1
	I_{OL} = 1.0mA	V_{OL}	–	0.4	V	1
Supply Voltage		V_{DD}	3.135	3.6	V	1
Isolated Output Buffer Supply		V_{DDQ}	2.375	2.9	V	1

TQFP THERMAL RESISTANCE

DESCRIPTION	CONDITIONS		SYMBOL	TYP	UNITS	NOTES
Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EAI/JESD51.	1-layer	θ_{JA}	40	°C/W	4
		4-layer	θ_{JA}	22	°C/W	4
Thermal Resistance (Junction to Top of Case)			θ_{JC}	8	°C/W	4

BGA THERMAL RESISTANCE

DESCRIPTION	CONDITIONS		SYMBOL	TYP	UNITS	NOTES
Junction to Ambient (Airflow of 1m/s)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EAI/JESD51.	1-layer	θ_{JA}	40	°C/W	4
		4-layer	θ_{JA}	25	°C/W	4
Junction to Case (Top)			θ_{JC}	9	°C/W	4
Junction to Bumps (Bottom)			θ_{JB}	17	°C/W	4

NOTE:
1. All voltages referenced to V_{SS} (GND).
2. Overshoot: V_{IH} ≤ +4.6V for t ≤ $^tKC/2$ for I ≤ 20mA
   Undershoot: V_{IL} ≥ -0.7V for t ≤ $^tKC/2$ for I ≤ 20mA
   Power-up: V_{IH} ≤ +3.6V and V_{DD} ≤ 3.135V for t ≤ 200ms
3. MODE has an internal pull-up, and input leakage = ±10µA.
4. This parameter is sampled.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{DD}, $V_{DD}Q$ = +3.3V +0.3V/-0.165V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYM	TYP	MAX -5	MAX -6	MAX -6.6	MAX -7.5	MAX -10	UNITS	NOTES
Power Supply Current: Operating	Device selected; All inputs ≤ V_{IL} or ≥ V_{IH}; Cycle time ≥ ^{t}KC MIN; V_{DD} = MAX; Outputs open	I_{DD}	TBD	525	450	400	325	250	mA	1, 2, 3
Power Supply Current: Idle	Device selected; V_{DD} = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ V_{IH}; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^{t}KC MIN	I_{DD1}	TBD	125	110	100	90	85	mA	1, 2, 3
CMOS Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; All inputs static; CLK frequency = 0	I_{SB2}	TBD	10	10	10	10	10	mA	2, 3
TTL Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{IL} or ≥ V_{IH}; All inputs static; CLK frequency = 0	I_{SB3}	TBD	25	25	25	25	25	mA	2, 3
Clock Running	Device deselected; V_{DD} = MAX; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^{t}KC MIN	I_{SB4}	TBD	125	110	100	90	85	mA	2, 3

TQFP CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Control Input Capacitance	T_A = 25°C; f = 1 MHz; V_{DD} = 3.3V	C_I	3	4	pF	4
Input/Output Capacitance (DQ)		C_O	4	5	pF	4
Address Capacitance		C_A	3	3.5	pF	4
Clock Capacitance		C_{CK}	2.5	3	pF	4

BGA CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Address/Control Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	3	4	pF	4
Input/Output Capacitance (DQ)		C_O	4	5	pF	4
Address Capacitance		C_A	3	3.5	pF	4
Clock Capacitance		C_{CK}	2.5	3	pF	4

NOTE:
1. I_{DD} is specified with no output current and increases with faster cycle times. $I_{DD}Q$ increases with faster cycle times and greater output loading.
2. "Device deselected" means device is in power-down mode as defined in the truth table. "Device selected" means device is active (not in power-down mode).
3. Typical values are measured at 3.3V, 25°C and 10ns cycle time.
4. This parameter is sampled.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 1) (0°C ≤ T_A ≤ 70°C; V_{DD}, $V_{DD}Q$ = +3.3V +0.3V/-0.165V unless otherwise noted)

DESCRIPTION		-5		-6		-6.6		-7.5		-10			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock													
Clock cycle time	^{t}KC	5.0		6.0		6.6		7.5		10		ns	
Clock frequency	^{f}KF		200		166		150		133		100	MHz	
Clock HIGH time	^{t}KH	1.6		1.7		1.8		1.9		3.2		ns	
Clock LOW time	^{t}KL	1.6		1.7		1.8		1.9		3.2		ns	
Output Times													
Clock to output valid	^{t}KQ		3.1		3.5		3.8		4.0		5.0	ns	
Clock to output invalid	^{t}KQX	1.0		1.5		1.5		1.5		1.5		ns	2
Clock to output in Low-Z	^{t}KQLZ	0		0		0		0		1.5		ns	2, 3, 4, 5
Clock to output in High-Z	^{t}KQHZ		3.1		3.5		3.8		4.2		5.0	ns	2, 3, 4, 5
OE# to output valid	^{t}OEQ		3.1		3.5		3.8		4.2		5.0	ns	6
OE# to output in Low-Z	^{t}OELZ	0		0		0		0		0		ns	2, 3, 4, 5
OE# to output in High-Z	^{t}OEHZ		3.0		3.5		3.8		4.2		4.5	ns	2, 3, 4, 5
Setup Times													
Address	^{t}AS	1.5		1.5		1.5		1.5		2.0		ns	7, 8
Address status (ADSC#, ADSP#)	^{t}ADSS	1.5		1.5		1.5		1.5		2.0		ns	7, 8
Address advance (ADV#)	^{t}AAS	1.5		1.5		1.5		1.5		2.0		ns	7, 8
Write signals (BWa#-BWd#, BWE#, GW#)	^{t}WS	1.5		1.5		1.5		1.5		2.0		ns	7, 8
Data-in	^{t}DS	1.5		1.5		1.5		1.5		2.0		ns	7, 8
Chip enables (CE#, CE2#, CE2)	^{t}CES	1.5		1.5		1.5		1.5		2.0		ns	7, 8
Hold Times													
Address	^{t}AH	0.5		0.5		0.5		0.5		0.5		ns	7, 8
Address status (ADSC#, ADSP#)	^{t}ADSH	0.5		0.5		0.5		0.5		0.5		ns	7, 8
Address advance (ADV#)	^{t}AAH	0.5		0.5		0.5		0.5		0.5		ns	7, 8
Write signals (BWa#-BWd#, BWE#, GW#)	^{t}WH	0.5		0.5		0.5		0.5		0.5		ns	7, 8
Data-in	^{t}DH	0.5		0.5		0.5		0.5		0.5		ns	7, 8
Chip enables (CE#, CE2#, CE2)	^{t}CEH	0.5		0.5		0.5		0.5		0.5		ns	7, 8

NOTE:

1. Test conditions as specified with the output loading as shown in Figure 1 for 3.3V I/O and Figure 3 for 2.5V I/O unless otherwise noted.
2. This parameter is measured with output load as shown in Figure 2 for 3.3V I/O and Figure 4 for 2.5V I/O.
3. This parameter is sampled.
4. Transition is measured ±500mV from steady state voltage.
5. Refer to Technical Note TN-58-09, "Synchronous SRAM Bus Contention Design Considerations," for a more thorough discussion on these parameters.
6. OE# is a "Don't Care" when a byte write enable is sampled LOW.
7. A WRITE cycle is defined by at least one byte write enable LOW and ADSP# HIGH for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and ADSC# or ADV# LOW or ADSP# LOW for the required setup and hold times.
8. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either ADSP# or ADSC# is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when either ADSP# or ADSC# is LOW to remain enabled.

3.3V I/O AC TEST CONDITIONS

Input pulse levels	$V_{IH} = (V_{DD}/2.2) + 1.5V$
	$V_{IL} = (V_{DD}/2.2) - 1.5V$
Input rise and fall times	1ns
Input timing reference levels	$V_{DD}/2.2$
Output reference levels	$V_{DD}/2.2$
Output load	See Figures 1 and 2

2.5V I/O AC TEST CONDITIONS

Input pulse levels	V_{SS} to 2.5V
Input rise and fall times	1ns
Input timing reference levels	1.25V
Output reference levels	1.25V
Output load	See Figures 3 and 4

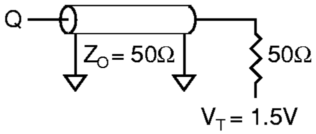


Figure 1
3.3V I/O OUTPUT LOAD EQUIVALENT

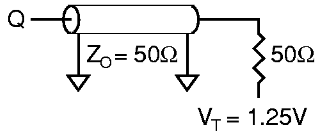


Figure 3
2.5V I/O OUTPUT LOAD EQUIVALENT

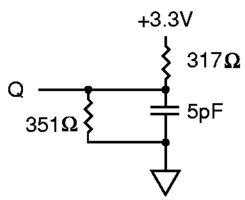


Figure 2
3.3V I/O OUTPUT LOAD EQUIVALENT

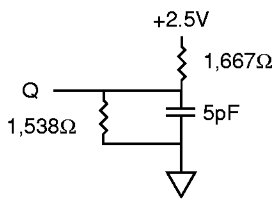


Figure 4
2.5V I/O OUTPUT LOAD EQUIVALENT

LOAD DERATING CURVES

Micron 512K x 18, 256K x 32, and 256K x 36 SyncBurst SRAM timing is dependent upon the capacitive loading on the outputs.

Consult the factory for copies of I/O current versus voltage curves.

SNOOZE MODE

SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to I_{SB2Z}. The duration of SNOOZE MODE is dictated by the length of time ZZ is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored.

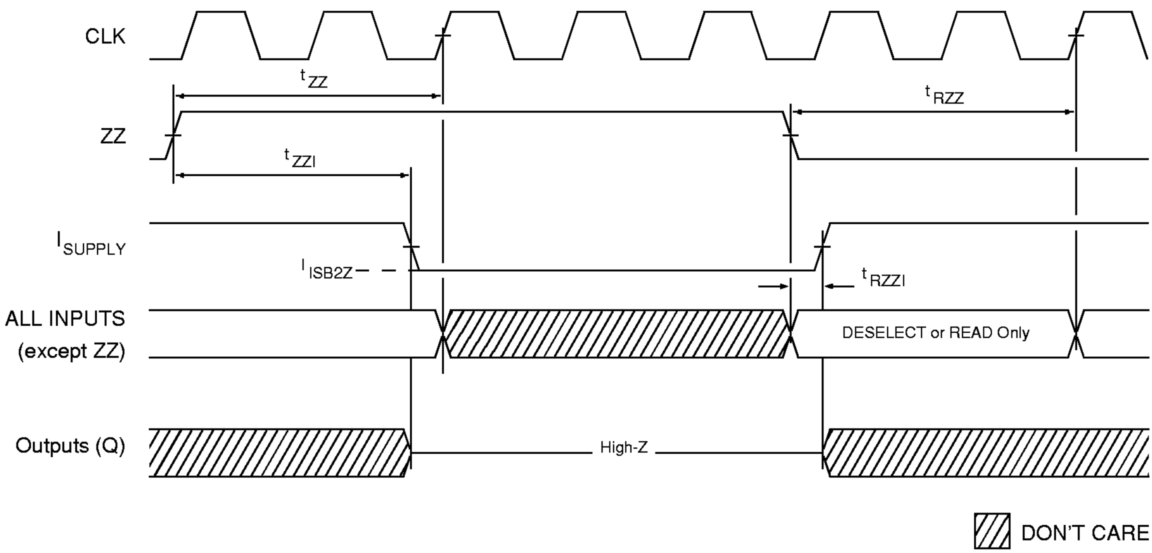
ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When ZZ becomes a logic HIGH, I_{SB2Z} is guaranteed after the setup time ^tZZ is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

SNOOZE MODE ELECTRICAL CHARACTERISTICS

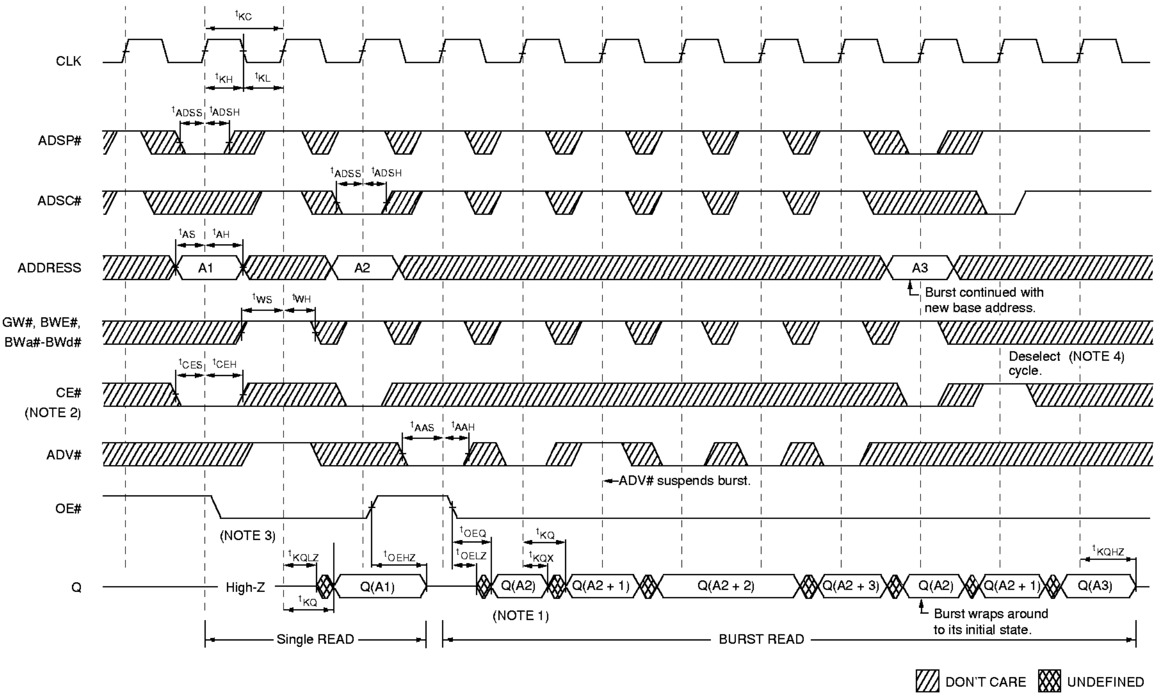
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	$ZZ \geq V_{IH}$	I_{SB2Z}		10	mA	
ZZ active to input ignored		^tZZ		$2(^tKC)$	ns	1
ZZ inactive to input sampled		^tRZZ	$2(^tKC)$		ns	1
ZZ active to snooze current		^tZZI		$2(^tKC)$	ns	1
ZZ inactive to exit snooze current		^tRZZI	0		ns	1

NOTE: 1. This parameter is sampled.

SNOOZE MODE WAVEFORM



READ TIMING [3]



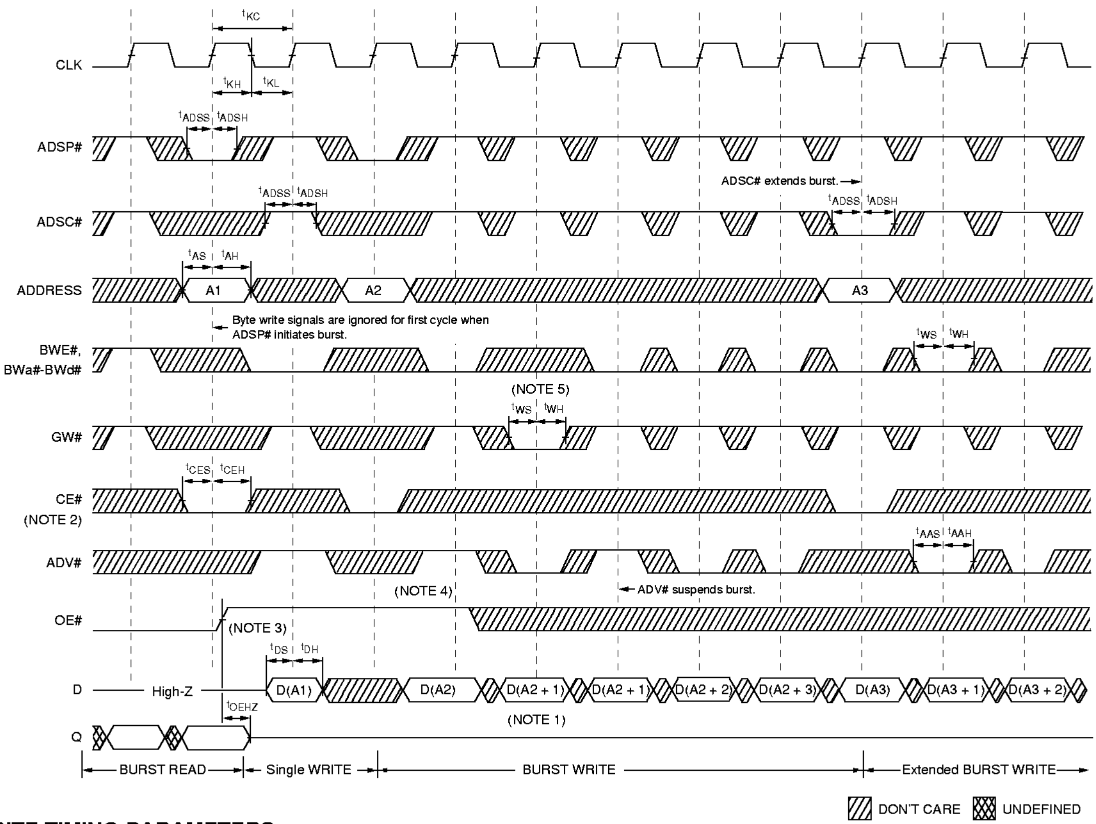
READ TIMING PARAMETERS

SYM	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-6.6 MIN	-6.6 MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
tKC	5.0		6.0		6.6		7.5		10		ns
tKF		200		166		150		133		100	MHz
tKH	1.6		1.7		1.8		1.9		3.2		ns
tKL	1.6		1.7		1.8		1.9		3.2		ns
tKQ		3.1		3.5		3.8		4.0		5.0	ns
tKQX	1.0		1.5		1.5		1.5		1.5		ns
tKQLZ	0		0		0		0		1.5		ns
tKQHZ		3.1		3.5		3.8		4.2		5.0	ns
tOEQ		3.1		3.5		3.8		4.2		5.0	ns
tOELZ	0		0		0		0		0		ns
tOEHZ		3.0		3.5		3.8		4.2		4.5	ns

SYM	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-6.6 MIN	-6.6 MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
tAS	1.5		1.5		1.5		1.5		2.0		ns
tADSS	1.5		1.5		1.5		1.5		2.0		ns
tAAS	1.5		1.5		1.5		1.5		2.0		ns
tWS	1.5		1.5		1.5		1.5		2.0		ns
tCES	1.5		1.5		1.5		1.5		2.0		ns
tAH	0.5		0.5		0.5		0.5		0.5		ns
tADSH	0.5		0.5		0.5		0.5		0.5		ns
tAAH	0.5		0.5		0.5		0.5		0.5		ns
tWH	0.5		0.5		0.5		0.5		0.5		ns
tCEH	0.5		0.5		0.5		0.5		0.5		ns

NOTE:
1. Q(A2) refers to output from address A2. Q(A2 + 1) refers to output from the next internal burst address following A2.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. OE# does not cause Q to be driven until after the following clock rising edge.
4. Outputs are disabled within two clock cycles after deselect.

WRITE TIMING



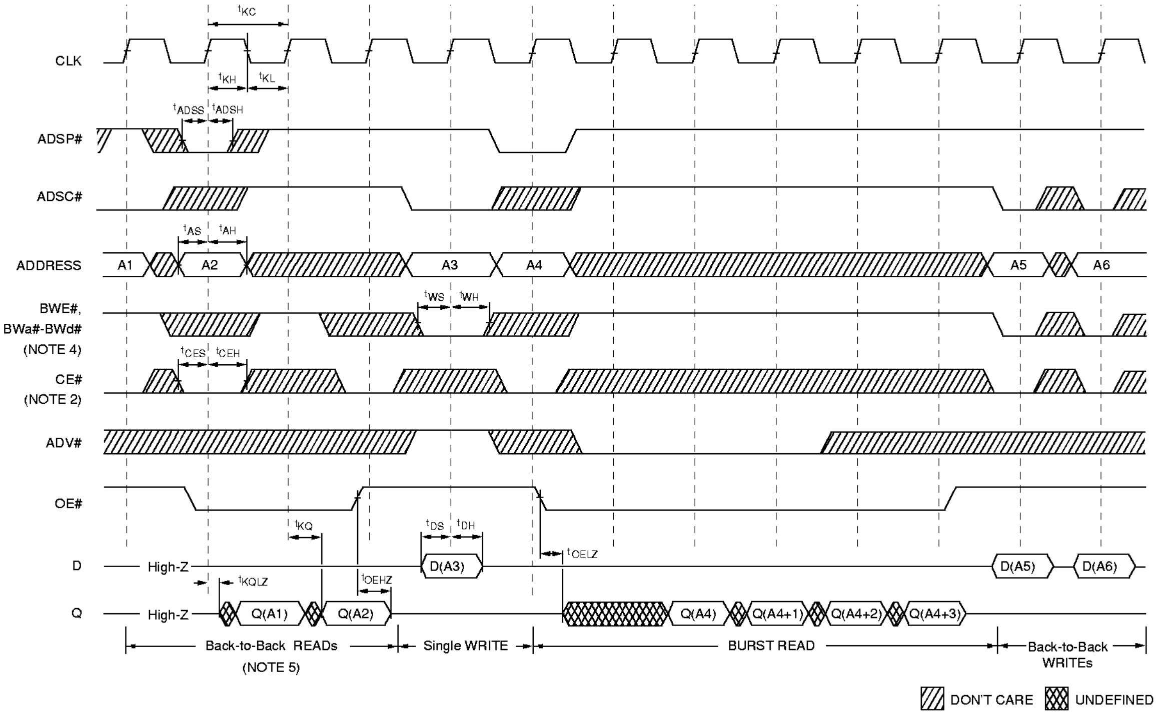
WRITE TIMING PARAMETERS

	-5		-6		-6.6		-7.5		-10		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tKC	5.0		6.0		6.6		7.5		10		ns
tKF		200		166		150		133		100	MHz
tKH	1.6		1.7		1.8		1.9		3.2		ns
tKL	1.6		1.7		1.8		1.9		3.2		ns
tOEHZ		3.0		3.5		3.8		4.2		4.5	ns
tAS	1.5		1.5		1.5		1.5		2.0		ns
tADSS	1.5		1.5		1.5		1.5		2.0		ns
tAAS	1.5		1.5		1.5		1.5		2.0		ns
tWS	1.5		1.5		1.5		1.5		2.0		ns

	-5		-6		-6.6		-7.5		-10		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tDS	1.5		1.5		1.5		1.5		2.0		ns
tCES	1.5		1.5		1.5		1.5		2.0		ns
tAH	0.5		0.5		0.5		0.5		0.5		ns
tADSH	0.5		0.5		0.5		0.5		0.5		ns
tAAH	0.5		0.5		0.5		0.5		0.5		ns
tWH	0.5		0.5		0.5		0.5		0.5		ns
tDH	0.5		0.5		0.5		0.5		0.5		ns
tCEH	0.5		0.5		0.5		0.5		0.5		ns

NOTE:
1. D(A2) refers to input for address A2. D(A2 + 1) refers to input for the next internal burst address following A2.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. OE# must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. ADV# must be HIGH to permit a WRITE to the loaded address.
5. Full-width WRITE can be initiated by GW# LOW; or by GW# HIGH, BWE# LOW and BWa#-BWb# LOW for x18 device; or GW# HIGH, BWE# LOW and BWa#-BWd# LOW for x32 and x36 devices.

READ/WRITE TIMING 3



READ/WRITE TIMING PARAMETERS

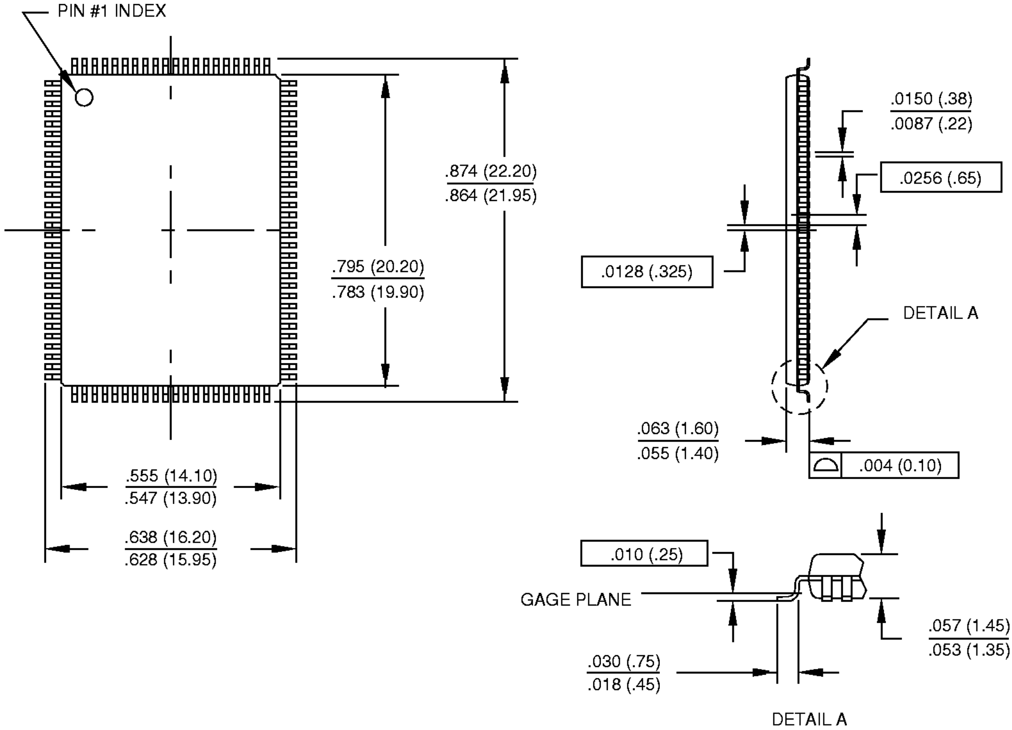
SYM	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-6.6 MIN	-6.6 MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
tKC	5.0		6.0		6.6		7.5		10		ns
tKF		200		166		150		133		100	MHz
tKH	1.6		1.7		1.8		1.9		3.2		ns
tKL	1.6		1.7		1.8		1.9		3.2		ns
tKQ		3.1		3.5		3.8		4.0		5.0	ns
tKQLZ	0		0		0		0		1.5		ns
tOELZ	0		0		0		0		0		ns
tOEHZ		3.0		3.5		3.8		4.2		4.5	ns
tAS	1.5		1.5		1.5		1.5		2.0		ns

SYM	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-6.6 MIN	-6.6 MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
tADSS	1.5		1.5		1.5		1.5		2.0		ns
tWS	1.5		1.5		1.5		1.5		2.0		ns
tDS	1.5		1.5		1.5		1.5		2.0		ns
tCES	1.5		1.5		1.5		1.5		2.0		ns
tAH	0.5		0.5		0.5		0.5		0.5		ns
tADSH	0.5		0.5		0.5		0.5		0.5		ns
tWH	0.5		0.5		0.5		0.5		0.5		ns
tDH	0.5		0.5		0.5		0.5		0.5		ns
tCEH	0.5		0.5		0.5		0.5		0.5		ns

NOTE:
1. Q(A4) refers to output from address A4. Q(A4 + 1) refers to output from the next internal burst address following A4.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an ADSP#, ADSC# or ADV# cycle is performed.
4. GW# is HIGH.
5. Back-to-back READs may be controlled by either ADSP# or ADSC#.

100-PIN TQFP

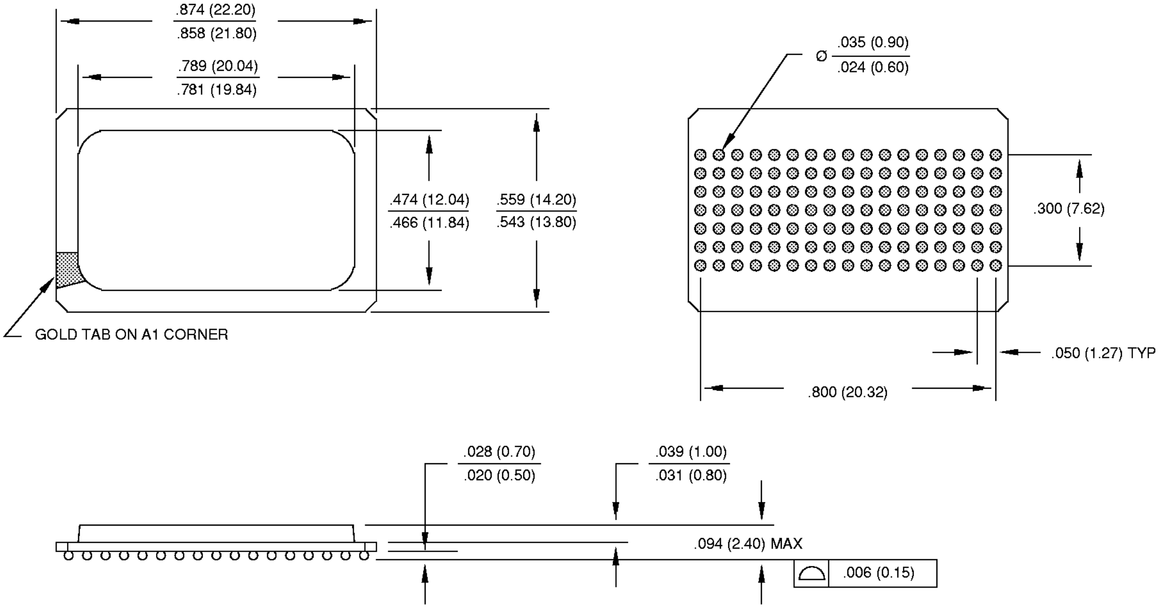
SA-1



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

119-BUMP BGA
SB-1



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992