MOTOROLA

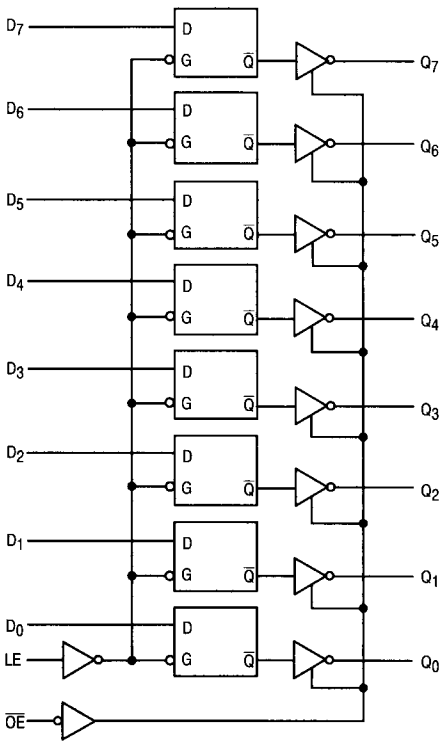
Octal D-Type Flip-Flop With Transparent Latch and 3-State Outputs

ELECTRICALLY TESTED PER:
MIL-M-38510/32502

The 54LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Input Clamp Diodes Limit High-Speed Termination Effects

LOGIC DIAGRAM



Military 54LS373

AVAILABLE AS:

1) JAN: JM38510/32502BXA
2) SMD: N/A
3) 883: 54LS373/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
$\overline{OE}$	1	1	1	V_{CC}
Q_0	2	2	2	V_{CC}
D_0	3	3	3	V_{CC}
D_1	4	4	4	V_{CC}
Q_1	5	5	5	V_{CC}
Q_2	6	6	6	V_{CC}
D_2	7	7	7	V_{CC}
D_3	8	8	8	V_{CC}
Q_3	9	9	9	V_{CC}
GND	10	10	10	GND
LE	11	11	11	V_{CC}
Q_4	12	12	12	V_{CC}
D_4	13	13	13	V_{CC}
D_5	14	14	14	V_{CC}
Q_5	15	15	15	V_{CC}
Q_6	16	16	16	V_{CC}
D_6	17	17	17	V_{CC}
D_7	18	18	18	V_{CC}
Q_7	19	19	19	V_{CC}
V_{CC}	20	20	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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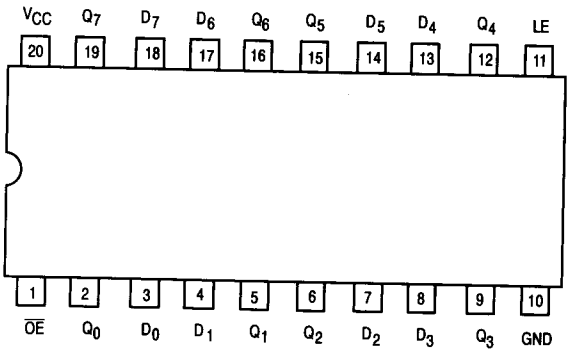
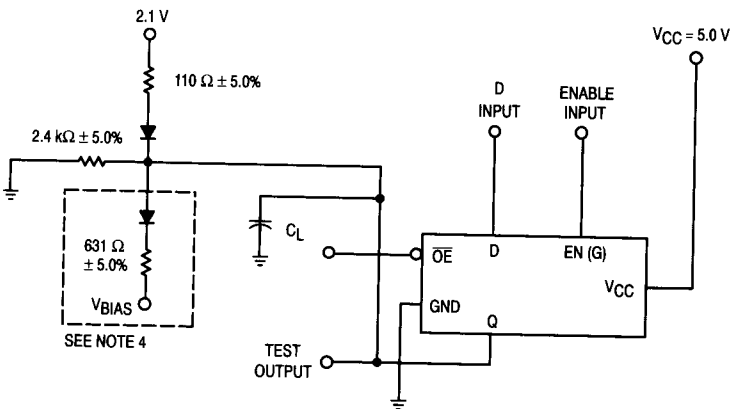
TRUTH TABLE			
Inputs		Outputs	
D_n	LE	$\overline{OE}$	Q_n
H	H	L	H
L	H	L	L
X	X	H	Z*

H = HIGH Logic Level
L = LOW Logic Level
X = Immaterial
Z = High Impedance
*Note: Contents of flip-flop unaffected by the state of the Output Enable input ($\overline{OE}$)

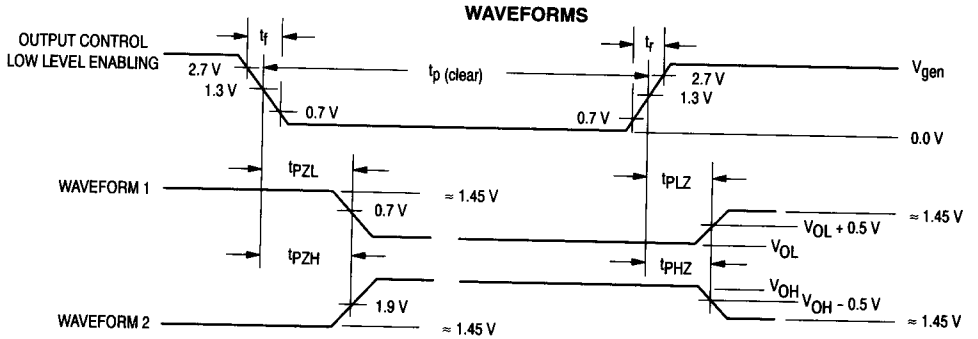
CONNECTION DIAGRAM



TRI-STATE SWITCHING TEST CIRCUIT



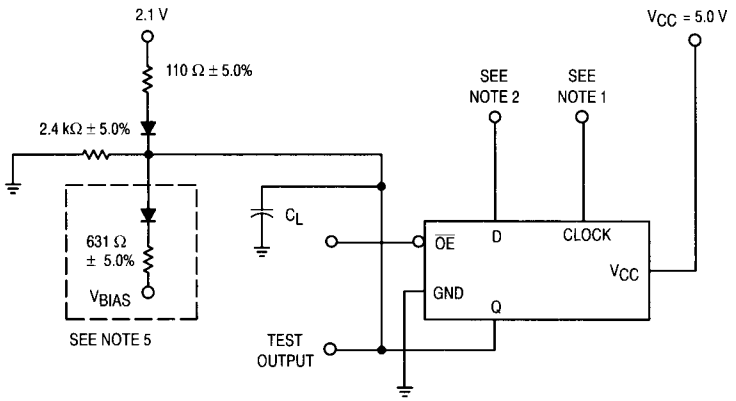
WAVEFORMS



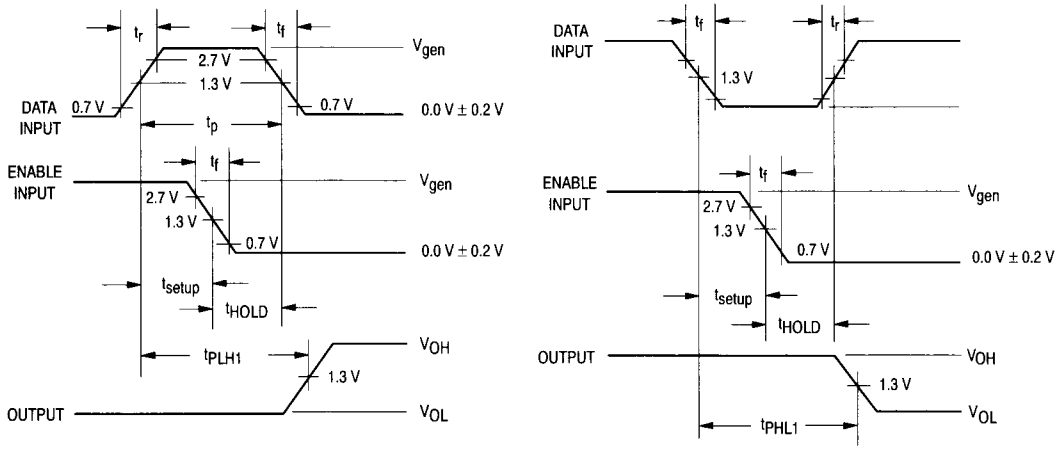
NOTES:

1. All diodes are 1N3064, or equivalent.
2. Output control pulse has the following characteristics: V_{gen} = 3.0 V ± 0.2 V, $t_f \leq 6.0$ ns, $t_r \leq 15$ ns, $t_{p(input)} \geq 200$ ns and PRR ≤ 1.0 MHz.
3. C_L = 50 pF ± 10% (including jig and probe capacitance).
4. The diode and resistor shown within the dotted area are optional. When the diode and resistor are used, V_{BIAS} shall be 5.5 V for all tests except for t_{PHZ}; for t_{PHZ} tests, V_{BIAS} shall be – 0.6 V.
5. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

SYNCHRONOUS SWITCHING (HIGH-LEVEL DATA) TEST CIRCUIT



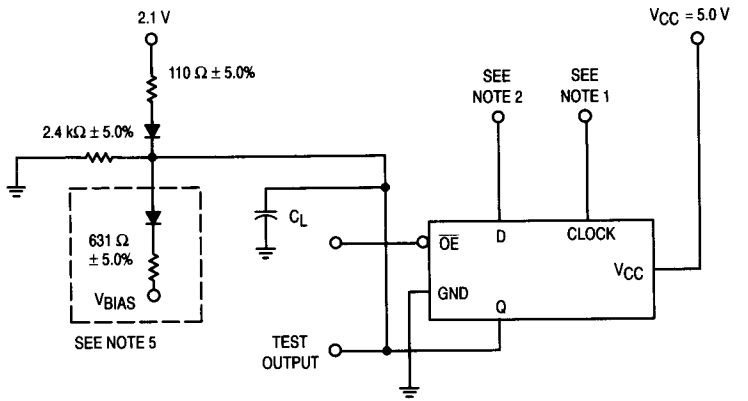
WAVEFORMS



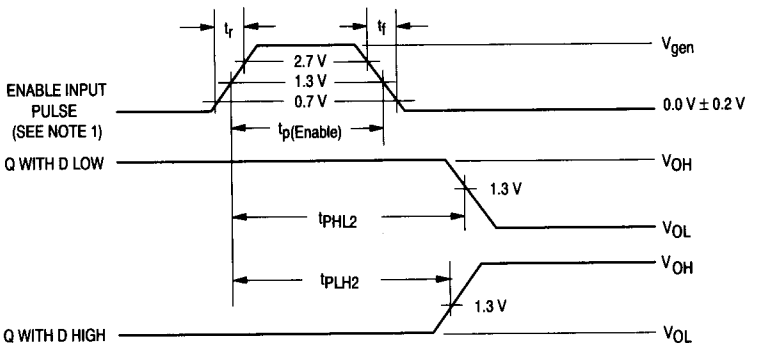
NOTES:

1. Enable input pulse has the following characteristics:
   V_{gen} = 3.0 V ± 0.2 V, $t_f \leq 6.0$ ns.
2. D input has the following characteristics:
   V_{gen} = 3.0 V ± 0.2 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, t_{setup} = 5.0 ns, t_{hold} = 20 ns, t_p = 25 ns.
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF ± 10% (including jig and probe capacitance).
5. The diode and resistor shown within the dotted area are optional. When the diode and resistor are used, V_{BIAS} shall be 5.5 V for all tests except for t_{PHZ}; for t_{PHZ} tests V_{BIAS} shall be – 0.6 V.
6. Terminal condition (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

SYNCHRONOUS SWITCHING (LOW-LEVEL DATA) TEST CIRCUIT



WAVEFORMS



NOTES:

1. Enable input characteristics for t_{PHL2} and t_{PLH2}:
   V_{gen} = 3.0 V ± 0.2 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, $t_{p(Enable)}$ = 15 ns and PRR ≤ 1.0 MHz.
2. All diodes are 1N3064, or equivalent.
3. C_L = 50 pF ± 10% (including jig and probe capacitance).
4. The diode and resistor shown within the dotted area are optional. When the diode and resistor are used, V_{BIAS} shall be 5.5 V for all tests except for t_{PHZ} ; for t_{PHZ} tests V_{BIAS} shall be – 0.6 V.
5. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		− 55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = − 1.0 mA, V_{IH} = 2.0 V, other inputs are open, $\overline{OE}$ = 0.7 V, LE = 2.0 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 12 mA, V_{IL} = 0.7 V, other inputs are open, LE = 2.0 V, $\overline{OE}$ = 0.7 V.
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} = 4.5 V, I_{IN} = − 18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open.
I_{IL1}	Logical "0" Input Current		− 400		− 400		− 400	µA	V_{CC} = 5.5 V, $V_{IN(\overline{OE})}$ = 0.4 V, other inputs are open.
I_{IL2}	Logical "0" Input Current	− 105	− 345	− 105	− 345	− 105	− 345	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open.
I_{IL3}	Logical "0" Input Current		− 400		− 400		− 400	µA	V_{CC} = 5.5 V, $V_{IN(LE)}$ = 0.4 V, other inputs are open.
I_{OS}	Output Short Circuit Current	− 30	− 130	− 30	− 130	− 30	− 130	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, other inputs are open, V_{OUT} = GND, LE = 5.5 V, $\overline{OE}$ = GND.
I_{IOZL}	Output Off Current High		20		20		20	µA	V_{CC} = 5.5 V, V_{IN} = 2.0 V, other inputs are open, V_{OUT} = 2.7 V, $\overline{OE}$ = 4.5 V, LE = 4.5 V.
I_{IOZH}	Output Off Current Low		− 20		− 20		− 20	µA	V_{CC} = 5.5 V, V_{IN} = 0.7 V, other inputs are open, V_{OUT} = 0.4 V, $\overline{OE}$ = 4.5 V, LE = 4.5 V.
I_{CCH}	Power Supply Current Off		40		40		40	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V (LE, $\overline{OE}$), other inputs are open.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.4 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay D_n to Q_n	3.0 —	18 18	3.0 —	24 23	3.0 —	24 23	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLH1} t_{PLH1}	Propagation Delay D_n to Q_n	3.0 —	18 18	3.0 —	24 23	3.0 —	24 23	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PHL2} t_{PHL2}	Propagation Delay LE to Q_n	3.0 —	30 30	3.0 —	39 38	3.0 —	39 38	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLH2} t_{PLH2}	Propagation Delay LE to Q_n	3.0 —	30 30	3.0 —	39 38	3.0 —	39 38	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLZ} t_{PLZ}	Output Disable Time	3.0 —	30 25	3.0 —	39 31	3.0 —	39 31	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 5.0 pF, R_L = 667 Ω.
t_{PHZ} t_{PHZ}	Output Disable Time	3.0 —	31 20	3.0 —	35 25	3.0 —	35 25	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 5.0 pF, R_L = 667 Ω.
t_{PZL} t_{PZL}	Output Enable Time	3.0 —	36 36	3.0 —	47 45	3.0 —	47 45	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PZH} t_{PZH}	Output Enable Time	3.0 —	28 28	3.0 —	37 32	3.0 —	37 32	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.

NOTES:
1. The limits specified for C_L = 45 pF and R_L = 667 Ω are guaranteed but not tested.
2. The limits specified for C_L = 5.0 pF and R_L = 667 Ω are guaranteed but not tested.

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