2-wire Serial EEPROM 32K/64K
# AF24BC32/64

FEATURES:

- Internally organized as 4096 x 8 (32K), 8192 x 8 (64K)
- Low-voltage and standard-voltage operation : 1.7 to 5.5 V
- 2-wire serial interface bus
- Data retention: 100 years
- High endurance: 1,000,000 Write Cycles
- 400kHz (1.7V ~ 5.5V) compatibility
- Self-timed write cycle (5ms max)

- Bi-directional data transfer protocol
- Write protect pin for hardware data protection
- 32-byte page write modes
- Allows for partial page writes
- Lead free package
- 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead MSOP (AF24BC32) and 8-lead UFDFPN (MLP) (AF24BC32) Packages

DESCRIPTION

Aplus Flash Technology's AF24BC32/64 provides 32K/64K of serial electrically erasable and programmable read-only memory (EEPROM). The wide Vdd range allows for low-voltage operation down to 1.7V. The device, fabricated using traditional CMOS EEPROM technology, is optimized for many industrial and commercial applications where low-voltage and low-power operation is essential. The AF24BC32/64 is available in 8-pin PDIP, 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead MSOP (AF24BC32) and 8-lead UFDFPN (MLP) (AF24BC32) packages and is accessed via a 2-wire serial interface.
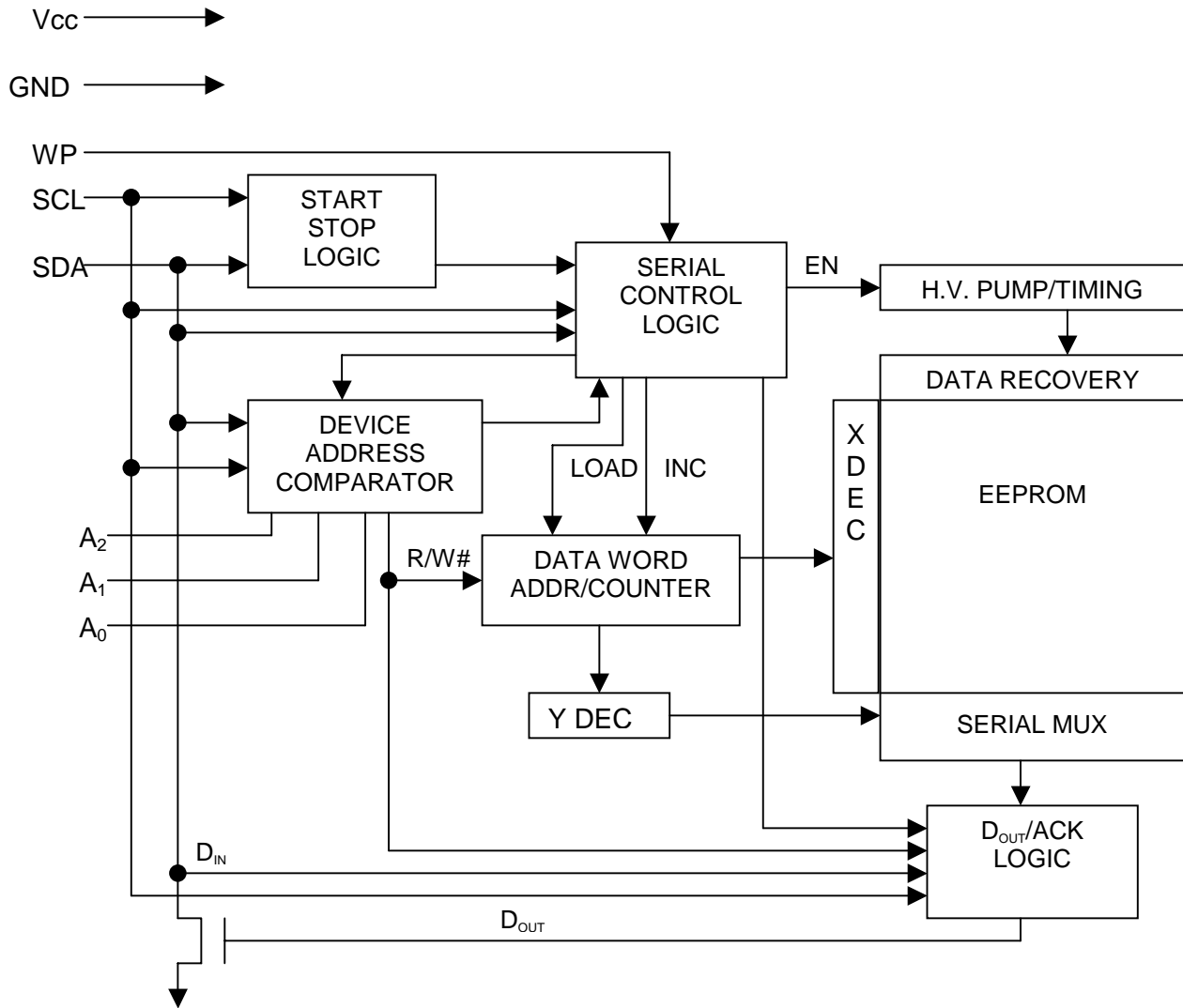
Figure 1. Pin Configurations

8-pin PDIP/TSSOP/SOIC/MSOP/UFDFPN(MLP)
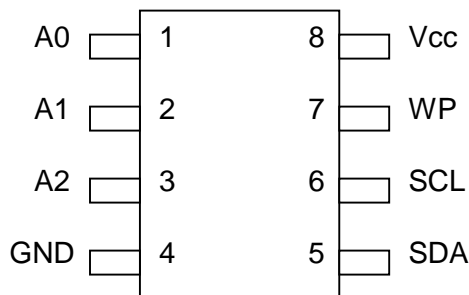
Pin Name	Function
A0 – A2	Address inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
GND	Ground
Vcc	Power Supply

Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

Operating Temperature……………………..-55ºC to +125ºC
Storage Temperature………..……………-65ºC to +150ºC
Voltage on Any Pin with
Respect to Ground...…………………..- 0.8V to Vcc +1.5V
Maximum Operating Voltage..………………………6.25V
DC Output Current……………………………………5.0 mA

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN DESCRIPTIONS

Serial Data (SDA): The SDA pin is used for sending and receiving data bits in serial mode. Since the SDA pin is defined as an open-drain connection, a pull-up resistor is needed.

Serial Clock (SCL): The SCL input is used to synchronize data input and output with the SDA pin. Data input is usually clocked on the rising edge of SCL, while data output is clocked out on the falling edge of SCL.

Device/Page Addresses (A2, A1, A0): The A2, A1, and A0 pins are used to address multiple devices on a single bus system and should be hard-wired. For the AF24BC32/64 chip, the A2, A1 and A0 pins provide the capability for addressing up to eight 32K/64K devices on a single bus system (please see the Device Addressing section for further details.) The A2, A1 and A0 pins are zero when they are not hard-wired.

Write Protect (WP): The AF24BC32/64 has a Write Protect pin that provides hardware data protection. When connected to ground, the Write Protect pin allows for normal read/write operations. If the WP pin is connected to Vcc, no data can be overwritten. WP function is handled under the top priority for status checking during power-on in order to protect the data security.

MEMORY ORGANIZATION

The internal memory organization for the AF24BC family is arranged differently for each of the densities. The AF24BC32/64 is internally organized as 128/256 pages of 32 bytes each and requires a 12/13-bit data word address.

PIN CAPACITANCE

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, Vcc = +1.8V

Symbol	Test Condition	Max	Units	Condition
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and not 100% tested.

DC CHARACTERISTICS

Applicable over recommended operating range from:

T_{AMB} = -40°C to +85°C, Vcc = +1.8V to +5.5V

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.7		5.5	V
V_{CC3}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	WRITE at 100kHz		3.0	5.0	mA
I_{SB1}	Standby Current V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
I_{SB2}	Standby Current V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}		1.4	4.0	µA
I_{SB3}	Standby Current V_{CC} = 5.5V	V_{IN} = V_{CC} or V_{SS}		5.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.2	5	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.1	5	µA
V_{IL}	Input Low Level (1)		-0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level (1)		V_{CC} x 0.7		Vcc+0.5V	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} =2.1mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.8V	I_{OL} =0.15 mA			0.2	V

Note: 1. V_{IL} and V_{IH} max are reference only and are not tested.

AC CHARACTERISTICS

Applicable over recommended operating range from:

T_{AMB} = -40°C to +85°C, Vcc = +1.8V to +5.5V, CL = 1 TTL Gate & 100pF (unless otherwise noted).

Symbol	Parameter	1.7 V-2.7V		2.7 V - 5.5 V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.2		µs
t_{HIGH}	Clock Pulse Width High	4.0		0.6		µs
t_I	Noise Suppression Time (1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	4.7		1.2		µs
$t_{HD.STA}$	Start Hold Time	4.0		0.6		µs
$t_{SU.STA}$	Start Setup Time	4.7		0.6		µs
$t_{HD.DAT}$	Data in Hold Time	0		0		µs
$t_{SU.DAT}$	Data in Setup Time	200		100		ns
t_R	Inputs Rise Time (1)		1.0		0.3	µs
t_F	Inputs Fall Time (1)		300		300	ns
$t_{SU.STO}$	Stop Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	100		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance (1)	5.0V, 25°C, Byte Mode	1M		1M		Write Cycles

Note: 1. This parameter is characterized and not 100% tested.

DEVICE OPERATION

Clock and Data Transitions: Transitions on the SDA pin should only occur when SCL is low (refer to the Data Validity timing diagram in Figure 5). If the SDA pin changes when SCL is high, then the transition will be interpreted as a START or STOP condition.

START Condition: A START condition occurs when the SDA transitions from high to low when SCL is high. The START signal is usually used to initiate a command (refer to the Start and Stop Definition timing diagram in Figure 6).

STOP Condition: A STOP condition occurs when the SDA transitions from low to high when SCL is high (refer to Figure 6. START and STOP Definition timing diagram). The STOP command will put the device into standby mode after no acknowledgment is issued during the read sequence.

Acknowledge: An acknowledgement is sent by pulling the SDA low to confirm that a word has been successfully received. All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words, so acknowledgments are usually issued during the 9th clock cycle.

Standby Mode: Standby mode is entered when the chip is initially powered-on or after a STOP command has been issued and any internal operations have been completed.

Memory Reset: In the event of unexpected power or connection loss, a START condition can be issued to restart the input command sequence. If the device is currently in write cycle mode, this command will be ignored.
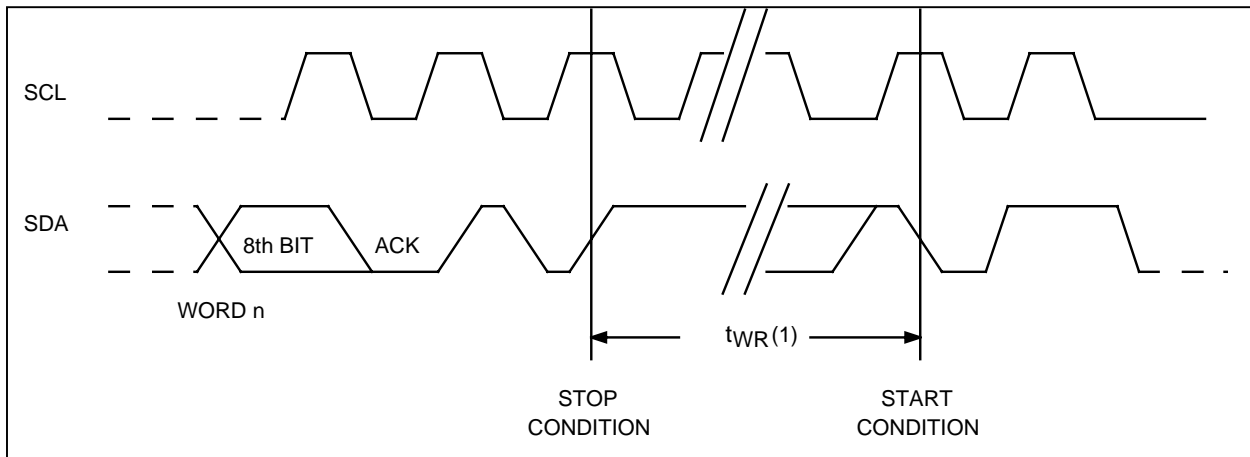
BUS TIMING

Figure 3. SCL: Serial Clock, SDA: Serial Data I/O
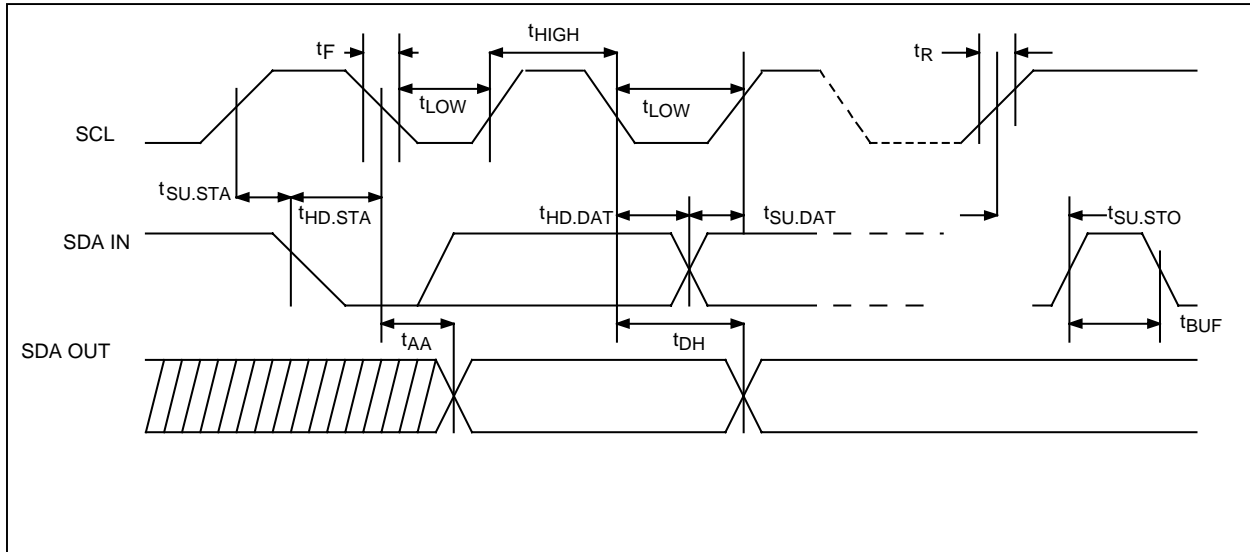
WRITE CYCLE TIMING

Figure 4. SCL: Serial Clock, SDA: Serial Data I/O

Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

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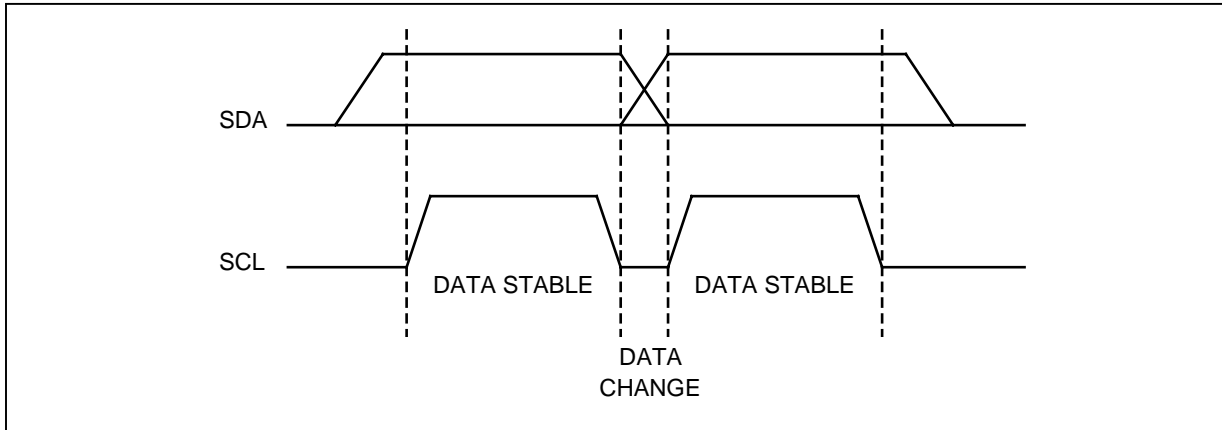Datasheet: AF24BC32/64

Figure 5. DATA VALIDITY

SDA

SCL

DATA STABLE

DATA STABLE

DATA
CHANGE

Figure 6. START AND STOP DEFINITION

SDA

SCL

START

STOP

Figure 7. OUTPUT ACKNOWLEDGE

SCL

1

8

9

DATA IN

DATA OUT

START
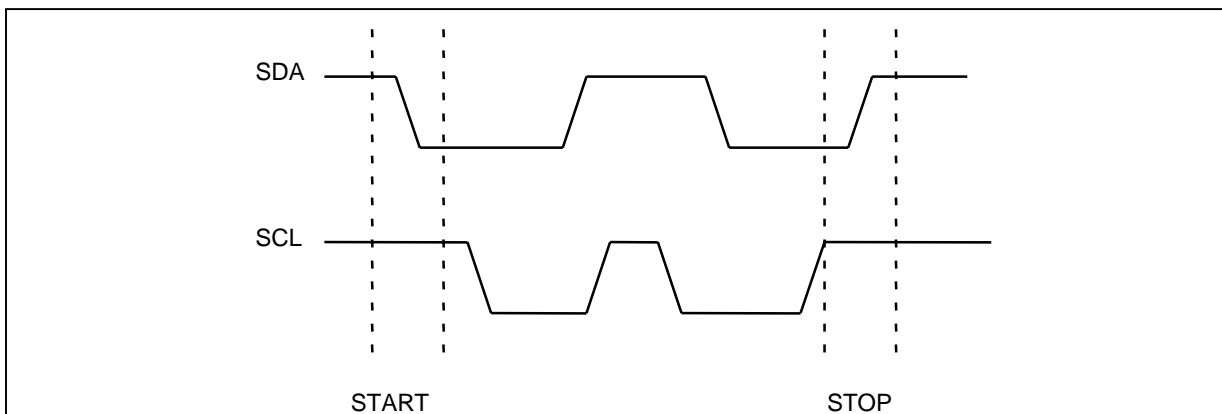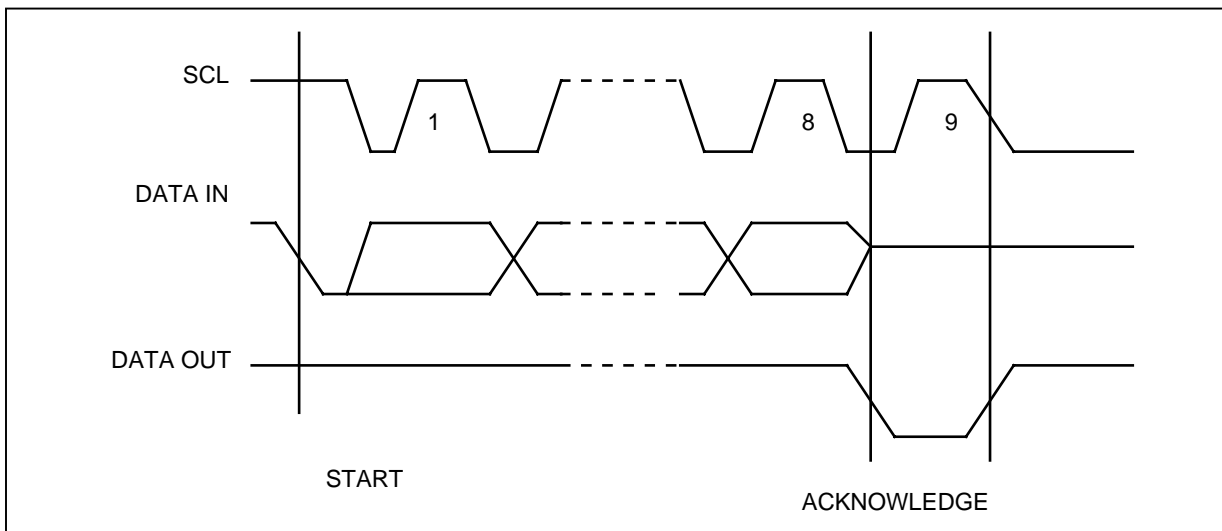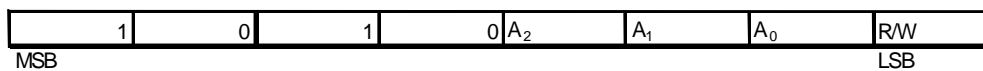
ACKNOWLEDGE

DEVICE ADDRESSING

To enable the chip for a read or write operation, an 8-bit device address word followed by a START condition must be issued. The 1st four bits of the device address word consists of a mandatory '1010' pattern. The next three bits should correspond to the address of the device, which is determined by the A2, A1, and A0 inputs (See Figure 8).

The eighth bit of the device address determines read or write operation. If the R/W bit is high, then a read operation is initiated. Otherwise, if the R/W bit is low, then a write operation is started.

Figure 8. Device Address

1	0	1	0	A_2	A_1	A_0	R/W
MSB							LSB

After comparing the device address and finding a match, the EEPROM device will issue an acknowledgment by pulling SDA low. If the comparison fails, the chip will return to standby mode.
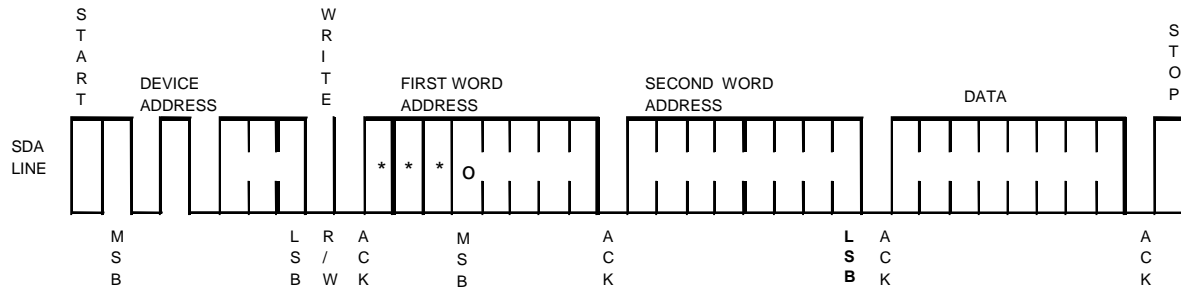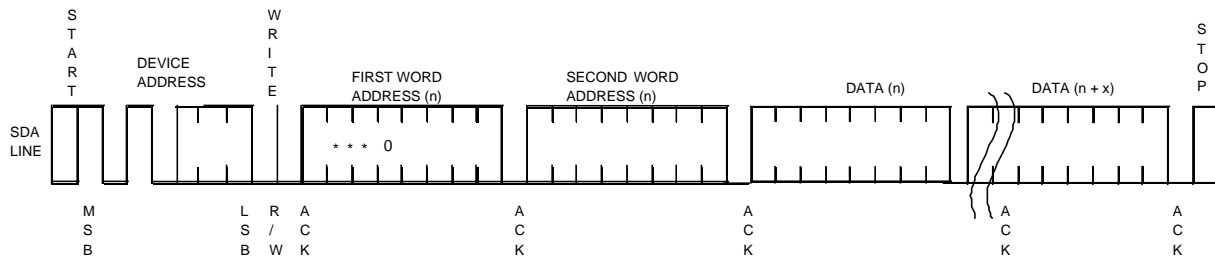
Figure 9. Byte Write

Figure 10. Page Write

(* = DON'T CARE bits for 32K/64K
o = DON'T CARE bits for 32K)

WRITE OPERATIONS

Byte/Page Write:

If a write operation is entered (R/$\overline{\text{W}}$=0) and an acknowledgment is sent, then the next sequence requires two sets of 8-bit data word addresses. After an acknowledgment is received after each address, the 1st byte of data can be loaded. The device will send an acknowledgment after each byte to confirm the transmission.

To begin the write cycle, a STOP condition must be issued (refer to Figure 9). Both byte and page write operations are supported, so the STOP condition can be issued after the 1st byte or the last byte in the page. When the STOP condition occurs, an internal timer is started, all inputs are disabled, and the EEPROM will not respond to any more commands until the write cycle is completed.

The internal page counter is incremented after each byte received, but the row location of the memory page will always remain the same. Therefore, the device will wrap around to the 1st byte in the page after the last byte in the page is received. Any further data loaded into the page buffer will overwrite the previous data loaded.

9

Acknowledge Polling: After the STOP condition is issued, the write cycle begins. Acknowledge polling can be initiated by sending a START condition followed by the device address word. If the EEPROM has completed the internal write cycle and returned to standby mode, the device will respond by sending back an acknowledgment by pulling the SDA pin low. Otherwise, the sequence will be ignored and no acknowledgment will be sent.

READ OPERATIONS

There are three types of read operations: current address read, random address read, and sequential read. A random address read can be considered a current address read operation with an additional sequence in the beginning to load a different address into the internal counter. A sequential read occurs when subsequent bytes are clocked out after a current address read or random address read occurs.

Current Address Read: A current address read operation is initiated by issuing R/W=1 in the device address word (refer to Figure 11). Since the internal address counter maintains the last address incremented by one accessed during the last read or write operation, the data output will correspond to this address. As long as the chip power is not disconnected, the internal address counter will always retain the last address incremented by one.

Random Read: To access a different address location than the one currently stored in the internal counter, a random read operation is provided. The random read is actually a combination of a "dummy" byte write sequence with a current address read command (refer to Figure 12). The "dummy" byte write loads a different address into the internal counter, and the data can then be accessed using the current address read.

Sequential Read: In order to access subsequent data words after a current address read or random read has been initiated, the user should send an acknowledgment to the EEPROM chip after each data byte received. If an acknowledgment is not received, then the chip will not send any more data and expect a STOP condition on the next cycle to reset back to standby mode (refer to Figure 13).

Sequential reads can be used to perform an entire chip read. Unlike the page write operation, the internal counter will increment to the next row after the last byte of the page has been reached. When the address reaches the last byte of the last memory page, the next address will increment to the 1st byte of the 1st memory page.

Once the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. When the microcontroller does not respond with a zero but does generate a following stop condition), the sequential read operation is terminated.
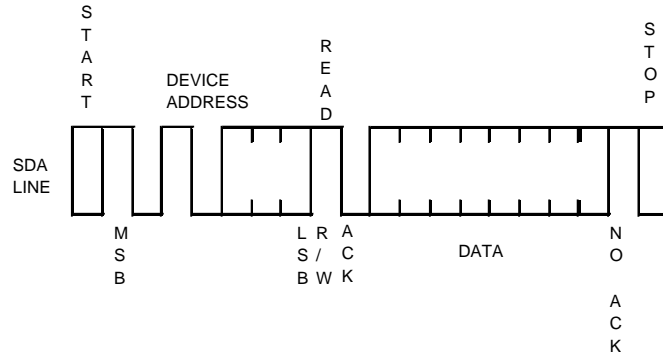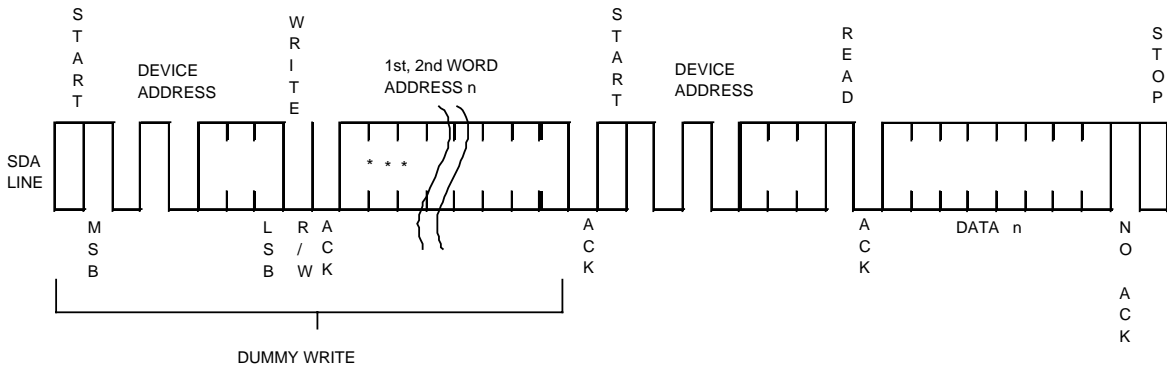
Figure 11. Current Address Read

Figure 12. Random Read

Note. 1. * = DON'T CARE bits

Figure 13. Sequential Read

Aplus Flash Technology, Inc.
Datasheet: AF24BC32/64
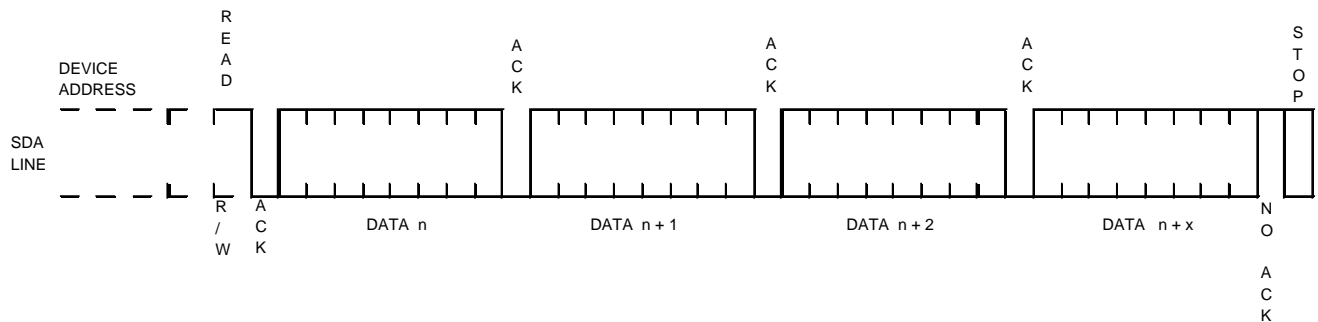
8L PDIP PACKAGE
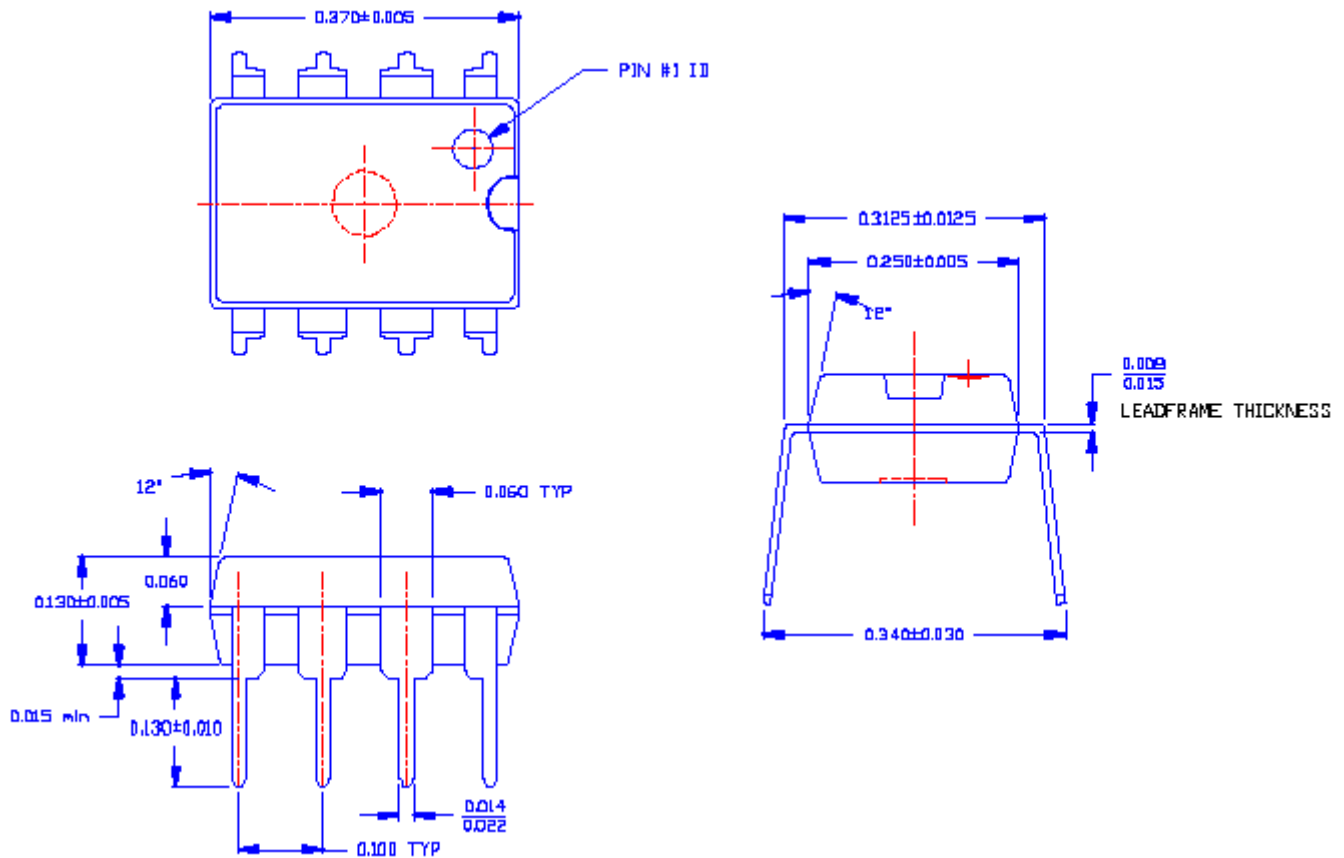
Note:
1) All package dimensions do not include mold flash. Mold flash shall not exceed 5 mils.
2) Lead dimensions does not include protrusions. Lead protrusions shall not exceed 10 mils and lead intrusion is not allowed.
3) All dimensions are in inches.

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8L SOIC PACKAGE

TOP VIEW

0.020 MAX.
0.013 MIN.

0.050 BSC

0.244 MAX.
0.232 MIN.

PIN #1 ID.

SIDE VIEW

0.030 MAX.
0.020 MIN.

0.008 +0.0015 -0.0005

0.154±0.003

0.150±0.003

0°~8°

0.028±0.002

FRONT VIEW

0.193±0.004

0.068 MAX.

0.057±0.002

0.009 MAX.
0.005 MIN.

Note:
1) All dimensions are in inches.

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8L TSSOP PACKAGE

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Datasheet: AF24BC32/64
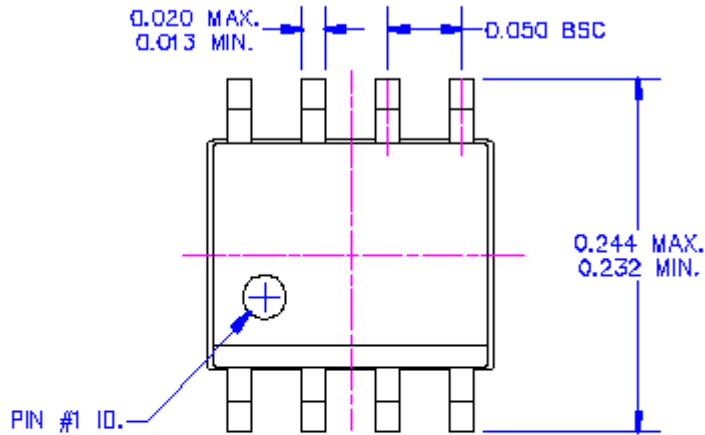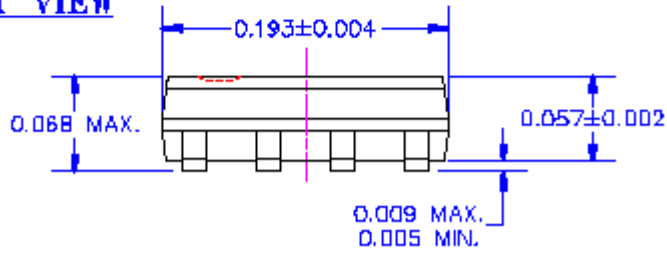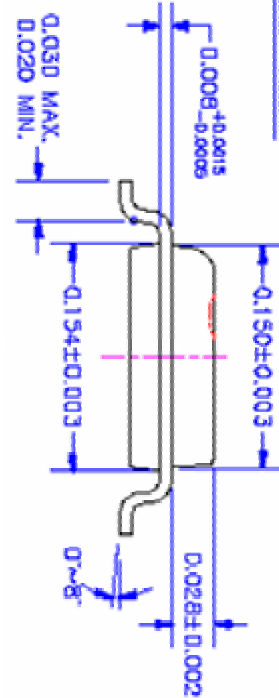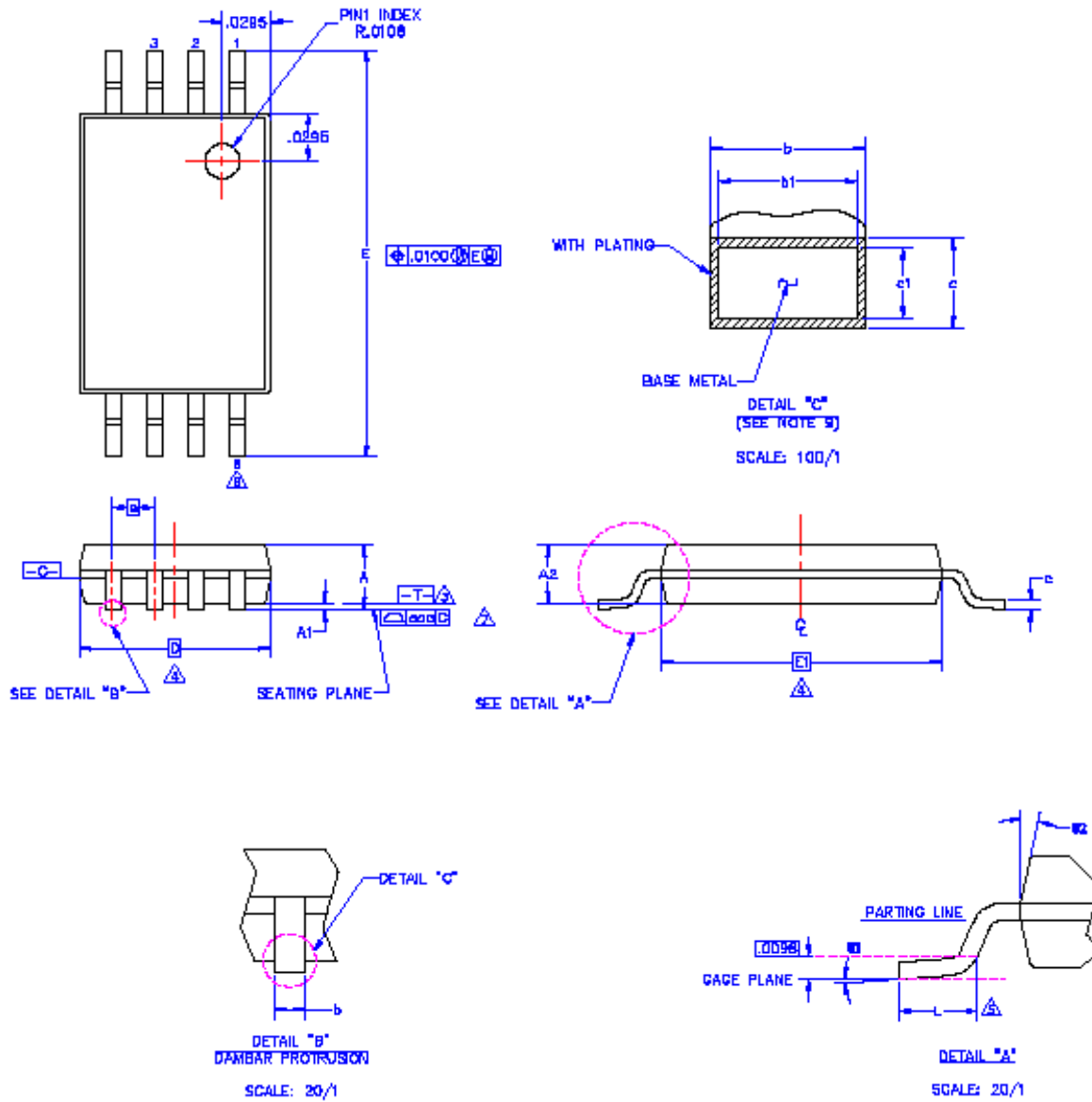
SYMBOL	DIMENSION					
	JEDEC STANDARD					
	IN MM			IN INCHES		
A	-	-	1.20	-	-	0.0472
A1	0.05	-	0.15	0.0020	-	0.0059
A2	0.80	1.00	1.05	0.0315	0.0394	0.0413
b	0.19	-	0.30	0.0075	-	0.0118
b1	0.19	0.22	0.25	0.0075	0.0087	0.0098
c	0.09	-	0.20	0.0035	-	0.0079
c1	0.09	-	0.16	0.0035	-	0.0063
D	2.90	3.00	3.10	0.1142	0.1181	0.1220
e	0.65BSC			0.0256 BSC		
E	6.4 BSC			0.2520 BSC		
E1	4.30	4.40	4.50	0.1693	0.1732	0.1772
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
θ1	0	-	8	0	-	8
θ2	12°REF			12°REF		
ααα	0.10			0.0039		

Notes:
1) Controlling dimensions are inches.
2) This package part is in compliance with JEDEC specification MD-153.
3) "T" is a reference datum.
4) "D" & "E" are reference datums and do not include mold flash or protrusions, and are measured at the parting line. Mold flash or protrusions shall not exceed 0.0059 per side.
5) Dimensions is the length of terminal for soldering to a substrate.
6) Terminal positions are shown for reference only.
7) Formed leads shall be planar with respect to one another within 0.0030 at seating plane.
8) The lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.0031 total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and an adjacent lead to be 0.0055. See details "B" and "C".
9) Detail "C" to be determined at 0.0039 to 0.0098 from the lead tip.

8L MSOP PACKAGE (AF24BC32)

DETAIL A

GAGE PLANE

0.25

PIN 1 INDICATOR ⌀0.45
x0.03DP SURFACE POLISHED

12°(4x)

12°(4x)

DETAIL A

Aplus Flash Technology, Inc.
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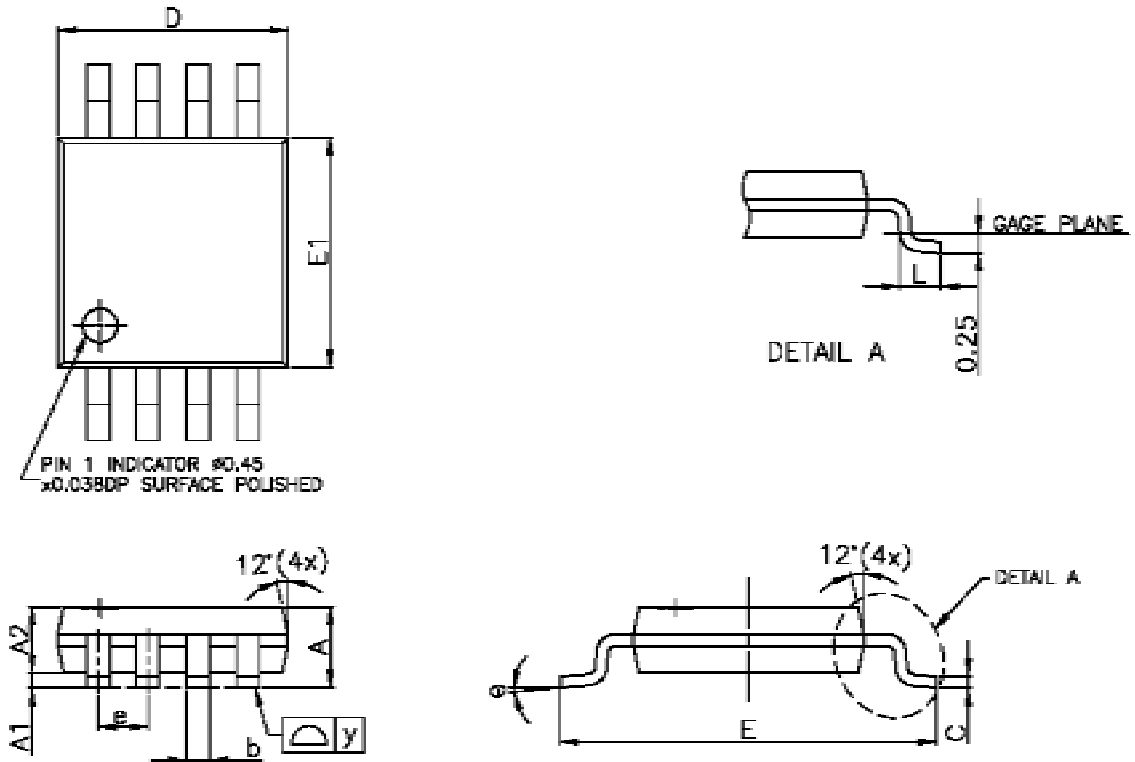
SYMBOLS	MSOP STANDARD					
	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.81	1.02	1.10	0.032	0.040	0.043
A1	0.05	-	0.15	0.002	-	0.006
A2	0.76	0.86	0.95	0.030	0.034	0.037
b	0.28	0.30	0.38	0.011	0.012	0.015
C	0.13	0.15	0.23	0.005	0.006	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.80	4.90	5.00	0.189	0.193	0.197
E1	2.90	3.00	3.10	0.114	0.118	0.122
e	-	0.65	-	-	0.0256	-
L	0.40	0.53	0.66	0.016	0.021	0.026
y	-	-	0.076	-	-	0.003
θ	0°	3°	6°	0°	3°	6°

Note:

1) **Controlling dimension: mm**
2) **Dimension "D" does not include Mold Flash, the bar burrs and gate burrs. Mold Flash, the bar burrs and gate burrs shall not exceed 0.006"[0.15mm] per end. Dimension "E1" does not include interlead Flash. Interlead Flash shall not exceed 0.010"[0.25mm] per side.**
3) **Dimension "b" does not include dambar protrusion. Allowable dambar protusion shall be 0.003"[0.08mm] total in exceed of the "b" dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead to be 0.0028"[0.07mm].**
4) **Tolerance: ± 0.010"[0.25mm] unless otherwise specified.**
5) **Otherwise dimension follow acceptable spec.**

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Datasheet: AF24BC32/64

8L UFDFPN (MLP) PACKAGE (AF24BC32)
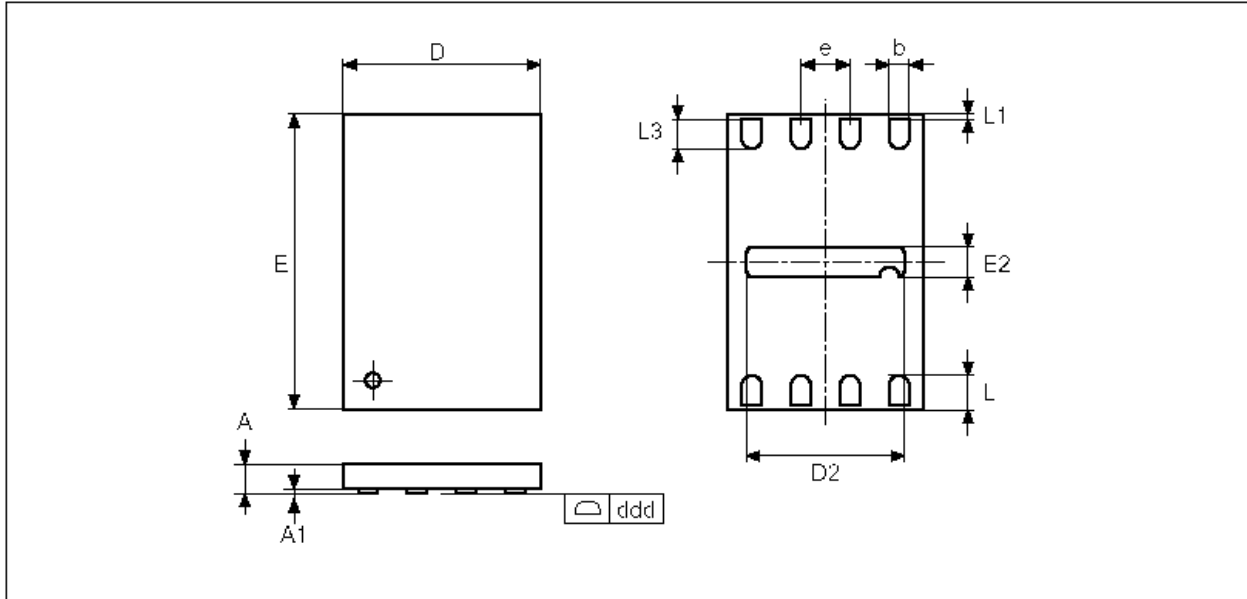
Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.55	0.50	0.60	0.022	0.020	0.024
A1	0.02	0.00	0.05	0.001	0.000	0.002
b	0.25	0.20	0.30	0.010	0.008	0.012
D	2.00	1.90	2.10	0.079	0.075	0.083
D2	1.60	1.50	1.70	0.063	0.059	0.067
ddd			0.08			0.003
E	3.00	2.90	3.10	0.118	0.114	0.122
E2	0.20	0.10	0.30	0.008	0.004	0.012
e	0.50	-	-	0.020	-	-
L	0.45	0.40	0.50	0.018	0.016	0.020
L1			0.15			0.006
L3		0.30			0.012	

AF24BC32 Ordering Information

Ordering Code	Package	Operating Ranges
AF24BC32 – PI	P	Lead free
AF24BC32 – SI	S	Industrial
AF24BC32 – TI	T	(-40°C to +85°C)
AF24BC32 – MI	M	
AF24BC32 – UI	U	

AF24BC64 Ordering Information

Ordering Code	Package	Operating Ranges
AF24BC64 – PI	P	Lead free
AF24BC64 – SI	S	Industrial
AF24BC64 – TI	T	(-40°C to +85°C)

Package Type	
P	8-pin, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
T	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
M	8-lead, Mini Small Outline Plastic Package (MSOP)
U	8-lead, Ultra thin Fine pitch Dual Flat Package No lead (UFDFPN (MLP))

PRODUCT ORDERING INFORMATION

AF24 BC aa -Y Z

Device Type

AF24

Supply Voltage

BC = 1.8V to 5.5V

Device Function
32 = 32 Kbit (4096 x 8)
64 = 64 Kbit (8192 x 8)

Package

P = PDIP
S = SOIC
T = TSSOP
M = MSOP
U = UFDFPN (MLP)

Temperature

I = Industrial (-40°C ~ 85°C)

Aplus Flash Technology, Inc.
Datasheet: AF24BC32/64

REVISIONS

Version Number	Description	Page	Date
1.0	Initial Release		3/5/05
1.1	Remove "Preliminary" and corrected the parameters of DC and AC.	**4**	5/25/06
1.2	Re-design WP pin functionality to top priority for status checking during power-on sequence	**3**	12/18/06
1.3	Add lead free description	**1, 18**	10/15/2007
1.4	(1) 1.8V @ 400kHz compatibility (2) 8L UFDFPN (MLP) PACKAGE (AF24BC32)	**1, 18**	12/24/07

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Note the following details:

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