ICS87974I-01

LOW SKEW, 1-TO-15, DIFFERENTIAL-TO-LVCMOS / LVTTL CLOCK GENERATOR

GENERAL DESCRIPTION

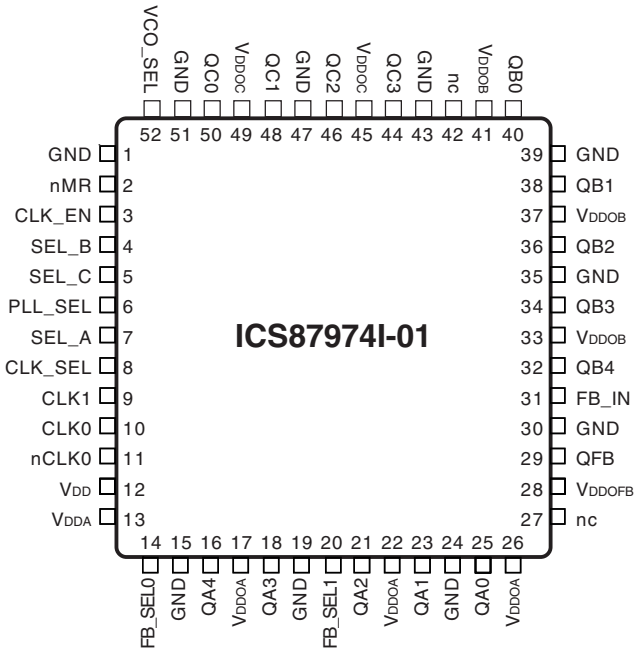
The ICS87974I-01 is a low skew, low jitter 1-to-15 Differential-to-LVCMOS / LVTTL Clock Generator/Zero Delay Buffer. The device has a fully integrated PLL and three banks whose divider ratios can be independently controlled, providing output frequency relationships of 1:1, 2:1, 3:1, 3:2, 3:2:1. In addition, the external feedback connection provides for a wide selection of output-to-input frequency ratios.The CLK1 and CLK0, nCLK0 pins allow for redundant clocking on the input and dynamically switching the PLL between two clock sources.

Guaranteed low jitter and output skew characteristics make the ICS87974I-01 ideal for those applications demanding well defined performance and repeatability.

FEATURES

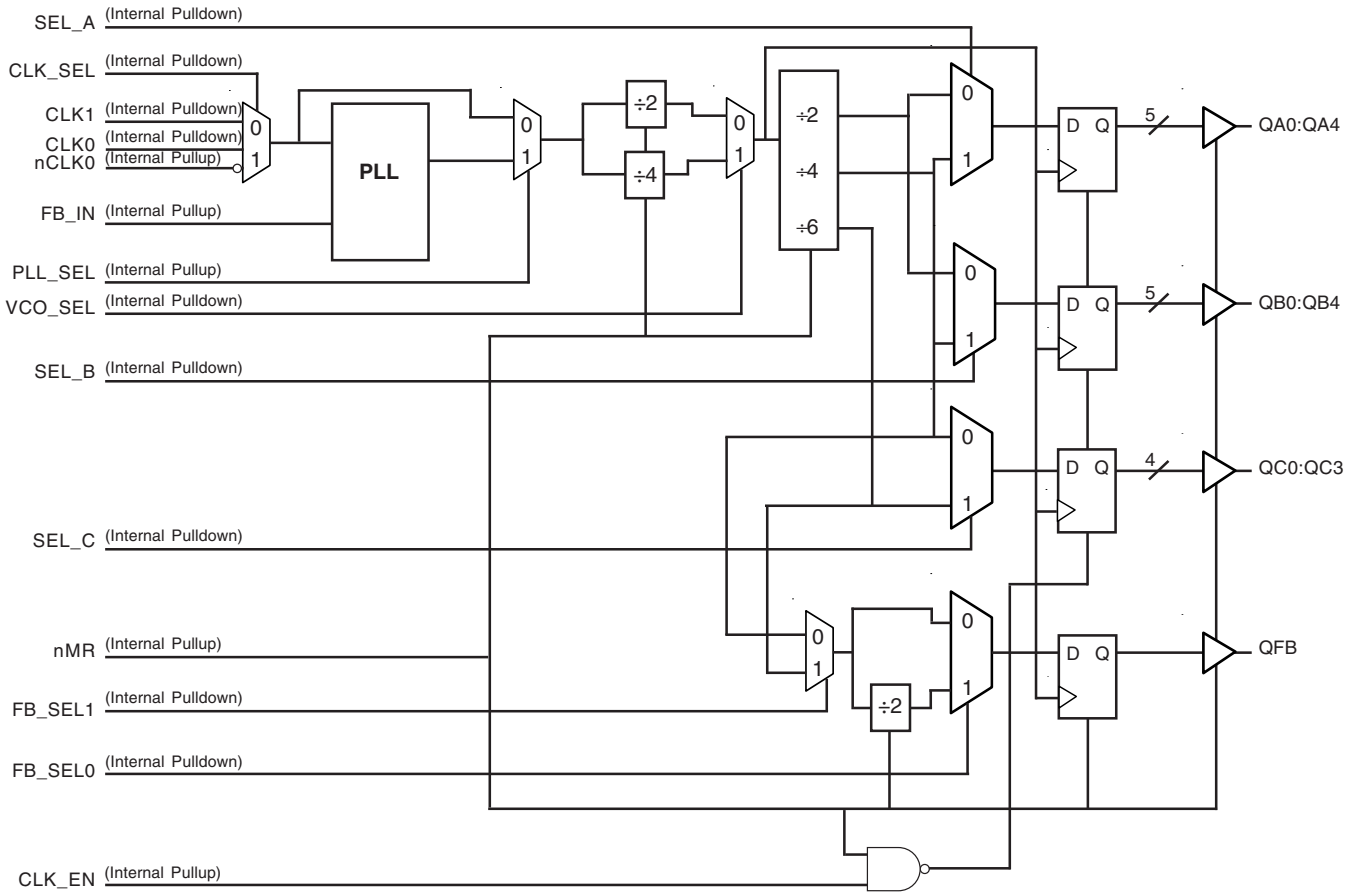
- Fully integrated PLL
- 15 single ended 3.3V LVCMOS / LVTTL outputs
- Selectable CLK1 or differential CLK0, nCLK0 inputs for redundant clock applications
- CLK1 accepts LVCMOS or LVTTL input levels
- CLK0, nCLK0 pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Maximum output frequency: 125MHz
- VCO range: 250MHz to 500MHz
- External feedback for "zero delay" clock regeneration
- Cycle-to-cycle jitter: 50ps (maximum)
- Output skew: 200ps (maximum)
- Bank skew: 70ps (maximum)
- PLL reference zero delay: CLK1: -150ps to 150ps
  CLK0, nCLK0: -475ps to -175ps
- 3.3V operating supply
- -40°C to 70°C ambient operating temperature

PIN ASSIGNMENT



52-Lead LQFP
10mm x 10mm x 1.4mm package body
Y package
Top View

BLOCK DIAGRAM



SIMPLIFIED BLOCK DIAGRAM

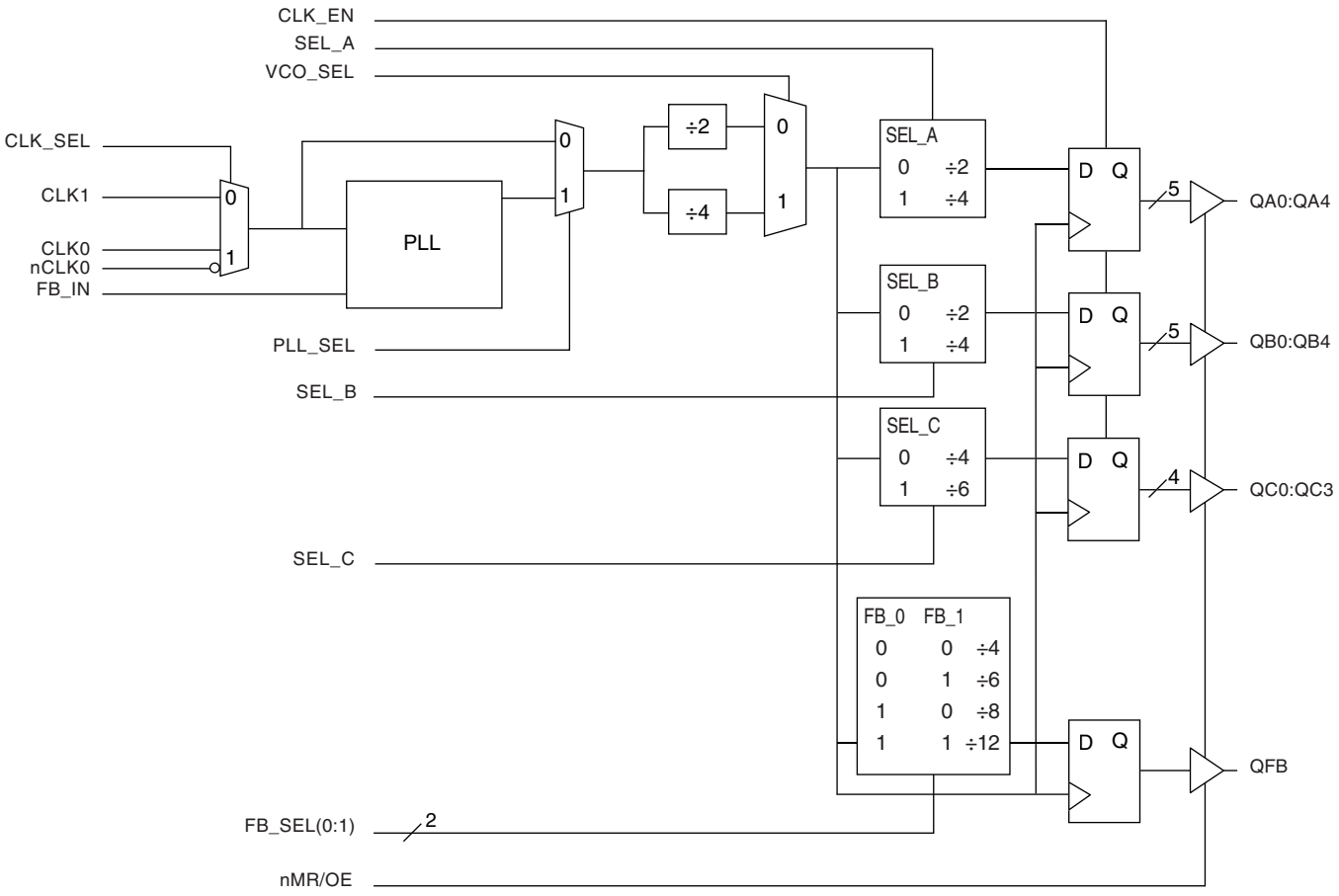


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 15, 19, 24, 30, 35, 39, 43, 47, 51	GND	Power		Power supply ground.
2	nMR	Input	Pullup	Active LOW Master Reset. When logic LOW, the internal dividers are reset causing the outputs to go low. when logic HIGH, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
3	CLK_EN	Input	Pullup	Clock enable. When LOW, all outputs except QFB are low. LVCMOS / LVTTL interface levels.
4	SEL_B	Input	Pulldown	Selects divide value for Bank B output as described in Table 3. LVCMOS / LVTTL interface levels.
5	SEL_C	Input	Pulldown	Selects divide value for Bank C output as described in Table 3. LVCMOS / LVTTL interface levels.
6	PLL_SEL	Input	Pullup	Selects between the PLL and the reference clock as the input to the dividers. When HIGH, selects PLL. When LOW, selects the reference clock. LVCMOS / LVTTL interface levels.
7	SEL_A	Input	Pulldown	Selects divide value for Bank A output as described in Table 3. LVCMOS / LVTTL interface levels.
8	CLK_SEL	Input	Pulldown	Clock select input. LVCMOS / LVTTL interface levels.
9	CLK1	Input	Pulldown	Clock input. LVCMOS / LVTTL interface levels.
10	CLK0	Input	Pulldown	Non-inverting differential clock input.
11	nCLK0	Input	Pullup	Inverting differential clock input
27, 42	nc	Unused		No connect.
12	V_{DD}	Power		Core supply pin.
13	V_{DDA}	Power		Analog supply pin.
14, 20	FB_SEL0, FB_SEL1	Input	Pulldown	Selects divide value for Bank feedback output as described in Table 3. LVCMOS / LVTTL interface levels.
16, 18, 21, 23, 25	QA4, QA3, QA2, QA1, QA0	Output		Bank A clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
17, 22, 26	V_{DDOA}	Power		Output supply pins for Bank A clock outputs.
28	V_{DDOFB}	Power		Output supply pin for QFB clock output.
29	QFB	Output		Clock output. LVCMOS / LVTTL interface levels.
31	FB_IN	Input	Pullup	Feedback input to phase detector for generating clocks with "zero delay". Connect to pin 29. LVCMOS / LVTTL interface levels.
32, 34, 36, 38, 40	QB4, QB3, QB2, QB1, QB0	Output		Bank B clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
33, 37, 41	V_{DDOB}	Power		Output supply pins for Bank B clock outputs.
44, 46, 48, 50	QC3, QC2, QC1, QC0	Output		Bank C clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
45, 49	V_{DDOC}	Power		Output supply pins for Bank C clock outputs.
52	VCO_SEL	Input	Pulldown	Selects VCO ÷ 4 when HIGH. Selects VCO ÷ 2 when LOW. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance		5	7	12	Ω
C_{PD}	Power Dissipation Capacitance (per output)	$V_{DD,}$ V_{DDA}, V_{DDOx} = 3.465V; NOTE 1			15	pF

NOTE 1: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOFB}.

TABLE 3A. OUTPUT CONTROL PIN FUNCTION TABLE

Inputs		Outputs			
nMR	CLK_EN	QA0:QA4	QB0:QB4	QC0:QC3	QFB
0	X	HiZ	HiZ	HiZ	HiZ
1	0	LOW	LOW	LOW	Enable
1	1	Enable	Enable	Enable	Enable

TABLE 3B. OPERATING MODE FUNCTION TABLE

Inputs	Operating Mode
PLL_SEL	
0	Bypass
1	PLL

TABLE 3C. PLL INPUT FUNCTION TABLE

Inputs	
CLK_SEL	PLL Input
0	CLK1
1	CLK0, nCLK0

TABLE 3D. SELECT PIN FUNCTION TABLE

SEL_A	QAx	SEL_B	QBx	SEL_C	QCx
0	÷ 2	0	÷ 2	0	÷ 4
1	÷ 4	1	÷ 4	1	÷ 6

TABLE 3E. FB SELECT FUNCTION TABLE

Inputs		Outputs
FB_SEL1	FB_SEL0	QFB
0	0	÷ 4
0	1	÷ 6
1	0	÷ 8
1	1	÷ 12

TABLE 3F. VCO SELECT FUNCTION TABLE

Inputs	
VCO_SEL	fVCO
0	VCO/2
1	VCO/4

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOx} = 3.3V±5\%$, T_A = -40°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDOx}	Output Supply Voltage; NOTE 1		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				125	mA
I_{DDO}	Output Supply Current				25	mA
I_{DDA}	Analog Supply Current				15	mA

NOTE 1: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOFB}.

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOx} = 3.3V±5\%$, T_A = -40°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	FB_SEL0, FB_SEL1, CLK1, SEL_A:SEL_C, CLK_SEL, VCO_SEL	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		FB_IN, nMR, PLL_SEL, CLK_EN	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	FB_SEL0, FB_SEL1, CLK1, SEL_A:SEL_C, CLK_SEL, VCO_SEL	V_{IN} = 0V, V_{DD} = 3.465V	-5			µA
		FB_IN, nMR, PLL_SEL, CLK_EN	V_{IN} = 0V, V_{DD} = 3.465V	-150			µA
V_{OH}	Output High Voltage; NOTE 1			2.4			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDOx}/2.

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOx} = 3.3V±5\%$, T_A = -40°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0	$V_{DD} = V_{IN} = 3.465V$			150	µA
		nCLK0	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	CLK0	$V_{IN} = 0V$, $V_{DD} = 3.465V$	-5			µA
		nCLK0	$V_{IN} = 0V$, $V_{DD} = 3.465V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} -0.85	V

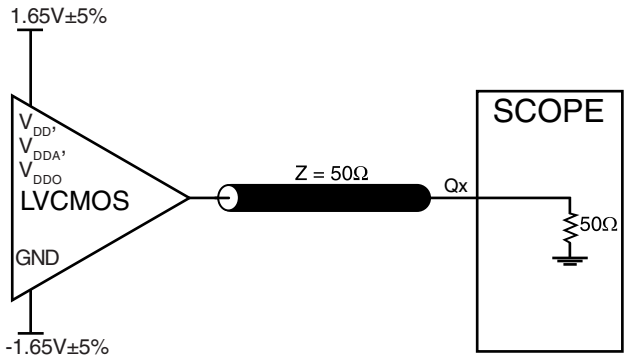
NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK0, nCLK0 is V_{DD} + 0.3V.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOx} = 3.3V±5\%$, T_A = -40°C TO 70°C

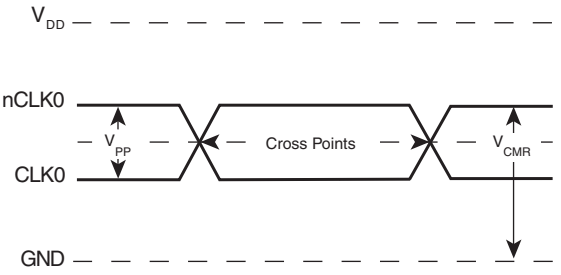
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		Qx ÷ 2, VCO ÷ 2			125	MHz
			Qx ÷ 4, VCO ÷ 2			62.5	MHz
			Qx ÷ 6, VCO ÷ 2			41.67	MHz
f_{VCO}	PLL VCO Lock Range; NOTE 5			250		500	MHz
t(Ø)	PLL Reference Zero Delay; NOTE 2, 5, 6	CLK1	PLL_SEL = 1	-150	0	150	ps
		CLK0, nCLK0		-475	-325	-175	ps
tsk(b)	Bank Skew; NOTE 3, 5					70	ps
*t*sk(o)	Output Skew; NOTE 4, 5					200	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 5		VCO = 500MHz, Div 4			50	ps
t_L	PLL Lock Time					10	mS
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		700	ps
odc	Output Duty Cycle			45		55	%
t_{EN}	Output Enable Time					10	ns
t_{DIS}	Output Disable Time					10	ns

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the V_{DD}/2 point of the input to theV_{DDOx}/2 of the output.
NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew within a bank with equal load conditions.
NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDOx}/2.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6: Reference frequency of 50MHz used with all banks in DIV4.

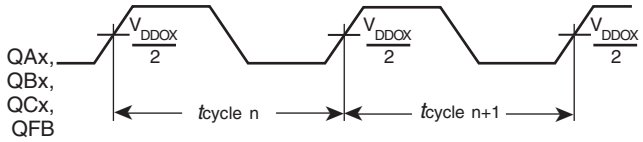
PARAMETER MEASUREMENT INFORMATION



3.3V OUTPUT LOAD AC TEST CIRCUIT



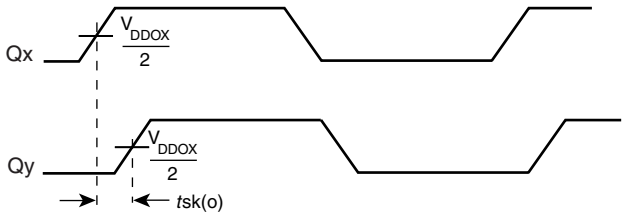
DIFFERENTIAL INPUT LEVEL



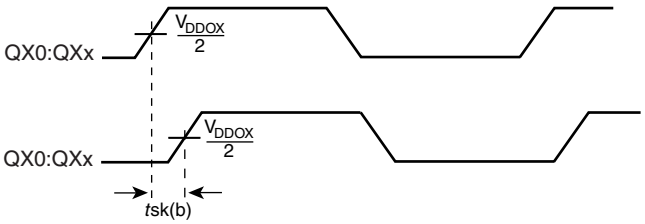
$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$

1000 Cycles

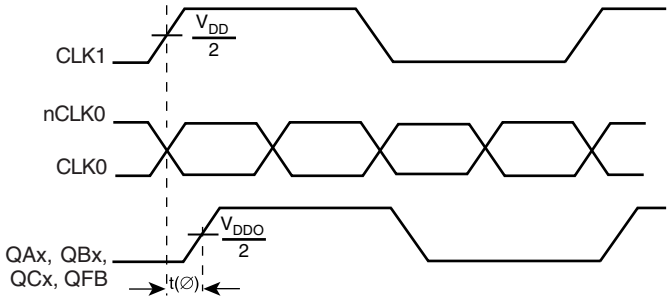
CYCLE-TO-CYCLE JITTER



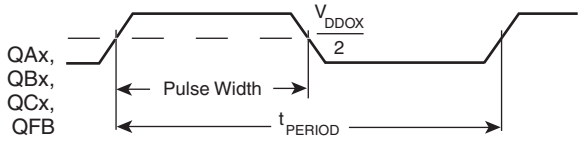
OUTPUT SKEW



BANK SKEW (where X denotes outputs in the same bank)

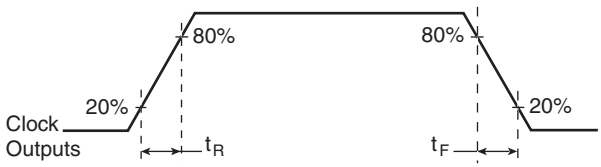


STATIC PHASE OFFSET



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RIS/FALL TIME

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

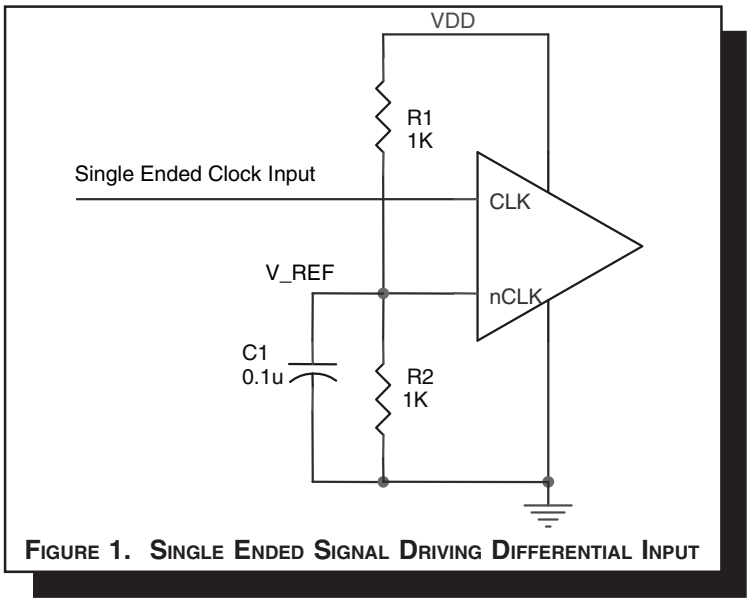


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS87974I-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDOx} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

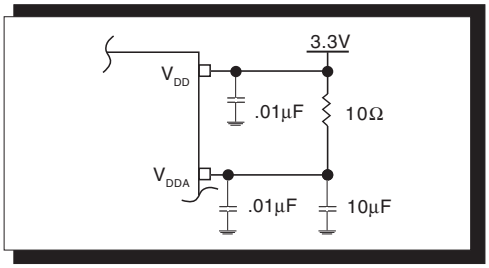


FIGURE 2. POWER SUPPLY FILTERING

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3D show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A,* the input termination applies for LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

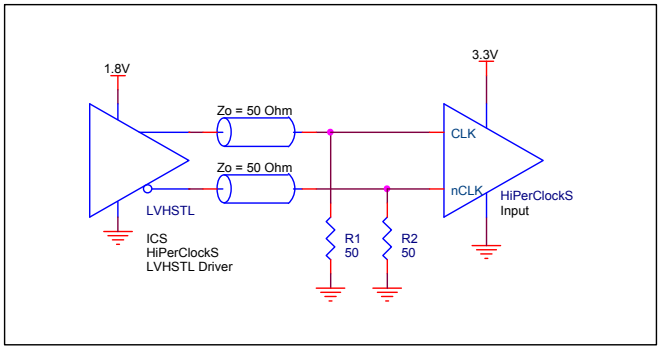


FIGURE 3A. CLK/nCLK INPUT DRIVEN BY LVHSTL DRIVER

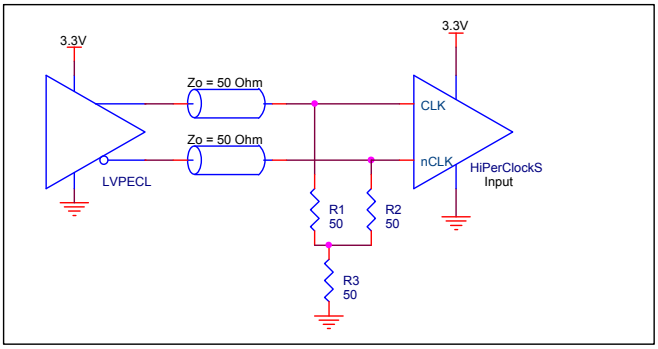


FIGURE 3B. CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

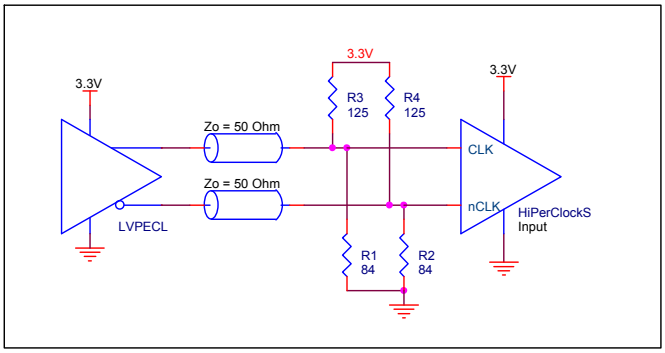


FIGURE 3C. CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

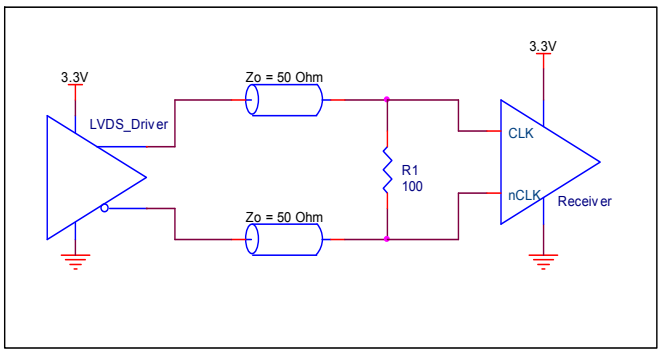


FIGURE 3D. CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

SCHEMATIC EXAMPLE

This application note provides general design guide using ICS87974I-01 LVCMOS buffer. Figure 4 shows a schematic example of the ICS87974I-01 LVCMOS clock generator. In this example, the input is driven by an LVCMOS driver.

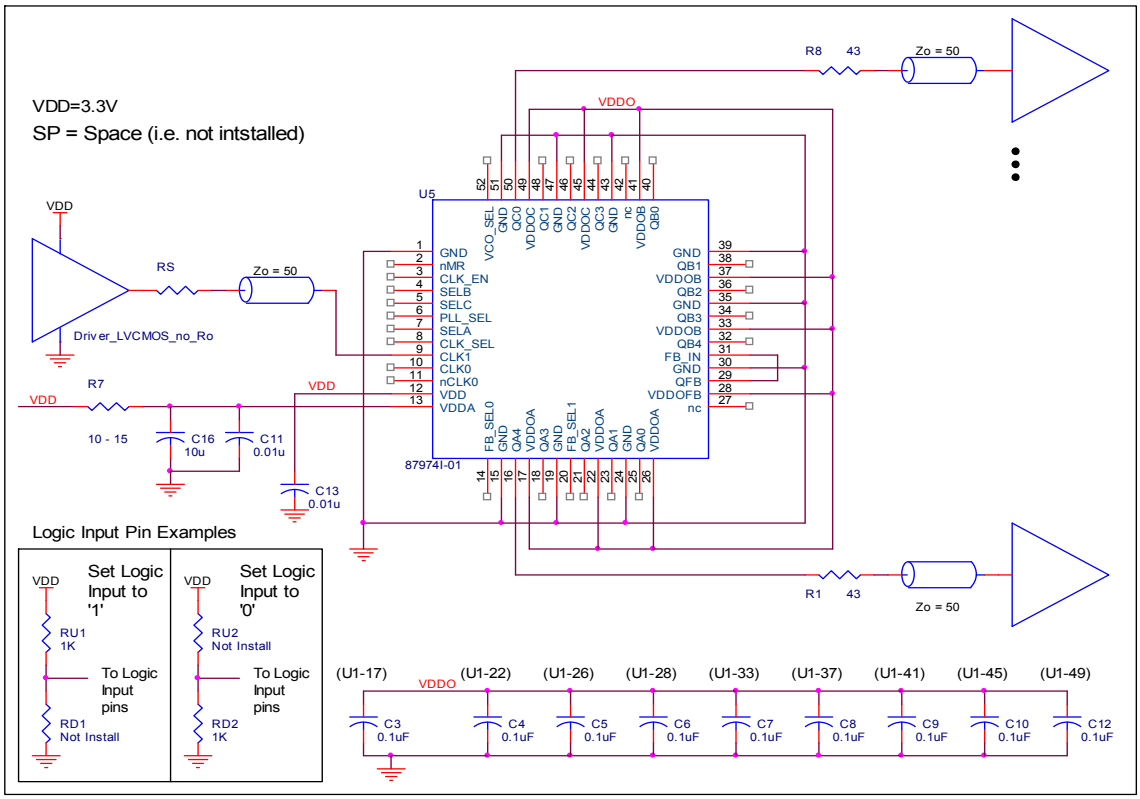


FIGURE 4. EXAMPLE ICS87974I-01 LVCMOS/LVTTL CLOCK OUTPUT BUFFER SCHEMATIC

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 52 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87974I-01 is: 4225

PACKAGE OUTLINE - Y SUFFIX FOR 52 LEAD LQFP

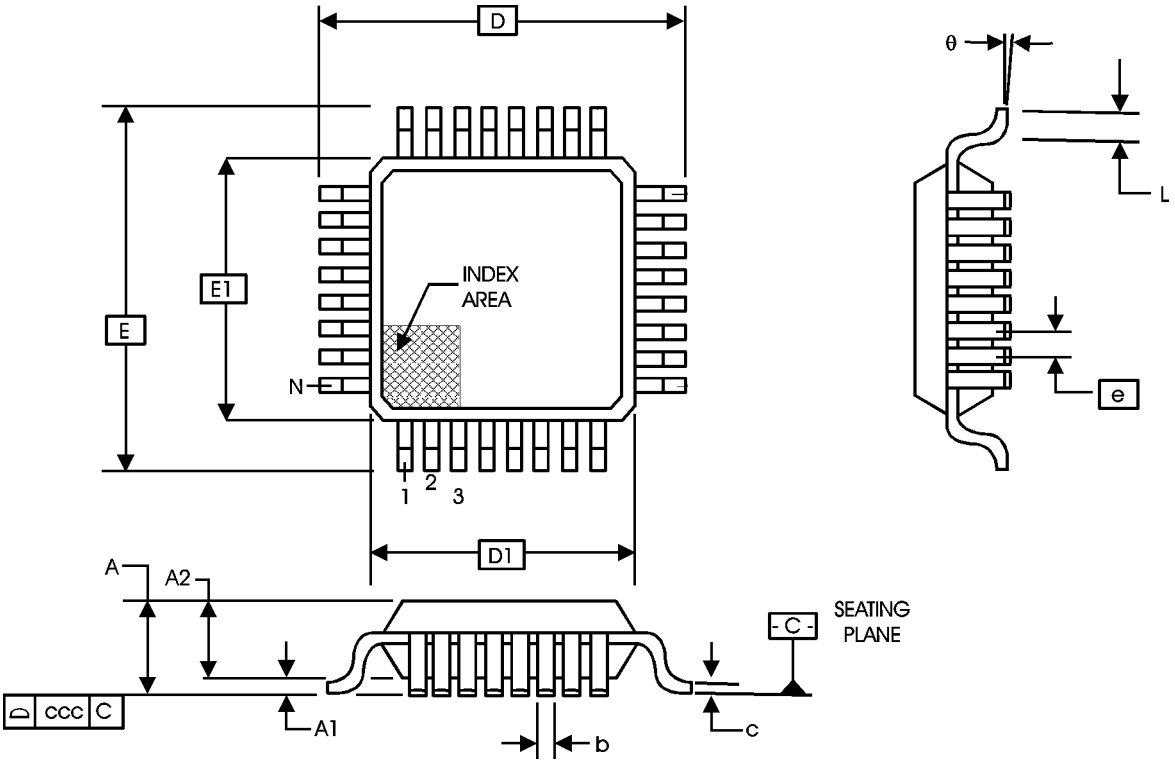


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCC		
	MINIMUM	NOMINAL	MAXIMUM
N		52	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
c	0.09	--	0.20
D		12.00 BASIC	
D1		10.00 BASIC	
E		12.00 BASIC	
E1		10.00 BASIC	
e		0.65 BASIC	
L	0.45	--	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87974AYI-01	ICS87974AYI-01	52 Lead LQFP	tray	-40°C to 70°C
87974AYI-01T	ICS87974AYI-01	52 Lead LQFP on Tape and Reel	500	-40°C to 70°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A		11	Added schematic layout.	11/13/03
A		2 & 3	Swichted labels for FB_SEL0 and FB_SEL1 in the Block Diagram and Simplified Block Diagram.	2/9/04
A	T8	14 16	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	8/10/10

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