National Semiconductor

54125/DM54125/DM74125 Quad TRI-STATE® Buffers

General Description

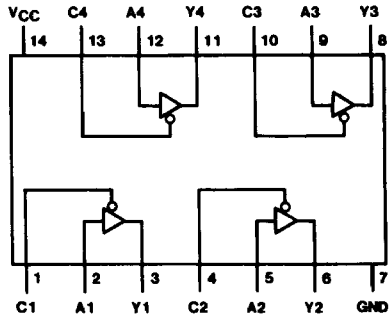
This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability at the high Logic level to permit the driving of bus lines without external pull-up resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Features

- Alternate Military/Aerospace device (54125) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6540–1

Order Number 54125DMQB, 54125FMQB, DM54125J, DM54125W or DM74125N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = A$

Inputs		Output
A	C	Y
L	L	L
H	L	H
X	H	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54125			DM74125			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{IZL}	Off-State Input Current with Low Level Input Voltage Applied	V_{CC} = Max, V_I = 0.4V				−40	μA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−30		−70	mA
			DM74	−28		−70	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			36	54	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the output control (C) inputs at 4.5V, the data inputs grounded, and the outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 400Ω				Units
		C_L = 5 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output				15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				18	ns
t_{PZH}	Output Enable Time to High Level Output				18	ns
t_{PZL}	Output Enable Time to Low Level Output				25	ns
t_{PHZ}	Output Disable Time from High Level Output		8			ns
t_{PLZ}	Output Disable Time from Low Level Output		14			ns