

Adjustable Precision Shunt Regulator

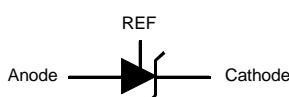
Features

- Precise Reference Voltage to 2.500V
- Guaranteed 0.5%, 1% or 2% Reference Voltage Tolerance
- Sink Current Capability, 1mA to 100mA
- Quick Turn-on
- Adjustable Output Voltage, $V_O = V_{REF}$ to 20V
- Low Operational Cathode Current, 250 μ A Typical
- 0.1 Ω Typical Output Impedance
- SOT-23, SOT-23-5, SOT-89, SOP-8, TO-92 and TO-92S Packages
- Lead Free and Green Devices Available (RoHS Compliant)

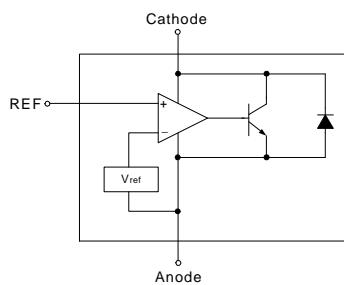
Applications

- Linear Regulators
- Adjustable Power Supply
- Switching Power Supply

Symbol



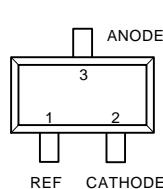
Functional Diagram



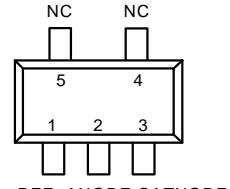
General Description

The APL431 is a 3-terminal adjustable voltage reference with specified thermal stability over applicable commercial temperature ranges. Output voltage may be set to any value between V_{REF} (2.5 V) and 20 V with two external resistors (See Figure 2). When used with an photocoupler, the APL431 is an ideal voltage reference in isolated feedback circuits for 2.5V to 12V switching-mode power supplies. This device has a typical output impedance of 0.1 Ω . Active output circuitry provides a very sharp turn-on characteristic, making the APL431 excellent replacements for zener diodes in many applications, including on-board regulation and adjustable power supplies.

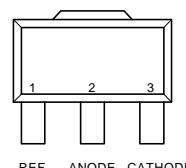
Pin Configuration



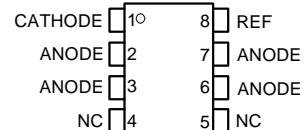
SOT-23 (Top View)



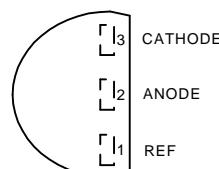
SOT-23-5 (Top View)



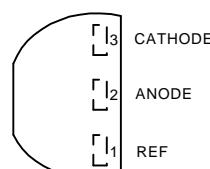
SOT-89 (Top View)



SOP-8 (Top View)



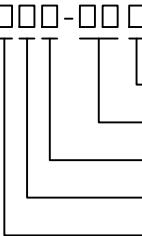
TO-92 (Top View)



TO-92S (Top View)

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APL431  Assembly Material Handling Code Temperature Range Package Code Elec. Grade	Elec. Grade A : 0.5% Reference Voltage Tolerance B : 1% Reference Voltage Tolerance C : 2% Reference Voltage Tolerance Package Code A : SOT-23 B : SOT-23-5 D : SOT-89 E : TO-92 I : TO-92S K : SOP-8 Y : Chip Form Temperature Range C : 0 to 70 °C I : -40 to 85 °C Q : -40 to 125 °C Handling Code TB : Tape & Box TR : Tape & Reel Assembly Material L : Lead Free Device G : Halogen and Lead Free Device
APL431 A/B : 431	APL431 E/I : 431 XXXXX XXXXX - Date Code
APL431 D/K : APL431 XXXXX XXXXX - Date Code	

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{KA}	Cathode Voltage	21	V
I_K	Continuous Cathode Current Range	100	mA
I_{REF}	Reference Current Range	3	mA
θ_{JA}	Thermal Resistance from Junction to Ambient in Free Air SOT-23 SOT-23-5 SOT-89 TO-92 SOP-8	416 357 250 250 210	°C/W
T_A	Ambient Temperature Range APL431XXC APL431XXI APL431XXQ	0 to 70 -40 to 85 -40 to 125	°C
T_J	Junction Temperature Range APL431XXC APL431XXI APL431XXQ	0 to 150 -40 to 150 -40 to 150	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C
T_{SOL}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Electrical Characteristics $T_A = 25^\circ\text{C}$ (unless otherwise noted)

Symbol	Parameter	Test Conditions	APL431			Unit
			Min.	Typ.	Max.	
V_{REF}	Reference Voltage	$V_{\text{KA}}=V_{\text{REF}}$, $I_K=10\text{mA}^{\ast 1}$	2.487	2.500	2.513	V
		$V_{\text{KA}}=V_{\text{REF}}$, $I_K=10\text{mA}^{\ast 1}$	2.475	2.500	2.525	
		$V_{\text{KA}}=V_{\text{REF}}$, $I_K=10\text{mA}^{\ast 1}$	2.450	2.500	2.550	
$\Delta V_{\text{REF}} / T$	Reference Voltage Drift Over Temperature Range	$V_{\text{KA}}=V_{\text{REF}}, I_K=10\text{mA}$ $T_A = 0 \text{ to } 70^\circ\text{C}^{\ast 1}$ $T_A = -40 \text{ to } 85^\circ\text{C}^{\ast 1}$ $T_A = -40 \text{ to } 125^\circ\text{C}^{\ast 1}$			20 30 35	mV
$\Delta V_{\text{REF}} / \Delta V_{\text{KA}}$	Voltage Ratio (Open Loop Gain)	$I_K=10\text{mA}, V_{\text{KA}}=V_{\text{REF}} \text{ to } 10\text{V}^{\ast 2}$		-1.5	-3	mV/V
		$I_K=10\text{mA}, V_{\text{KA}}=V_{\text{REF}} \text{ to } 20\text{V}^{\ast 2}$		-1.2	-2.5	
I_{REF}	Reference Current	$I_K=10\text{mA}$, $R_1=10\text{k}\Omega$, $R_2=\text{open}^{\ast 2}$		1.0	3	μA
$\Delta I_{\text{REF}}/T$	Reference Current Drift	$I_K=10\text{mA}$, $R_1=10\text{k}\Omega$, $R_2=\text{open}$, $T_A = -40 \text{ to } 85^\circ\text{C}^{\ast 2}$		0.3	1	μA
$I_{K(\min)}$	Min. Cathode Current	$V_{\text{KA}}=V_{\text{REF}}^{\ast 1}$		0.25	0.5	mA
$I_{K(\text{off})}$	Off-state Cathode Current	$V_{\text{KA}}=20\text{V}$, $V_{\text{REF}}=0\text{V}^{\ast 3}$		0.1	1	μA
$ Z_{\text{KA}} $	Dynamic Impedance	$V_{\text{KA}}=V_{\text{REF}}$ $I_K=1\text{mA} \text{ to } 100\text{mA}$, $f \leq 1\text{kHz}^{\ast 1}$		0.1	0.4	Ω
I_K	Cathode Current				100	mA

Notes : *1 : use Figure 1

*2 : use Figure 2

*3 : use Figure 3

Test figures

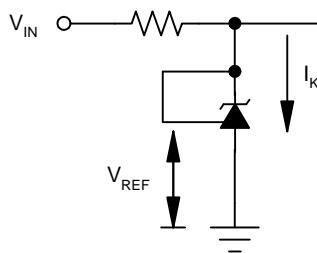


Figure 1. Test Circuit for $V_{\text{KA}}=V_{\text{REF}}$, $V_O=V_{\text{KA}}=V_{\text{REF}}$

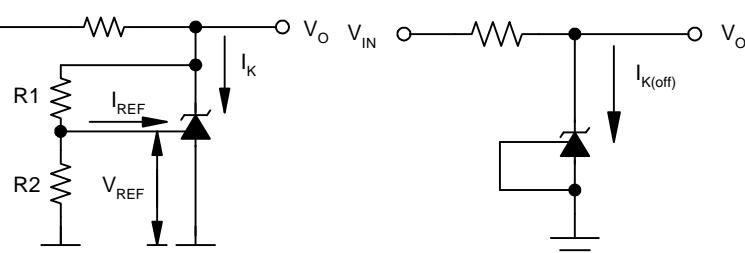


Figure 2. Test Circuit for $V_{\text{KA}}>V_{\text{REF}}$,
 $V_O=V_{\text{KA}}=V_{\text{REF}} \times (1+R_1/R_2) + I_{\text{REF}} \times R_1$

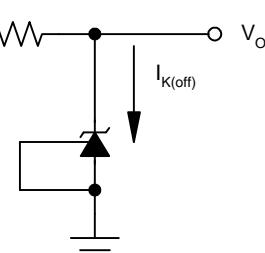
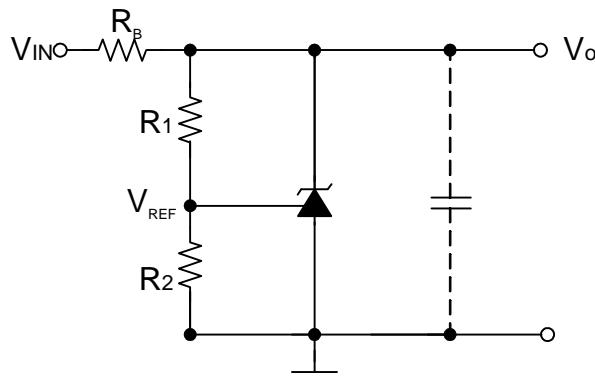
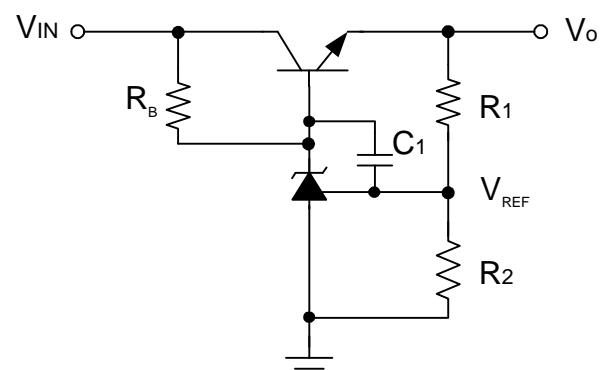


Figure 3. Test Circuit for $I_{\text{K}(\text{off})}$

Application Circuits



Precision Voltage Reference

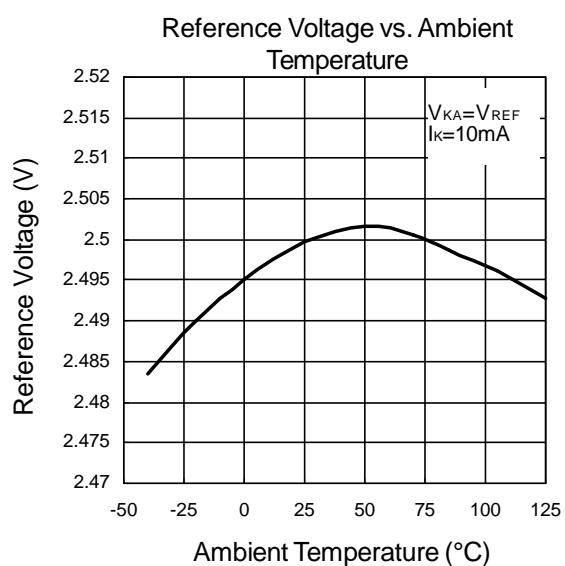
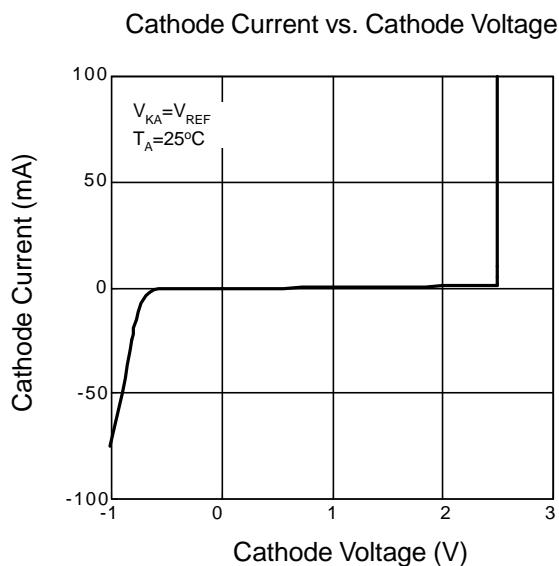
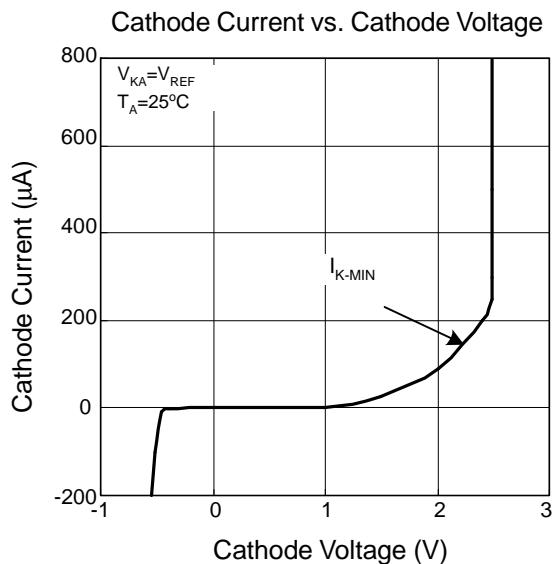
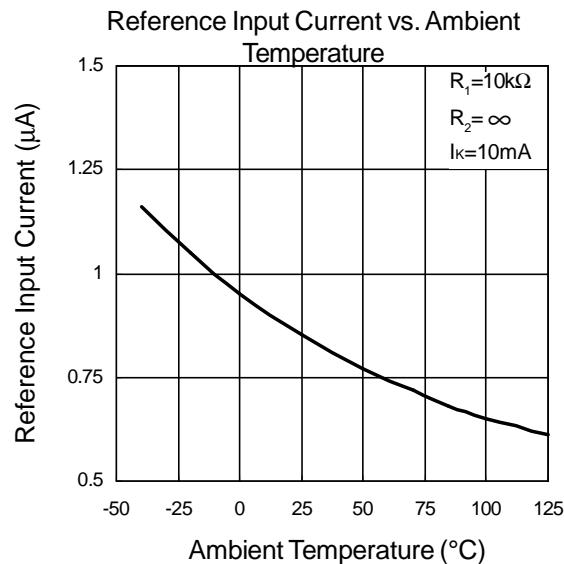


Precision High-Current Series Regulator

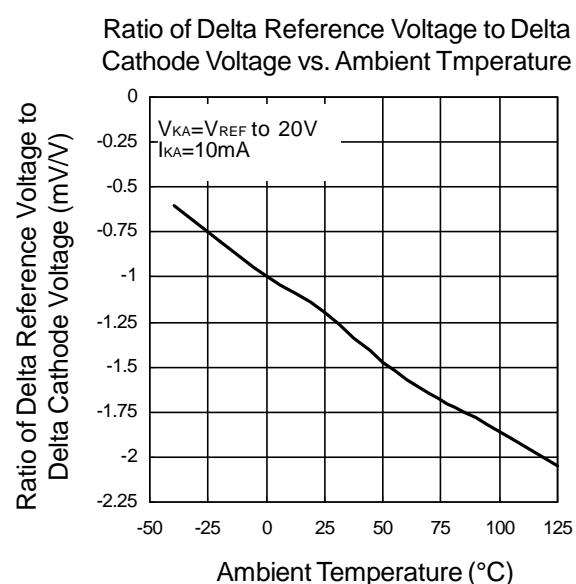
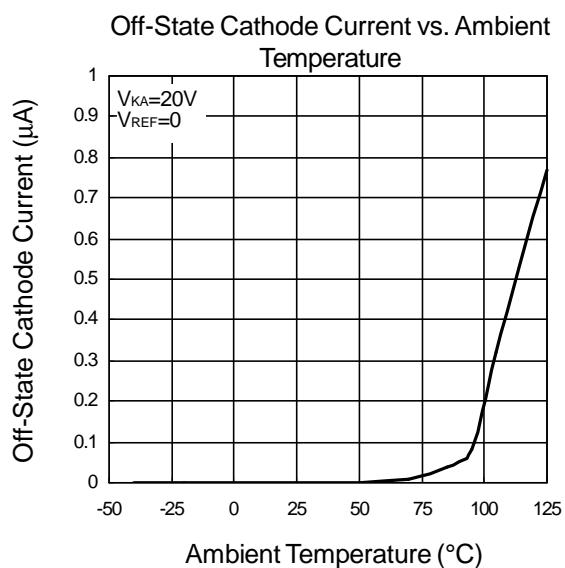
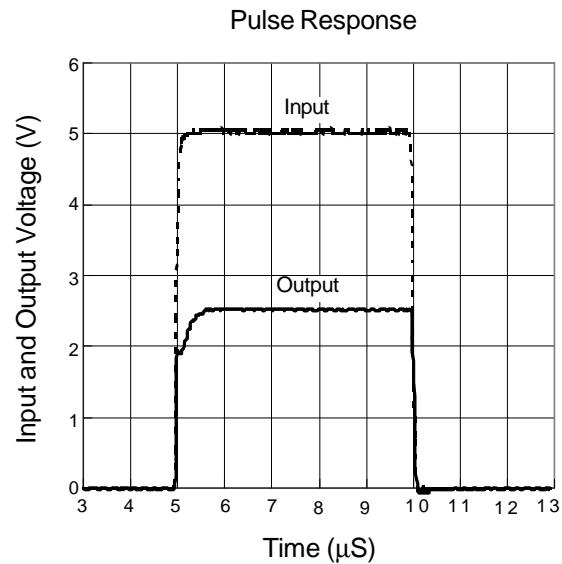
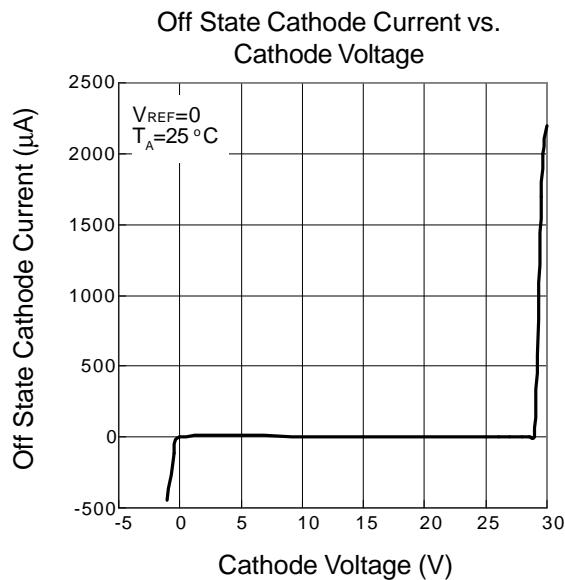
Notes for Application Circuits:

- 1) For the series regulator applications, add a compensation capacitor C_1 between CATHODE and REF is strongly recommended to improve the stability of output voltage .
- 2) Set V_o according to the following equation: $V_o = V_{REF}(1+R1/R2)+I_{REF} \times R1$
- 3) Choose the value for R_B as follows:
 - A) The maximum limit for R_B should be such that the cathode current (I_K) is greater than the minimum operating current (0.5mA) at $V_{IN(MIN)}$.
 - B) The minimum limit for R_B should be such that the cathode current (I_K) does not exceed 100mA under all load conditions, and the instantaneous turn-on value for I_K does not exceed 120mA.

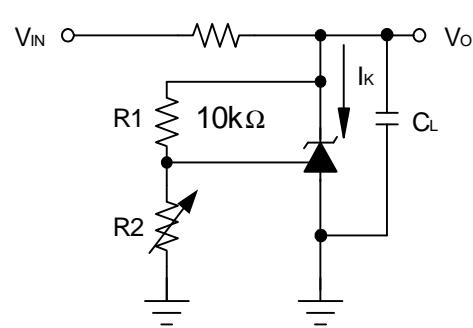
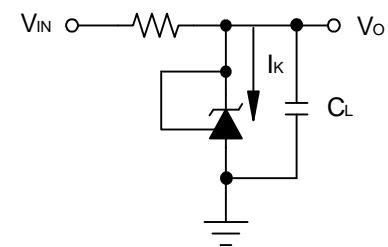
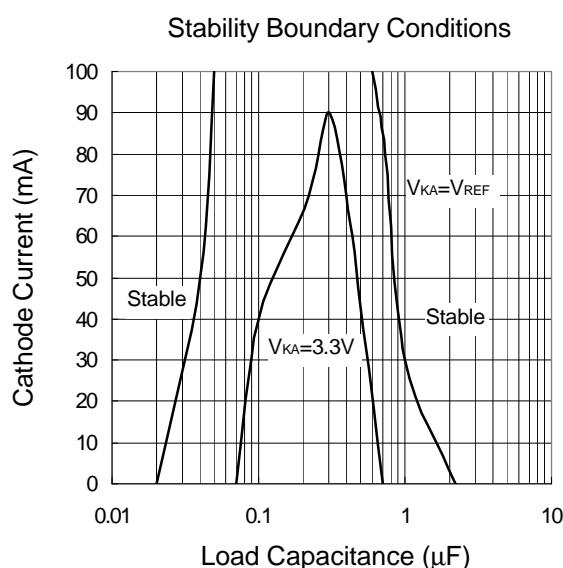
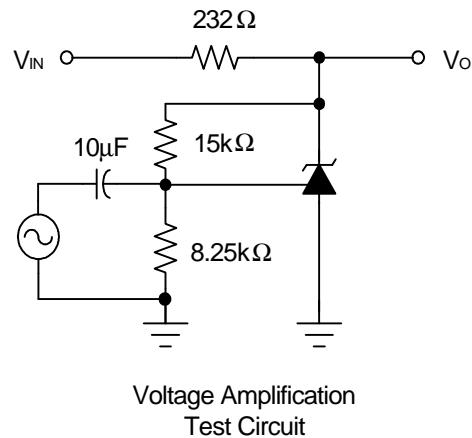
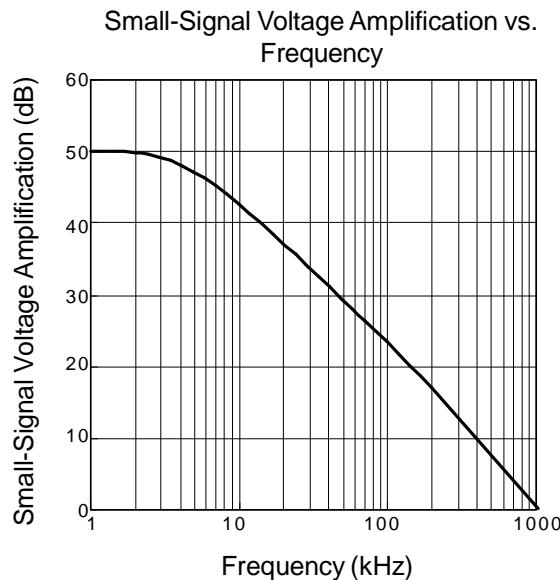
Typical Characteristics



Typical Characteristics (Cont.)

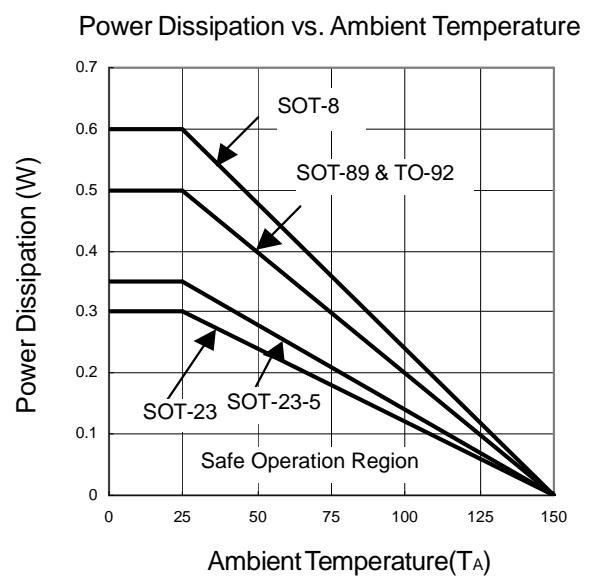
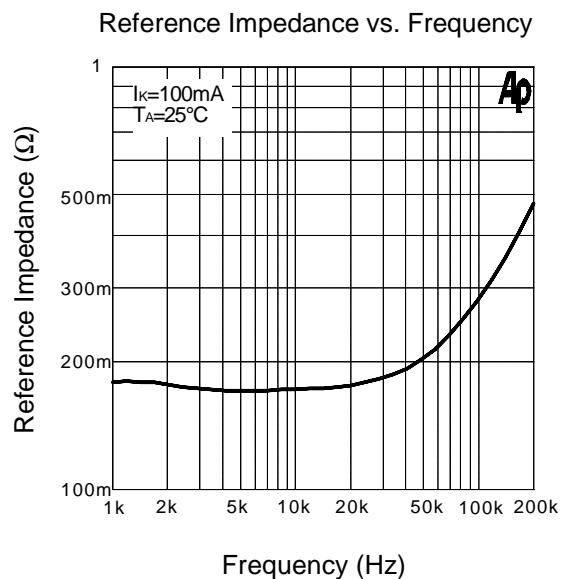


Typical Characteristics (Cont.)



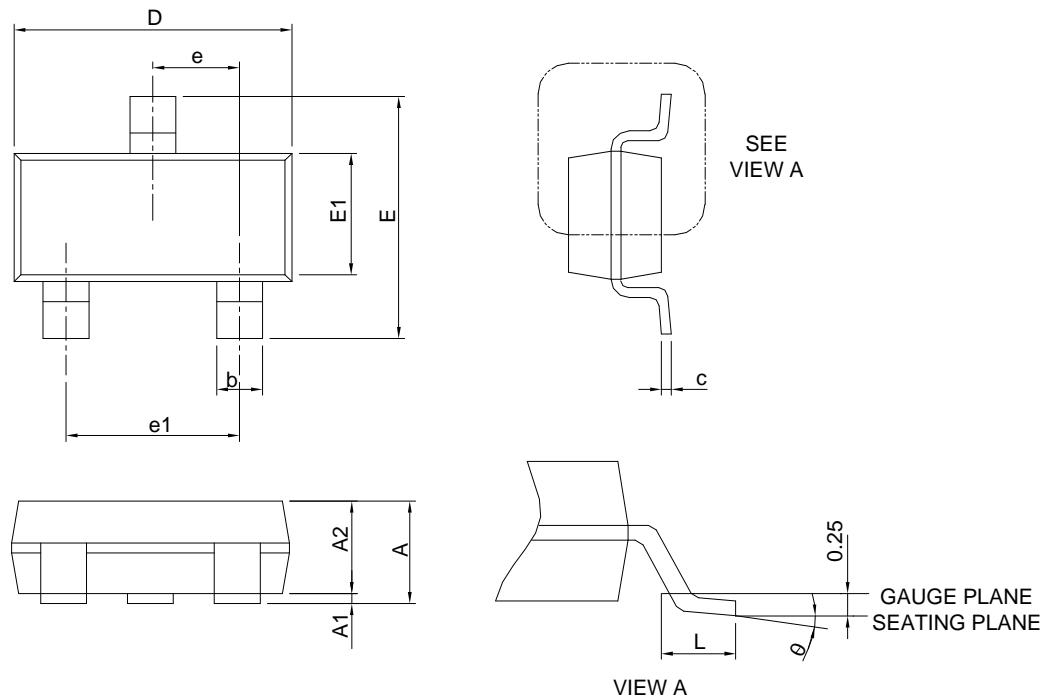
Stability Test Circuit for $V_{KA} > V_{REF}$,
 $V_o = V_{KA} = V_{REF} \times (1 + R_1/R_2) + I_{REF} \times R_1$
 Use the MLCC for C_L

Typical Characteristics (Cont.)



Package Information

SOT-23-3

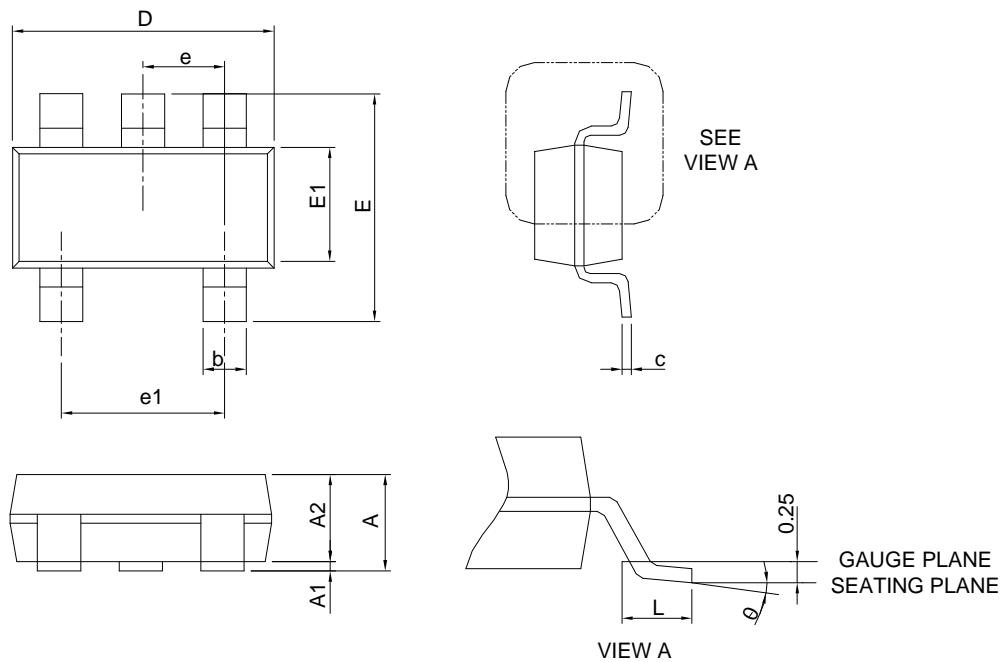


SYMBOL	SOT-23			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Package Information

SOT-23-5

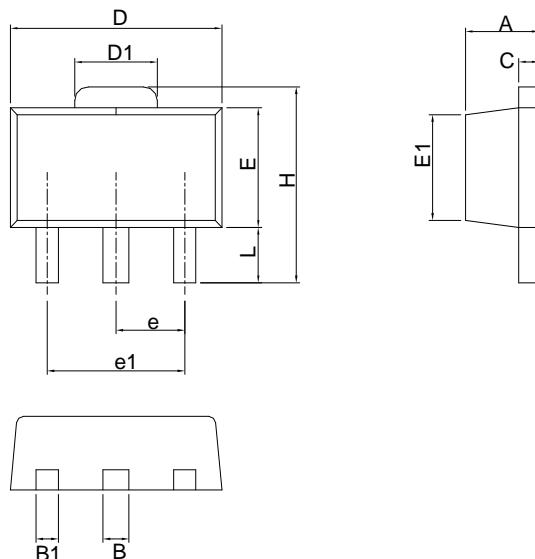


S Y M B O R	SOT-23-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.016	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

- Note : 1. Follow JEDEC TO-178 AA.
 2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Package Information

SOT-89

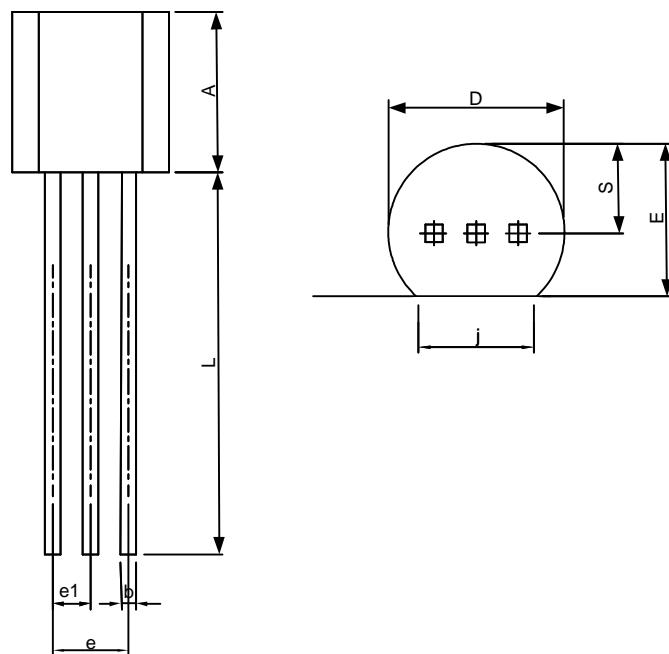


SYMBOL	SOT-89			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.40	1.60	0.055	0.063
B	0.44	0.56	0.017	0.022
B1	0.36	0.48	0.014	0.019
C	0.35	0.44	0.014	0.017
D	4.40	4.60	0.173	0.181
D1	1.62	1.83	0.064	0.072
E	2.29	2.60	0.090	0.102
E1	2.13	2.29	0.084	0.090
e	1.50 BSC		0.059 BSC	
e1	3.00 BSC		0.118 BSC	
H	3.94	4.25	0.155	0.167
L	0.89	1.20	0.035	0.047

Note : Follow JEDEC TO-243 AA.

Package Information

TO-92

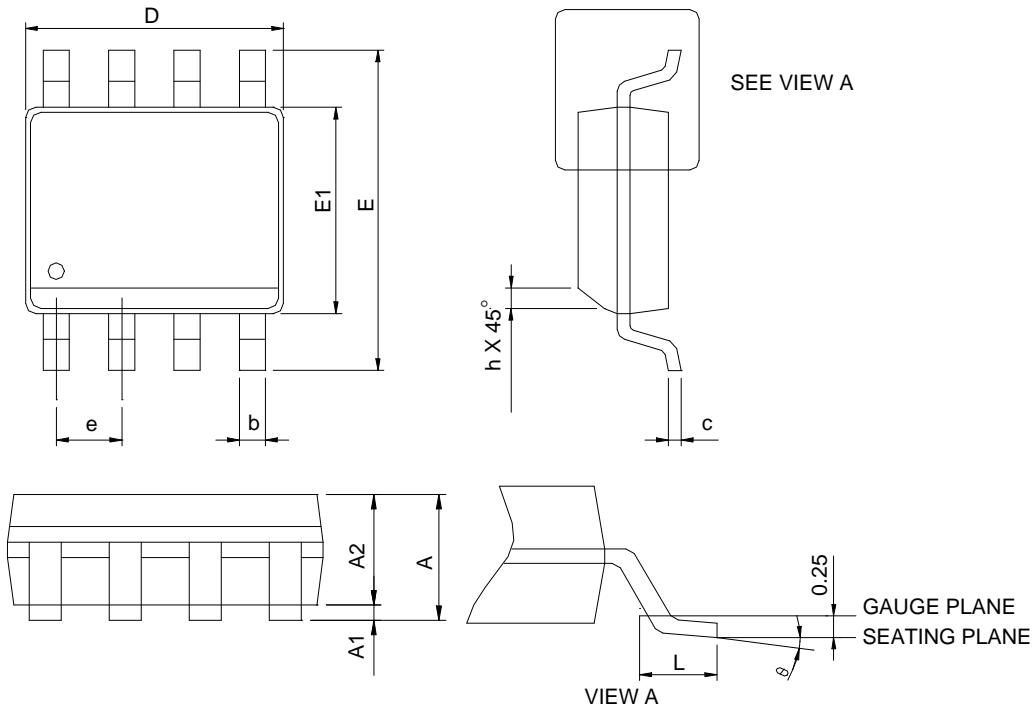


SYMBOL	TO-92			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.32	5.33	0.170	0.210
b	0.41	0.53	0.016	0.021
D	4.45	5.20	0.175	0.205
E	3.18	4.19	0.125	0.165
e	2.42	2.66	0.095	0.105
e1	1.15	1.39	0.045	0.055
j	3.43	4.00	0.135	0.157
L	12.70	15.00	0.500	0.591
S	2.03	2.66	0.080	0.105

Note : Follow JEDEC TO-92.

Package Information

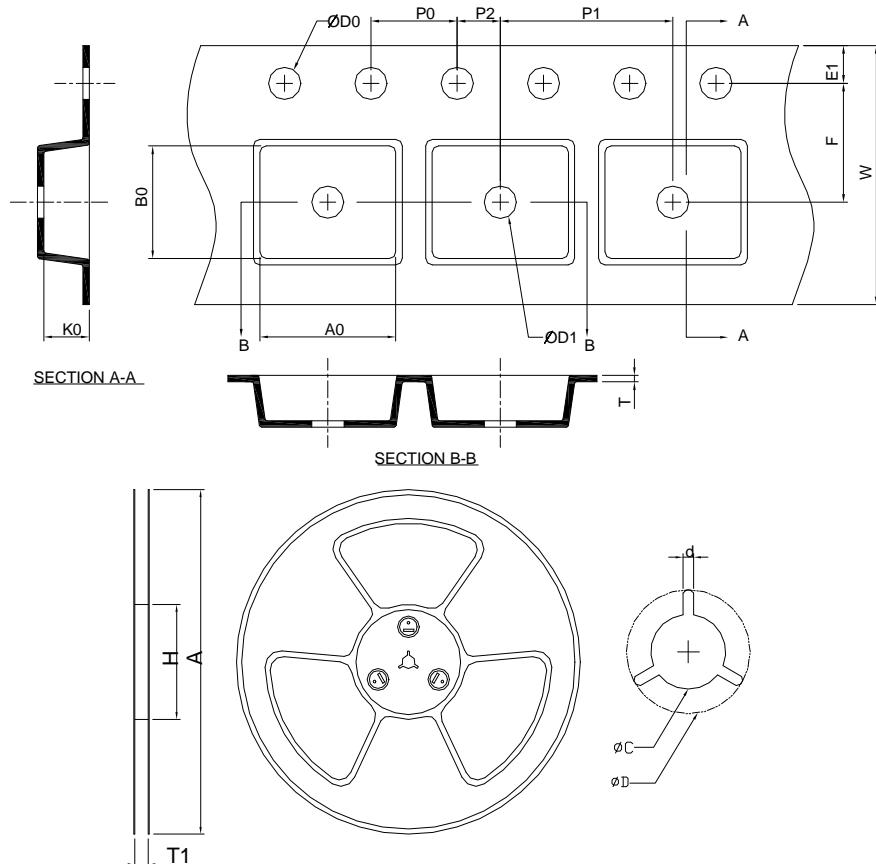
SOP-8



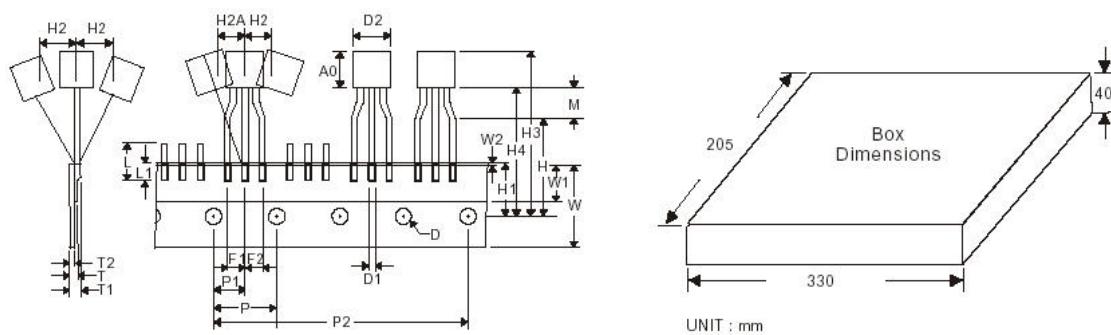
SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

- Note:
- Follow JEDEC MS-012 AA.
 - Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
 - Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Carrier Tape & Box Dimensions



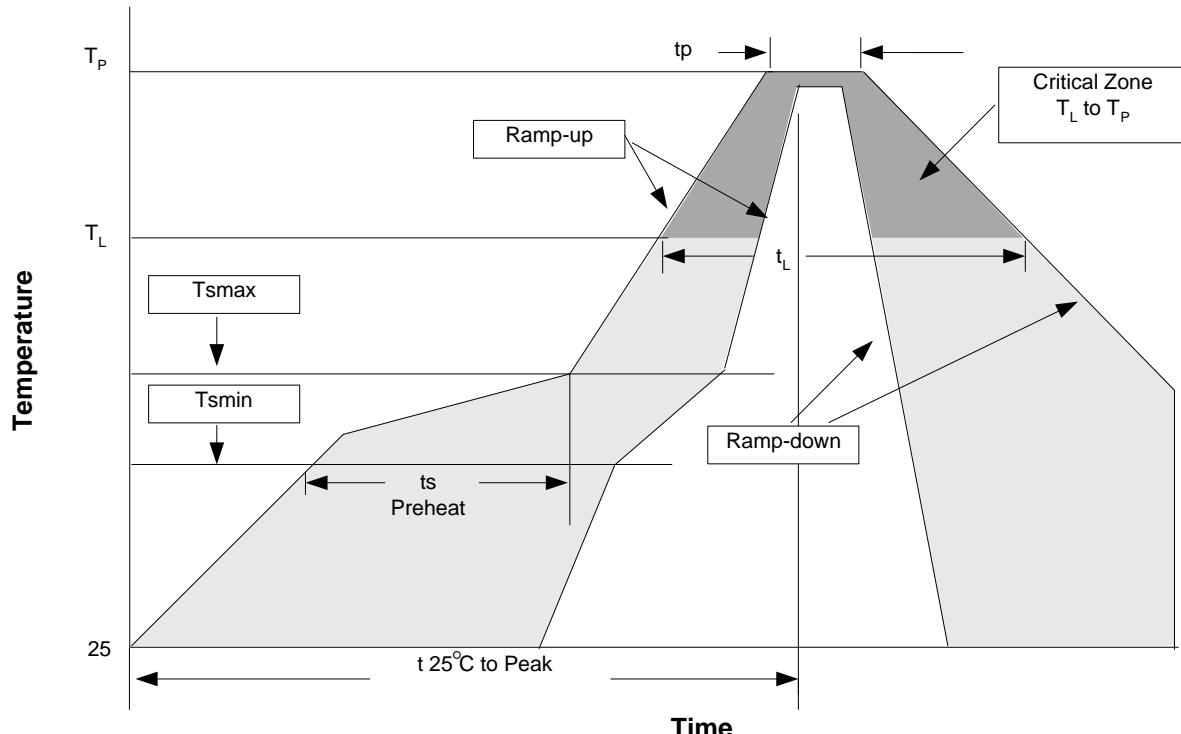
Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0 ±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40 ±0.20	5.20 ±0.20	2.10 ±0.20
Application	A	H	T1	C	d	D	W	E1	F
SOT-23	178.0 ±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0 ±0.30	1.75 ±0.10	3.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	4.0 ±0.10	2.0 ±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.20 ±0.20	3.10 ±0.20	1.50 ±0.20
Application	A	H	T1	C	d	D	W	E1	F
SOT-23-5	178.0 ±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0 ±0.30	1.75 ±0.10	3.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	4.0 ±0.10	2.0 ±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.20 ±0.20	3.10 ±0.20	1.50 ±0.20
Application	A	H	T1	C	d	D	W	E1	F
SOT-89	178.0 ±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.50 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.80 ±0.20	4.50 ±0.20	1.80 ±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
SOT-23-3	Tape & Reel	3000
SOT-89	Tape & Reel	1000
TO-92	Tape & Box	2000
SOT-23-5	Tape & Reel	3000
SOP-8	Tape & Reel	2500

Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, I_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat	<ul style="list-style-type: none"> - Temperature Min (T_{Smin}) - Temperature Max (T_{Smax}) - Time (min to max) (t_s) 	<ul style="list-style-type: none"> 100°C 150°C 60-120 seconds 150°C 200°C 60-180 seconds
Time maintained above:	<ul style="list-style-type: none"> - Temperature (T_L) - Time (t_L) 	<ul style="list-style-type: none"> 183°C 60-150 seconds 217°C 60-150 seconds
Peak/Classification Temperature (T_p)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (t_p)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

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