TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHCT245F, TC74VHCT245FW, TC74VHCT245FS

OCTAL BUS TRANSCEIVER

The TC74VHCT245 is an advanced high speed CMOS OCTAL BUS TRANSCEIVER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It is intended for two - way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

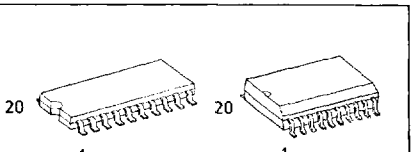
The input voltage are compatible with TTL output voltage.

This device may be used as a level converter for interfacing 3.3V to 5V system.

Input protection and output circuit ensure that 0 to 7V can be applied to the input and output pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input / output voltages such as battery back up, hot board insertion, etc.

FEATURES :

- High Speed ..... t_{pd} = 4.9ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Compatible with TTL outputs ··· V_{IL} = 0.8V (Max.)
  V_{IH} = 2.0V (Min.)
- Power Down Protection is provided on all inputs and outputs
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Low Noise ····· V_{OLP} = 1.6V (Max.)
- Pin and Function Compatible with 74ALS245



F (SOP20-P-300-1.27) FW (SOL20-P-300-1.27)
Weight : 0.22g (TYP.) Weight : 0.46g (TYP.)

FS (SSOP20-P-225-0.65A)
Weight : 0.09g (TYP.)

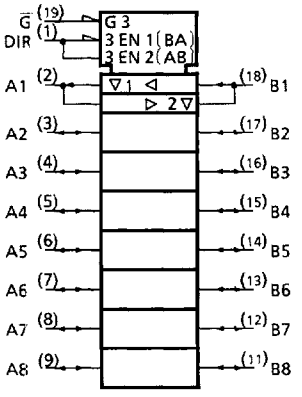
APPLICATION NOTES

This device can drive the components with CMOS input level by adding a external pull up resistor to output terminal.

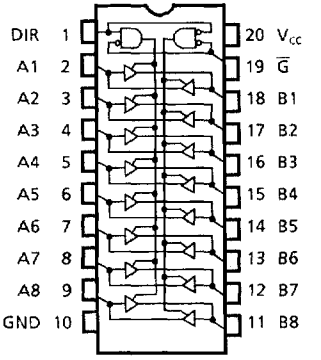
Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

IEC LOGIC SYMBOL



PIN ASSIGNMENT



(TOP VIEW)

961001EBA2

TRUTH TABLE

INPUTS		FUNCTION		OUTPUT
$\overline{G}$	DIR	A BUS	B BUS	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	High Impedance		Z

X : Don't Care
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage (DIR,$\overline{G}$)	V_{IN}	−0.5~7.0	V
DC I/O Voltage	$V_{I/O}$	−0.5~7.0	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	−20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage (DIR,$\overline{G}$)	V_{IN}	0~5.5	V
Output Voltage	$V_{I/O}$	0~5.5	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dV	0~20	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITON		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			4.5~5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			4.5~5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	4.5	3.15	3.65	—	3.15	—	V
			I_{OH} = −8mA	4.5	2.50	—	—	2.40	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5	—	0.0	0.10	—	0.10	V
			I_{OL} = 8mA	4.5	—	—	0.36	—	0.44	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	—	±2.50	μA
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	
	I_{CCT}	PER INPUT : V_{IN} = 3.4V OTHER INPUT : V_{CC} or GND		5.5	—	—	1.35	—	1.50	mA
Output Leakage Current	I_{OPD}	V_{OUT} = 5.5V		0	—	—	+0.5	—	+5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		5.0 ± 0.5	15	—	4.9	7.7	1.0	8.5	ns
				50	—	5.4	8.7	1.0	9.5	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L = 1kΩ	5.0 ± 0.5	15	—	9.4	13.8	1.0	15.0	
				50	—	9.9	14.8	1.0	16.0	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L = 1kΩ	5.0 ± 0.5	50	—	10.1	15.4	1.0	16.5	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input Capacitance	C_{IN}	DIR, $\overline{G}$			—	4	10	—	10	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn			—	13	—	—	—	
Power Dissipation Capacitance	C_{PD}	(Note 2)			—	16	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

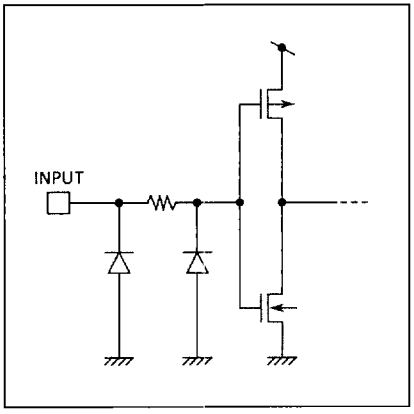
Note (2) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per bit)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	C_L = 50pF	5.0	1.2	1.6	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	C_L = 50pF	5.0	−1.2	−1.6	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	C_L = 50pF	5.0	−	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	C_L = 50pF	5.0	−	0.8	V

INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT