IOR INTERNATIONAL RECTIFIER

Data Sheet No. PD-3.127

T-25-19

S23D SERIES
2000-1400 VOLTS RANGE
285 AMP RMS, RING AMPLIFYING GATE
PHASE CONTROL TYPE STUD MOUNTED SCRs

VOLTAGE RATINGS

VOLTAGE CODE (1)	V_{RRM}, V_{DRM} – (V) Max. rep. peak reverse and off-state voltage		V_{RSM} – (V) Max. non-rep. peak reverse voltage $t_p \leq 5ms$	NOTES
	T_J = 0° to 125°C	T_J = -40° to 0°C	T_J = 25° to 125°C	
20A	2000	1900	2100	Gate open
18A	1800	1710	1900	
16B	1600	1520	1700	
14B	1400	1330	1500	

(1) To complete the part number, refer to the Ordering Information table.

MAXIMUM ALLOWABLE RATINGS

PARAMETER		VALUE	UNITS	NOTES
T_J	Junction temperature	-40 to 125	°C	
T_{stg}	Storage temperature	-40 to 150	°C	
$I_{T(AV)}$	Max. av. current	180	A	180° half sine wave
	@ Max. T_C	85	°C	
$I_{T(RMS)}$	Max. RMS current	285	A	
I_{TSM}	Max. peak non-rep. surge current	4800	A	50Hz half cycle sine wave — Initial T_J = 125°C, rated V_{RRM} applied after surge.
		4800		60Hz half cycle sine wave
		5450		50Hz half cycle sine wave — Initial T_J = 125°C, no voltage applied after surge.
		5700		60Hz half cycle sine wave
I^2t	Max. I^2t capability	105	kA^2s	t = 10ms — Initial T_J = 125°C, rated V_{RRM} applied after surge.
		96		t = 8.3ms
		149		t = 10ms — Initial T_J = 125°C, no voltage applied after surge.
		136		t = 8.3ms
$I^2\sqrt{t}$	Max. $I^2\sqrt{t}$ capability	1490	$kA^2\sqrt{s}$	Initial T_J = 125°C, no voltage applied after surge. I^2t for time $t_x = I^2\sqrt{t} \cdot \sqrt{t_x}$. $0.1 \leq t_x \leq 10ms$.
di/dt	Max. non-rep. rate-of-rise of current	800	A/µs	T_J = 125°C, $V_D = V_{DRM}$, I_{TM} = 1600A. Gate pulse: 20V, 20Ω, 10µs, 0.5µs rise. Max. repetitive di/dt is approximately 40% of non-repetitive value.
P_{GM}	Max. peak gate power	10	W	$t_p \leq 5ms$
$P_{G(AV)}$	Max. av. gate power	2	W	
$+I_{GM}$	Max. peak gate current	3	A	$t_p \leq 5ms$
$-V_{GM}$	Max. peak neg. gate voltage	5	V	
T	Mounting torque	31 [275] ± 10%	N•m	Non-lubricated threads.
		24.5 [210] ± 10%	(lbf-in)	S23DP... type only. Lubricated threads.

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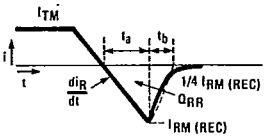
CHARACTERISTICS

PARAMETER		MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{TM}	Peak on-state voltage	—	1.40	1.53	V	Initial T_J = 25°C, 60Hz half sine, I_{peak} = 566A.
$V_{T(TO)1}$	Low-level threshold	—	—	0.831	V	T_J = 125°C. Av. power = $V_{T(TO)} * I_{T(AV)} + r_T * (I_{T(RMS)})^2$ Use low level values for $I_{TM} \leq \pi I_{T(AV)}$
$V_{T(TO)2}$	High-level threshold	—	—	0.898		
r_{T1}	Low-level resistance	—	—	1.260	mΩ	
r_{T2}	High-level resistance	—	—	1.160		
I_L	Latching current	—	200	—	mA	T_C = 25°C, 12V anode. Gate pulse: 10V, 20Ω, 100µs.
I_H	Holding current	—	70	500	mA	T_C = 25°C, 12V anode. Initial I_T = 5A.
t_d	Delay time	—	0.6	1.5	µs	T_C = 25°C, V_D = V_{DRM}, 50A resistive load. Gate pulse: 10V, 20Ω, 10µs, 1µs rise.
t_q	Turn-off time	—	120	—	µs	T_J = 125°C. I_{TM} = 300A, di_R/dt = 15A/µs, V_R = 50V, dv/dt = 20V/µs lin. to rated V_{DRM}. Gate: 0V, 100Ω.
t_a	Reverse current rise	—	14	—	µs	T_J = 125°C, I_{TM} = 300A, di_R/dt = 1.5A/µs 
t_b	Reverse current fall	—	3.6	—	µs	
$I_{RM(REC)}$	Reverse current	—	21	—	A	
Q_{RR}	Recovered charge	—	185	—	µC	
dv/dt	Critical rate-of-rise of voltage	500	700	—	V/µs	T_J = 125°C. Exp. to 100% or lin. to 80% V_{DRM}, gate open. Higher dv/dt values available.
		1000	—	—		T_J = 125°C. Exp. to 67% V_{DRM}, gate open.
I_{RM}, I_{DM}	Peak reverse and off-state current	—	15	30	mA	T_J = 125°C. Rated V_{RRM} and V_{DRM}, gate open.
I_{GT}	DC gate current to trigger	—	—	300	mA	T_C = -40°C +12V anode. For recommended gate drive see "Gate Characteristics" figure.
		40	60	150		T_C = 25°C
V_{GT}	DC gate voltage to trigger	—	—	3.3	V	T_C = -40°C
		—	1.2	2.5		T_C = 25°C
V_{GD}	DC gate voltage not to trigger	—	—	0.3	V	T_C = 125°C. Max. value which will not trigger with rated V_{DRM} anode.
R_{thJC}	Thermal resistance, junction-to-case	—	—	0.140	°C/W	DC operation
		—	—	0.160	°C/W	180° sine wave
		—	—	0.164	°C/W	120° rectangular wave
R_{thCS}	Thermal resistance, case-to-sink	—	—	0.080	°C/W	Mounting surface smooth, flat and greased.
wt	Weight	—	227(8)	—	g(oz.)	
	Case Style		TO-209AB (TO-93)		JEDEC	

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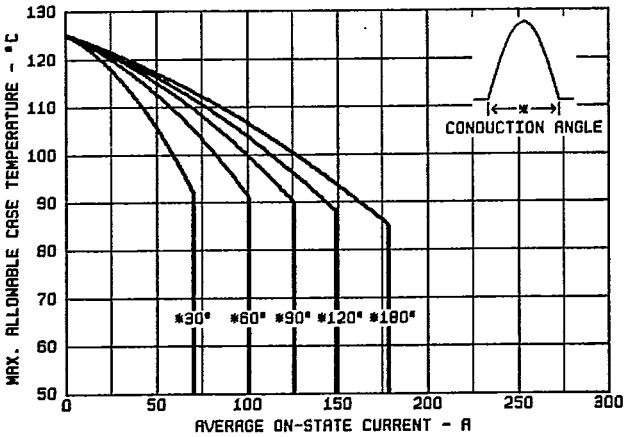

Fig. 1 — Case Temperature Ratings — Sinusoidal Waveforms, 50 to 400 Hz

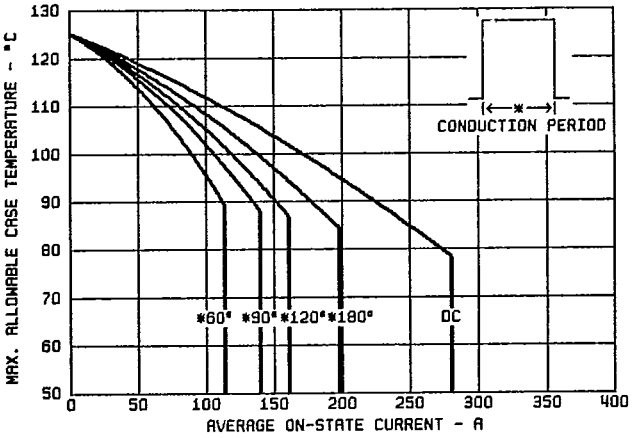

Fig. 2 — Case Temperature Ratings — Rectangular Waveforms, 50 to 400 Hz

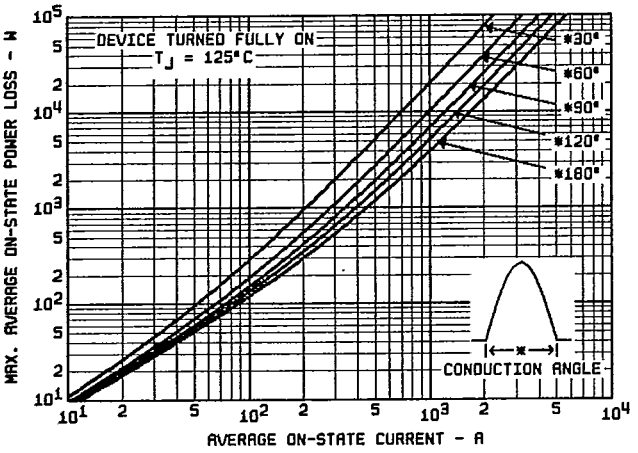

Fig. 3 — Power Loss Characteristics — Sinusoidal Waveforms

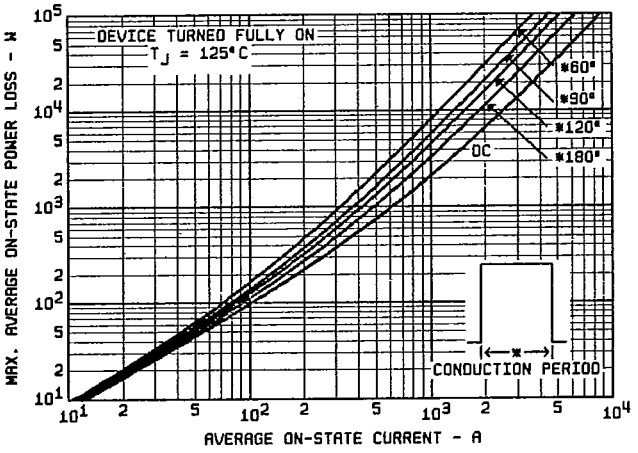

Fig. 4 — Power Loss Characteristics — Rectangular Waveforms

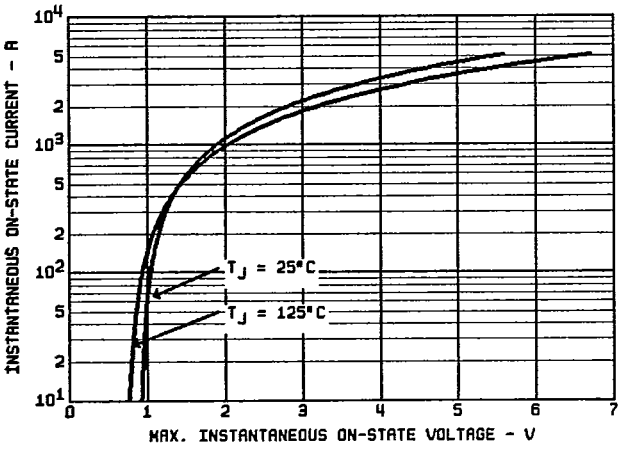

Fig. 5 — On-State Characteristics

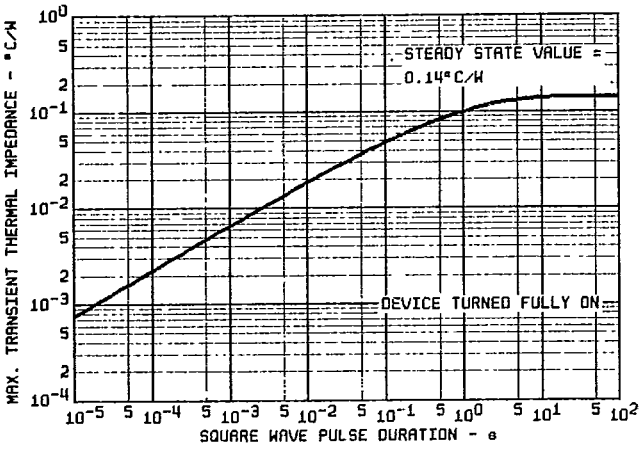

Fig. 6 — Transient Thermal Impedance, Junction-to-Case

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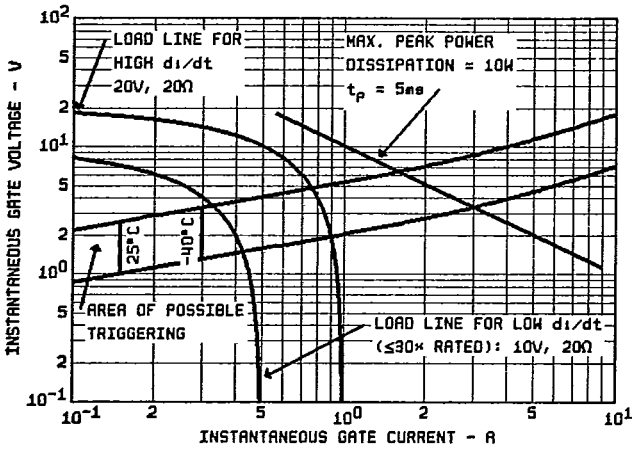

Fig. 7 — Gate Characteristics

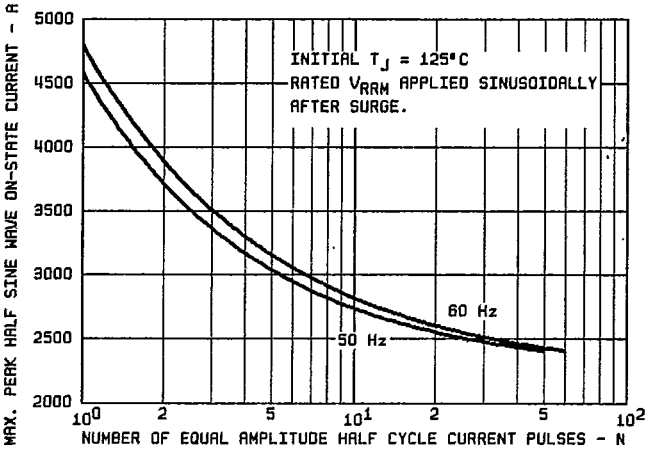

Fig. 8 — Non-Repetitive Surge Current Ratings

ORDERING INFORMATION

TYPE	PACKAGE (1)		TEMPERATURE		VOLTAGE		LEADS & TERMINALS		BASE MODIFICATION (2)	
	CODE	DESCRIPTION	CODE	MAX. T_J	CODE	V_{DRM}	CODE	DESCRIPTION	CODE	DESCRIPTION
S23	D	3/4" stud, ceramic housing. Standard in USA. (Fig. 1)	—	125°C	20A	2000V	0	Flexible leads, eyelet terminals. Standard in USA. (Fig. 1)	M	Metric threads.
					18A	1800V				
					16B	1600V				
	DP	3/4" stud, compression bonded, ceramic housing. Standard in Europe. (Fig. 2)			14B	1400V	1	Flexible leads, fast-on terminals. Standard in Europe. (Fig. 2)		

(1) Other packages are also available:
- flat base, similar to TO-209AB (TO-93) with stud removed.
For futher details See Alternative Case Style Section.

(2) Use only if required

For example, for a device with standard USA case, max. T_J = 125°C, V_{DRM} = 1800V, order as:

TYPE	PACKAGE	TEMPERATURE	VOLTAGE	LEADS & TERMINALS
S23	D	--	18A	0

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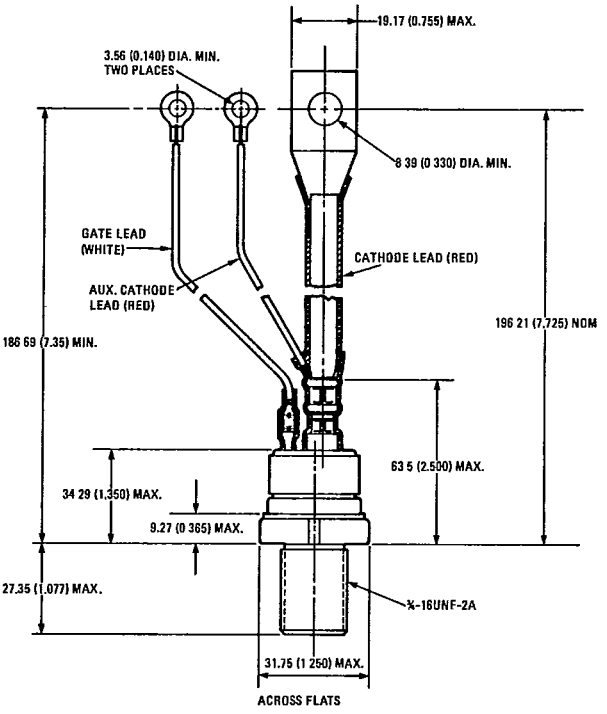

Fig. 1 — Conforms to JEDEC Outline TO-209AB (TO-93)

Dimensions in Millimeters and (Inches)

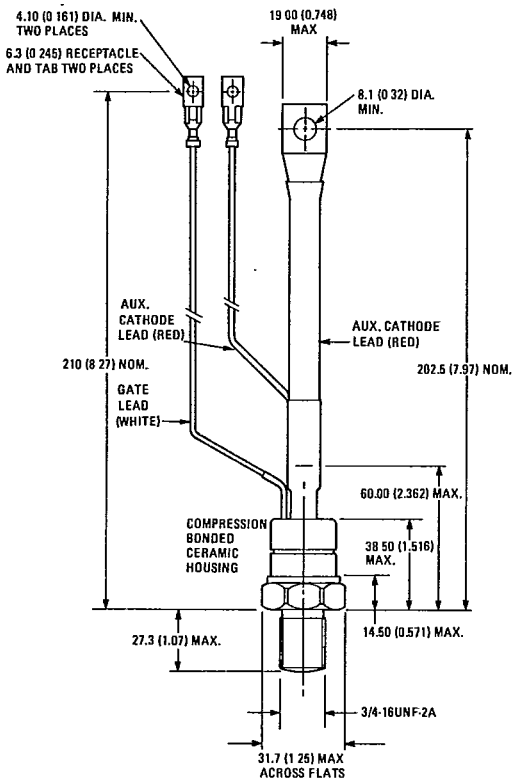

Fig. 2 — Similar to JEDEC Outline TO-209AB (TO-93)

Dimensions in Millimeters and (Inches)