8-Bit addressable latch — 54F259

FEATURES

- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common Clear input
- Useful as a 1-of-8 active High decoder

DESCRIPTION

The 54F259 addressable latch has four distinct modes of operation that are selectable by controlling the Master Reset and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the store mode, all latches remain in their previous states and are unaffected by the Data or Address inputs.

To eliminate the possibility of entering erroneous data in the latches, the enable should be held High (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode ($\overline{MR}$ = $\overline{E}$ = Low), addressed outputs will follow the level of the D inputs, with all other outputs Low. In the Master Reset mode, all outputs are Low and unaffected by the Address and Data inputs.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
16-Pin Ceramic DIP	54F259/BEA	GDIP1-T16
16-Pin Ceramic Flat Pack	54F259/BFA	GDFP2-F16
20-Pin Ceramic LLCC	54F259/B2A	CQCC2-N20

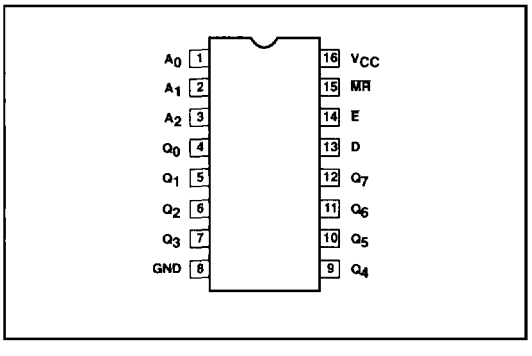
* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

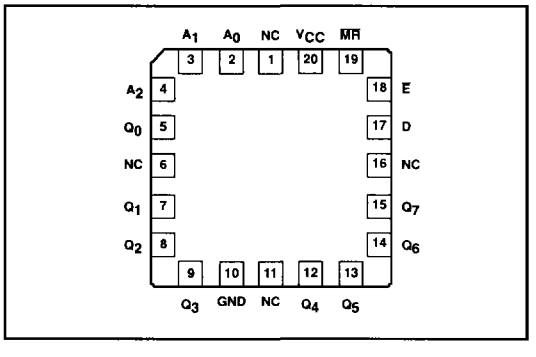
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{MR}$, $\overline{E}$	Master reset, enable inputs	1.0/1.0	20μA/0.6mA
A_0, A_2	Address Inputs	1.0/1.0	20μA/0.6mA
D	Data input	1.0/1.0	20μA/0.6mA
Q_0 - Q_7	Outputs	50/33	1mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

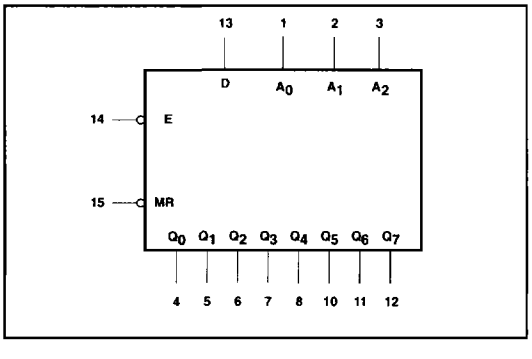
PIN CONFIGURATION



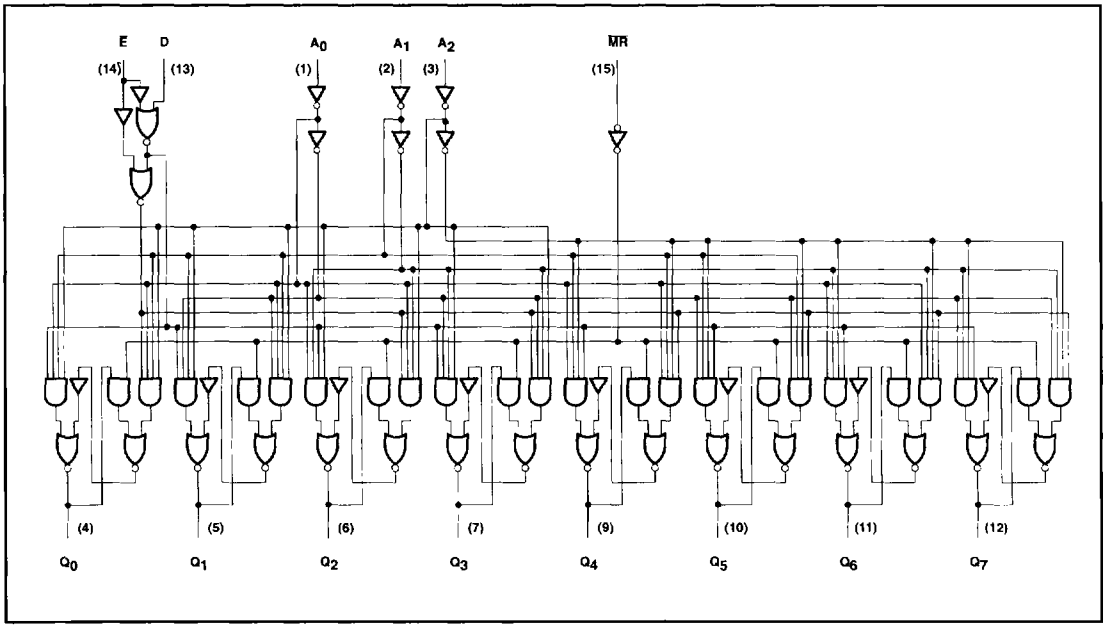
LLCC LEAD CONFIGURATION



LOGIC SYMBOL



LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS							
	$\overline{MR}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Master Reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplexer (active High decoder when D = H	L	L	d	L	L		Q = d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q = d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q = d	L	L	L	L	L
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	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	L	L	d	H	H	L	L	L	L	L	L	L	L	Q = d
Store (do nothing)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
Addressable latch	H	L	d	L	L	L	Q = d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q = d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q = d	q_3	q_4	q_5	q_6	q_7
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	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q = d

H = High voltage level steady state.
L = Low voltage level steady state.
X = Don't care.
d = High or Low data one set-up time prior to the Low-to-High Enable transition.
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max		24	46	mA
		I_{CCL}			37	75	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D to Q_n	Waveform 2	4.0 3.0	7.0 5.0	9.0 7.0	4.0 2.5	13.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n	Waveform 1	4.5 3.0	8.0 5.0	10.5 7.0	4.5 3.0	14.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 3	5.0 4.0	10.0 8.5	14.0 9.5	5.0 4.0	14.5 12.0	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 4	5.0	7.0	9.0	5.0	14.0	ns

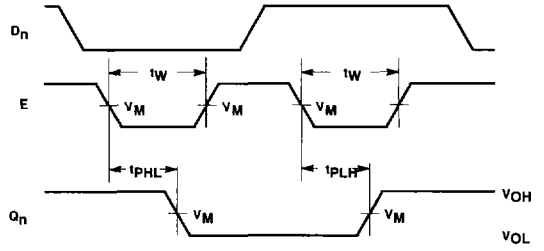
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D to $\overline{E}$	Waveform 5	3.0 6.5			3.0 8.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D to $\overline{E}$	Waveform 5	0 0			0 0		ns ns
t_s	Setup time, High or Low A_n to $\overline{E}$[4]	Waveform 6	2.0			2.0		ns
t_g	Hold time, High or Low A_n to $\overline{E}$[5]	Waveform 6	0			1.0		ns
t_w	$\overline{E}$ pulse width	Waveform 1	7.5			8.0		ns
t_w	$\overline{MR}$ pulse width	Waveform 4	3.0			4.0		ns

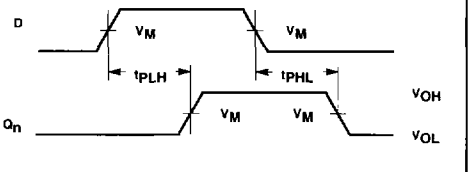
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. The Address to Enable setup time is the time before the High-to-Low Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
5. The Address to Enable hold time is the time after the Low-to-High Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

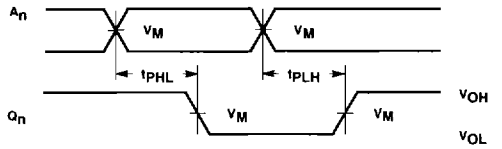
AC WAVEFORMS



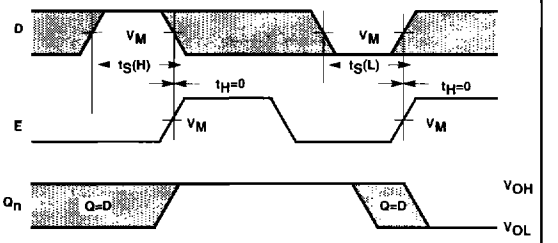
Waveform 1. Propagation Delay Enable to Output and Enable Pulse Width



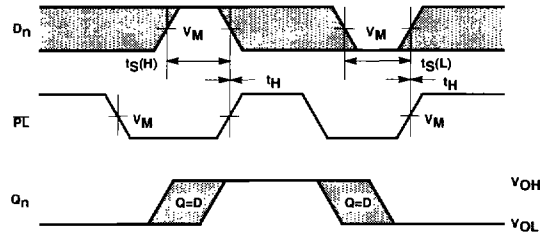
Waveform 2. Propagation Delay Data to Output



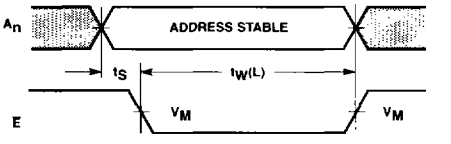
Waveform 3. Propagation Delay Address to Output



Waveform 4. Master Reset to Output Delay and Master Reset Pulse Width



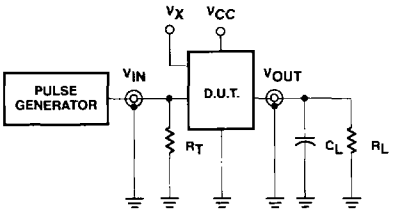
Waveform 5. Data Setup and Hold Times



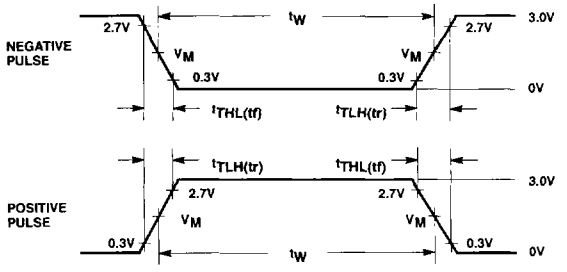
Waveform 6. Address Setup and Hold Times

NOTE: For all waveforms, $V_M = 1.5V$
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns