Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MV74SC373, MV74SC374, MV74SC533 MV74SC534, MV74SC563, MV74SC564 MV74SC573, MV74SC574

3-STATE OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE TRIGGERED FLIP-FLOPS

This family of 8 bit latches features 3-state operation and is designed for use in high speed, bus oriented systems. The '373 appears transparent to data (outputs change asynchronously) when Latch Enable, $\overline{LE}$, is HIGH. When $\overline{LE}$ is LOW, data meeting the set up times becomes latched. The '374 latches hold their individual data when meeting set up times with the clock, CK, LOW-to-HIGH transition. With both devices $\overline{OE}$ does not affect the state of the latches, but when $\overline{OE}$ is HIGH the outputs become high impedance. Data may thus be latched even when the device is deselected. The family offers a choice of inverted or non-inverted outputs.

The devices are available in 20-lead ceramic DIL (DG) package.

FEATURES

- Equivalent to 74LS Series
- Low Power ISO-CMOS Technology
- Short Propagation Delay
- Improved Noise Margins, with Input Hysteresis
- Bus Oriented 3-State Outputs
- High Current, Sink/Source Capability

DEVICE SELECTION

Product	Format	Output
MV74SC373	transparent latch	non-inverted
MV74SC374	D type flip-flop	non-inverted
MV74SC533	transparent latch	inverted
MV74SC534	D type flip-flop	inverted
MV74SC563	transparent latch	inverted
MV74SC564	D type flip-flop	inverted
MV74SC573	transparent latch	non-inverted
MV74SC574	D type flip-flop	non-inverted

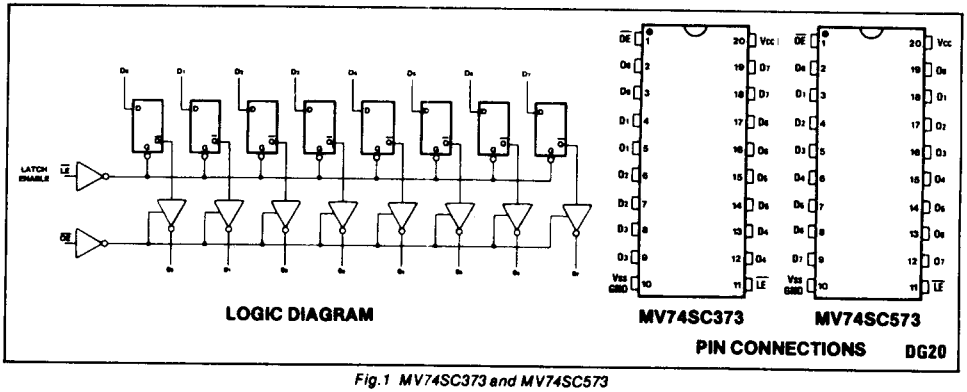

Fig.1 MV74SC373 and MV74SC573

RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage		V_{CC}	3	5	7	V
High level output current		I_{OH}		− 24		mA
Low level output current		I_{OL}		24		mA
Operating free-air temperature		Tamb	0		70	°C
Width of clock/enable pulse,		t_w	15			nS
Data set up time	MV74SCXX3 MV74SCXX4	t_{su}	0↓	2↓ 20↑		nS nS
Data hold time	MV74SCXX4 MV74SCXX4	t_h	10↓ 0↑			nS nS

1. The arrow indicates clock/enable transition: ↑ LOW to HIGH, ↓ HIGH to LOW
2. Voltage values are with respect to V_{SS}/GND

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
High level input voltage	V_{IH}	2.0			V	V_{CC} = 5.25V
Low level input voltage	V_{IL}			0.8	V	V_{CC} = 4.75V
Hysteresis ($V_{T+} - V_{T-}$) LE,CK,$\overline{OE}$			0.3		V	
High level output voltage	V_{OH}	2.4 4 35			V V	V_{CC} = 4.75V, I_{OH} = -10mA I_{OH} = -2mA
Low level output voltage	V_{OL}			0.4	V	V_{CC} = 4.75V, I_{OL} = 10mA
Input current at maximum input voltage	I_I			15	µA	V_{CC} = 5.25V, V_I = 5.5V
High level input current any input	I_{IH}			10	µA	V_{CC} = 5.25V, V_I = 2.7V
Low level input current	I_{IL}			− 10	µA	V_{CC} = 5.25V, V_I = 0.4V
Off-state output current high-level voltage applied	I_{OZH}			20	µA	V_{CC} = 5.25V, V_O = 2.7V
Off-state output current,low-level voltage applied	I_{OZL}			− 20	µA	V_{CC} = 5.25V, V_O = 0.4V
Short circuit current (Note 3)	I_{OS}		− 40		mA	V_{CC} = 5.25V
Quiescent supply current	I_{CC}			0.1	mA	V_{CC} = 5.25V, outputs disabled

3. Max. dissipation or 1mS duration should not be exceeded.
4. All TYP. values at T amb = 25°C V CC = 5V

SWITCHING CHARACTERISTICS (Fig. 5)

Test conditions (unless otherwise stated):
V_{CC} = 5V, T_{amb} = +25°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Propagation delay time, low-to-high level output	t_{PLH}		55 60		nS	MV74SC373, MV74SC573 C_L = 45pF MV74SC533, MV74SC563
Propagation delay time high-to-low level output	t_{PHL}		55 60		nS	MV74SC374, MV74SC574 MV74SC534, MV74SC564 R_L = 667
Output enable time to low level	t_{PZL}		40		nS	C_L = 5 pF
Output enable time to high level	t_{PZH}		40		nS	
Output disable time from low level	t_{PLZ}		33		nS	R_L = 667
Output disable time from high level	t_{PHZ}		72		nS	
Operating frequency	f_{MAX}		20		MHZ	Note 5

5. Maximum clock frequency is tested with all outputs loaded.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

PARAMETER	SYMBOL	VALUE
Supply voltage	V_{CC}	− 0.5V to 7.0V
Input voltage	V_I	− 0.3V to V_{CC} + 0.3V
Output current, per output	I_O	± 75mA
Operating temperature	Tamb	− 40°C to + 85°C
Storage temperature	T_S	− 65°C to 150°C
Package power dissipation	P	450mW

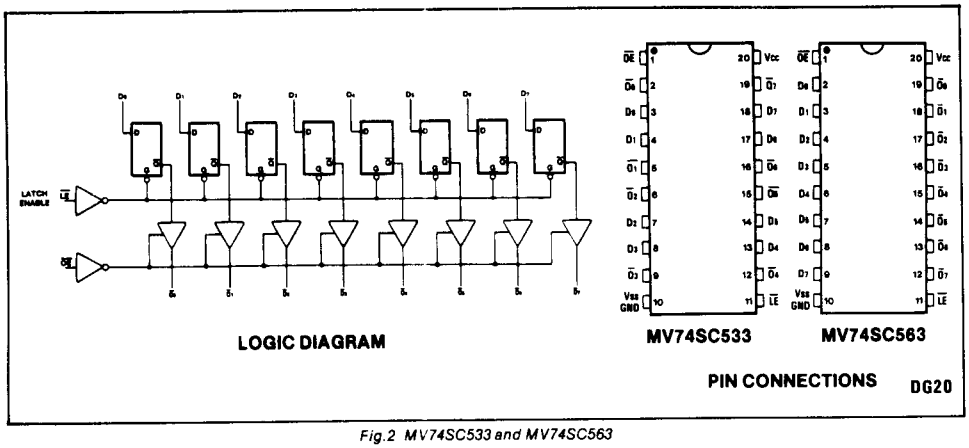

Fig.2 MV74SC533 and MV74SC563

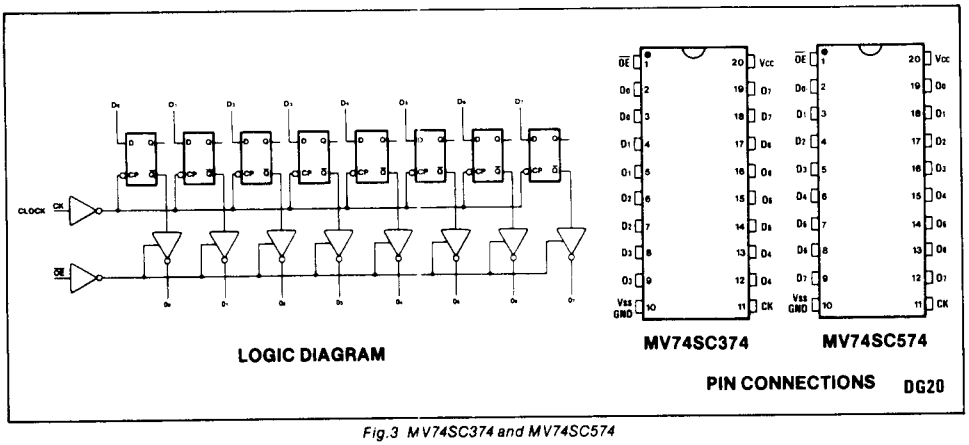

Fig.3 MV74SC374 and MV74SC574

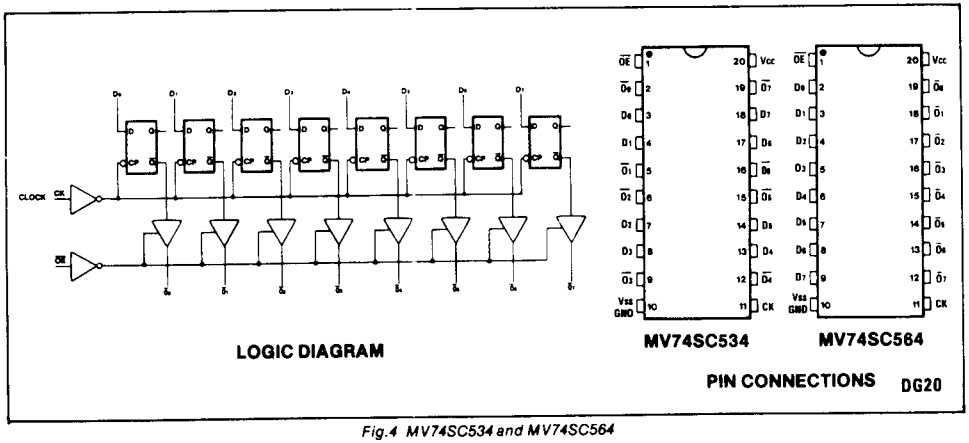

Fig.4 MV74SC534 and MV74SC564

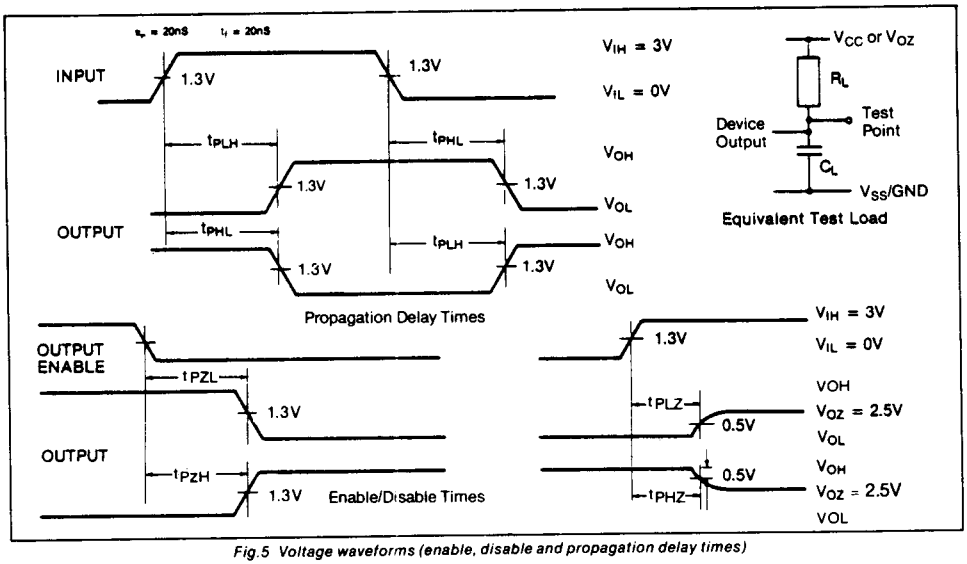

Fig.5 Voltage waveforms (enable, disable and propagation delay times)

PIN FUNCTIONS

Pin	Description
D_{0-7}	Data Inputs
O_{0-7}	Non Inverted Data Outputs
$\overline{O}_{0-7}$	Inverted Data Outputs
$\overline{OE}$	Output Enable
CK	Clock Input
$\overline{LE}$	Latch Enable
V_{CC}	Positive Supply Voltage
V_{SS}/GND	System Ground