

## **Rochester Electronics Manufactured Components**

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

## **Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

August 1997

## 12-Bit, Low Cost, Monolithic D/A Converters

### Features

- DAC 80V/DAC 85V Alternative Source
- Monolithic Construction
- Fast Settling Time (Typ) ..... 1.5 $\mu$ s
- Guaranteed Monotonicity
- Wafer Laser Trimmed Linearity, Gain, Offset
- Span Resistors On-Chip
- On-Board Reference
- Supply Operation .....  $\pm 12$ V

### Applications

- High Speed A/D Converters
- Precision Instrumentation
- CRT Display Generation

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI3-DAC80V-5	0 to 75	24 Ld PDIP	E24.6
HI3-DAC85V-4	-25 to 85	24 Ld PDIP	E24.6

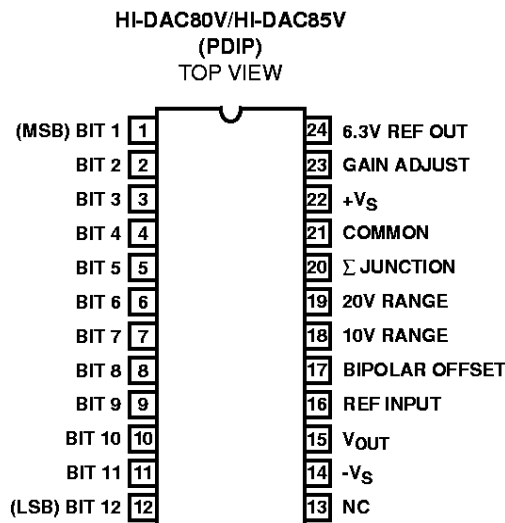
### Description

The HI-DAC80V is a monolithic direct replacement for the popular DAC80 and AD DAC80. The HI-DAC85V is a monolithic direct replacement for the popular DAC85 and AD DAC85 as well as the HI-5685V. Single chip construction along with several design innovations make the HI-DAC80V the optimum choice for low cost, high reliability applications. Harris' unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching times and minimum glitch. On board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy.

Internally the HI-DAC80V/HI-DAC85V eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

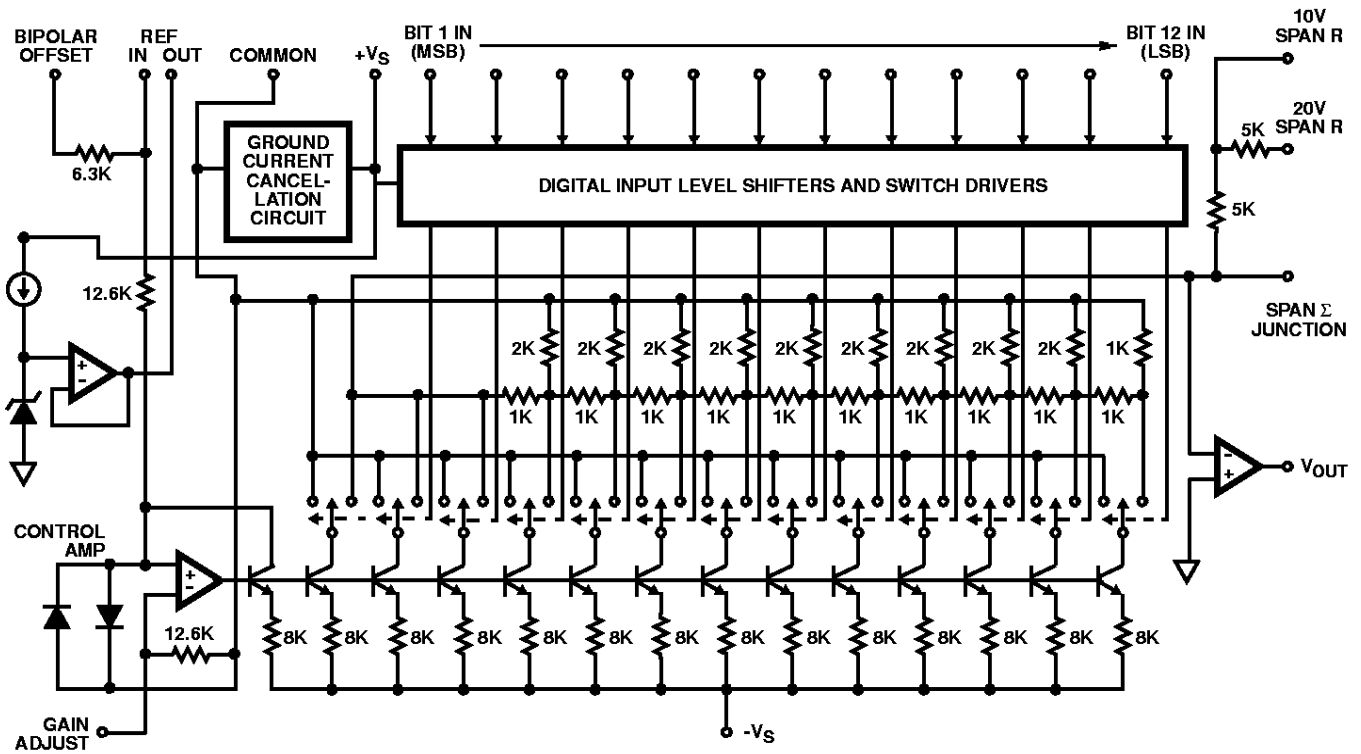
The HI-DAC80V is available as a voltage output device which is guaranteed over the 0°C to 75°C temperature range. The HI-DAC85V is available as a voltage output device which is guaranteed over the -25°C to 85°C temperature range. It includes a buried zener reference featuring a low temperature coefficient as well as an on board operational amplifier. The HI-DAC80V requires only two power supplies and will operate in the range of  $\pm (11.4$ V to 16.5V).

### Pinout



# HI-DAC80V, HI-DAC85V

## Functional Block Diagram



## HI-DAC80V, HI-DAC85V

### Absolute Maximum Ratings

Power Supply Inputs	
+V <sub>S</sub> .....	+20V
-V <sub>S</sub> .....	-20V
Reference	
Input (Pin 16) .....	+V <sub>S</sub>
Output Drain .....	2.5mA
Digital Inputs (Bits 1 to 12) .....	-1V to +V <sub>S</sub>

### Operating Conditions

Operating Temperature Range	
HI-DAC80V .....	0°C to 75°C
HI-DAV85V .....	-25°C to 85°C

### Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)
PDIP Package .....	60
Maximum Power Dissipation	
PDIP Package .....	550mW
Maximum Junction Temperature .....	150°C
Maximum Storage Temperature Range .....	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) .....	300°C

### Die Characteristics

Process .....	Bipolar-DI
Transistor Count .....	214

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

1.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### Electrical Specifications $T_A = 25^\circ\text{C}$ , $V_S \pm 12\text{V}$ to $\pm 15\text{V}$ (Note 4), Pin 16 to Pin 24, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	HI-DAC80V-5, HI-DAC85V-5			UNITS	
		MIN	TYP	MAX		
<b>SYSTEM PERFORMANCE</b>						
Resolution		-	-	12	Bits	
<b>ACCURACY</b> (Note 2)						
Linear Error	Full Temperature	-	$\pm 1/4$	$\pm 1/2$	LSB	
Differential Linearity Error	Full Temperature	-	$\pm 1/2$	$\pm 3/4$	LSB	
Monotonicity	Full Temperature	Guaranteed				
Gain Error	Full Temperature (Notes 1, 3)	-	$\pm 0.1$	$\pm 0.3$	% FSR	
Offset Error	Full Temperature (Note 1)		$\pm 0.05$	$\pm 0.15$	% FSR	
<b>ANALOG OUTPUT</b>						
Output Ranges		-	$\pm 2.5$	-	V	
		-	$\pm 5$	-	V	
		-	$\pm 10$	-	V	
		-	0 to 5	-	V	
		-	0 to 10	-	V	
Output Current		$\pm 5$	-	-	mA	
Output Resistance		-	0.05	-	$\Omega$	
Short Circuit Duration	To Common	Continuous			-	
<b>DRIFT</b> (Note 2)						
Total Bipolar Drift (Includes Gain, Offset and Linearity Drifts)	Full Temperature	-	-	$\pm 20$	ppm/°C	
Total Error	Full Temperature (Note 5)	-	$\pm 0.08$	$\pm 0.15$	% FSR	
						Bipolar
Gain	With Internal Reference	-	$\pm 15$	$\pm 30$	ppm/°C	
	Without Internal Reference	-	$\pm 7$	-	ppm/°C	
Unipolar Offset		-	$\pm 1$	$\pm 3$	ppm/°C	
Bipolar Offset		-	$\pm 5$	$\pm 10$	ppm/°C	
<b>CONVERSION SPEED</b>						
Settling Time	Full Scale Transition All Bits ON to OFF or OFF to ON to $\pm 0.01\%$ or FSR (Note 2)	-	3	-	$\mu\text{s}$	
					With 10K Feedback	$\mu\text{s}$
					With 5K Feedback	$\mu\text{s}$
For 1 LSB Change		-	1.5	-	$\mu\text{s}$	

## HI-DAC80V, HI-DAC85V

### Electrical Specifications $T_A = 25^\circ\text{C}$ , $V_S \pm 12\text{V}$ to $\pm 15\text{V}$ (Note 4), Pin 16 to Pin 24, Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	HI-DAC80V-5, HI-DAC85V-5			UNITS
		MIN	TYP	MAX	
Slew Rate		10	15	-	V/ $\mu\text{s}$
<b>INTERNAL REFERENCE</b>					
Output Voltage		6.250	+6.3	6.350	V
Output Impedance		-	1.5	-	$\Omega$
External Current		-	-	+2.5	mA
Tempco of Drift		-	5	-	ppm/ $^\circ\text{C}$
<b>DIGITAL INPUT (Note 2)</b>					
Logic Levels					
Logic "1"	TTL Compatible At +1 $\mu\text{A}$	+2	-	+5.5	V
Logic "0"	TTL Compatible At -100 $\mu\text{A}$	0	-	+0.8	V
<b>POWER SUPPLY SENSITIVITY (Notes 2, 4)</b>					
+15V Supply		-	0.001	0.002	% FSR / % $V_S$
-15V Supply		-	0.001	0.002	% FSR / % $V_S$
<b>POWER SUPPLY CHARACTERISTICS (Note 4)</b>					
Voltage Range					
+ $V_S$	Full Temperature	+11.4	+15	+16.5	V
- $V_S$	Full Temperature	-11.4	-15	-16.5	V
Current					
+ $I_S$	Full Temperature, $V_S = \pm 15\text{V}$	-	+12	+15	mA
- $I_S$	Full Temperature, $V_S = \pm 15\text{V}$	-	-15	-20	mA

#### NOTES:

- Adjustable to zero using external potentiometers.
- See Definitions.
- FSR is "Full Scale Range: and is 20V for  $\pm 10\text{V}$  range, 10V for  $\pm 5\text{V}$  range, etc.
- The HI-DAC80V/HI-DAC85V will operate with supply voltages as low as  $\pm 11.4\text{V}$ . It is recommended that output voltage range -10V to +10V not be used if the supply voltages are less than  $\pm 12.5\text{V}$ .
- With Gain and Offset errors adjusted to zero at  $25^\circ\text{C}$ .

## Definitions of Specifications

### Digital Inputs

The HI-DAC80V accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

### Settling Time

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of  $\pm 1/2$  LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low. In a 12-bit system  $\pm 1/2$  LSB =  $\pm 0.012\%$  of FSR.

TABLE 1.

DIGITAL INPUT	ANALOG OUTPUT		
	COMPLEMENTARY STRAIGHT BINARY	COMPLEMENTARY OFFSET BINARY	COMPLEMENTARY TWO'S COMPLEMENT †
MSB...LSB			
000...000	+ Full Scale	+ Full Scale	-LSB
100...000	Mid Scale-1 LSB	-1 LSB	+ Full Scale
111...111	Zero	- Full Scale	Zero
011...111	+ $1/2$ Full Scale	Zero	- Full Scale

† Invert MSB with external inverter to obtain CTC Coding

## HI-DAC80V, HI-DAC85V

### Thermal Drift

Thermal drift is based on measurements at 25°C, at high ( $T_H$ ) and low ( $T_L$ ) temperatures. Drift calculations are made for the high ( $T_H - 25^\circ\text{C}$ ) and low ( $25^\circ\text{C} - T_L$ ) ranges, and the larger of the two values is given as a specification representing worst case drift.

Gain Drift, Offset Drift, Reference Drift and Total Bipolar Drift are calculated in parts per million per °C as follows:

$$\text{GainDrift} = \frac{\Delta\text{FSR}/\Delta^\circ\text{C}}{\text{FSR}} \times 10^6$$

$$\text{OffsetDrift} = \frac{\Delta\text{Offset}/\Delta^\circ\text{C}}{\text{FSR}} \times 10^6$$

$$\text{ReferenceDrift} = \frac{\Delta V_{\text{REF}}/(\Delta^\circ\text{C})}{V_{\text{REF}}} \times 10^6$$

$$\text{TotalBipolarDrift} = \frac{\Delta V_{\text{O}}/(\Delta^\circ\text{C})}{\text{FSR}} \times 10^6$$

NOTE: FSR = Full Scale Output Voltage - Zero Scale Output Voltage

$\Delta\text{FSR} = \text{FSR}(T_H) - \text{FSR}(25^\circ\text{C})$ ,  
or  $\text{FSR}(25^\circ\text{C}) - \text{FSR}(T_L)$ .

$V_{\text{O}} =$  Steady State response to any input code.

Total Bipolar Drift is the variation of output voltage with temperature, in the bipolar mode of operation. It represents the net effect of drift in Gain, Offset, Linearity and Reference Voltage. Total Bipolar Drift values are calculated, based on measurements as explained above. Gain and Offset need not be calibrated to zero at 25°C. The specified limits for TBD apply for any input code and for any power supply setting within the specified operating range.

### Accuracy

**Linearity Error** (Short for "Integral Linearity Error." Also, sometimes called "Integral Nonlinearity" and "Nonlinearity".) The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to end-point linearity for D/A converter products from Harris Semiconductor, i.e., the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

**Differential Linearity Error** The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of  $\pm 1$  LSB or less guarantees monotonicity.

**Monotonicity** The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

**Total Error** The net output error resulting from all internal effects (primarily non-ideal Gain, Offset, Linearity and Reference Voltage). Supply voltages may be set to any

values within the specified operating range. Gain and offset errors must be calibrated to zero at 25°C. Then the specified limits for Total Error apply for any input code and for any temperature within the specified operating range.

### Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in  $-V_S$ , or  $+V_S$  supplies. It is specified under DC conditions and expressed as full scale range percent of change divided by power supply percent change.

$$\text{PSS} = \frac{\frac{\Delta\text{FullScaleRange} \times 100}{\text{FSR}(\text{Nominal})}}{\frac{\Delta V_S \times 100}{V_S(\text{Nominal})}}$$

### Glitch

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale, i.e., the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the Product of duration and amplitude.)

### Decoupling and Grounding

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-DAC80V/HI-DAC85V (preferably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

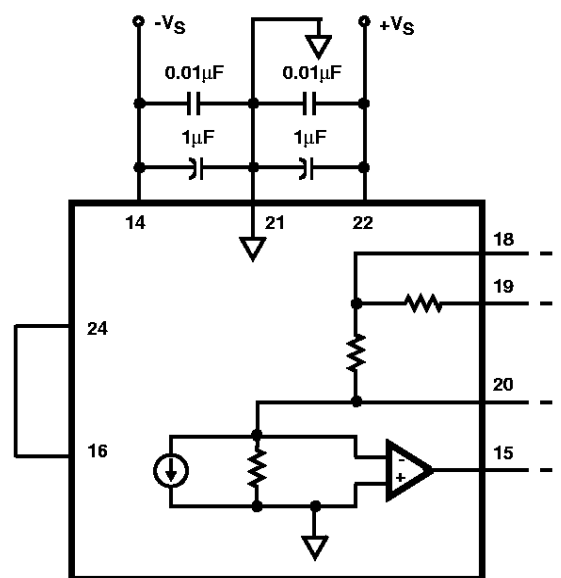


FIGURE 1.

# HI-DAC80V, HI-DAC85V

## Reference Supply

An internal 6.3V reference is provided on board the HI-DAC80V/HI-DAC85V. The voltage (pin 24) is accurate to  $\pm 0.8\%$  and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-DAC80V/HI-DAC85V. All gain adjustments should be made under constant load conditions.

## Output Voltage Ranges

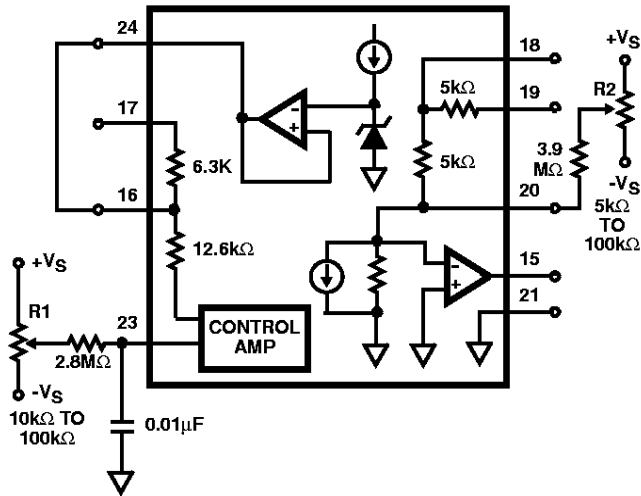


FIGURE 2. HI-DAC80V/HI-DAC85V

TABLE 2. RANGE CONNECTIONS

	RANGE	CONNECT		
		PIN 15	PIN 17	PIN 19
Unipolar	0 to +5V	18	NC	20
	0 to +10V	18	NC	NC
Bipolar	$\pm 2.5V$	18	20	20
	$\pm 5V$	18	20	NC
	$\pm 10V$	19	20	15

TABLE 3. GAIN AND OFFSET CALIBRATIONS

UNIPOLAR CALIBRATION	
Step 1:	Offset Turn all bits OFF (11 . . . 1) Adjust R2 for 0V out
Step 2:	Gain Turn all bits ON (00 . . . 0) Adjust R1 for FS - 1 LSB That is: 4.9988 for 0 to +5V range 9.9976 for 0 to +10V range
BIPOLAR CALIBRATION	
Step 1:	Offset Turn all bits OFF (11 . . . 1) Adjust R2 for Negative FS That is: -10V for $\pm 10V$ range -5V for $\pm 5V$ range -2.5V for $\pm 2.5V$ range
Step 2:	Gain Turn all bits ON (00 . . . 0) Adjust R1 for Positive FS - 1 LSB That is: +9.9951V for $\pm 10V$ Range +4.9976V for $\pm 5V$ Range +2.4988V for $\pm 2.5V$ Range
This Bipolar procedure adjusts the output range end points. The maximum error at zero (half scale) will not exceed the Linearity Error. See the "Accuracy" Specifications.	

# HI-DAC80V, HI-DAC85V

## Die Characteristics

### DIE DIMENSIONS:

108 mils x 163 mils

### METALLIZATION:

Type: Al

Thickness:  $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

### TIE SUBSTRATE TO:

Ground

### PASSIVATION:

Type: Nitride over Silox

Nitride Thickness:  $3.5\text{k}\text{\AA} \pm 0.5\text{k}\text{\AA}$

Silox Thickness:  $12\text{k}\text{\AA} \pm 1.5\text{k}\text{\AA}$

### WORST CASE CURRENT DENSITY:

$0.95 \times 10^5 \text{ A/cm}^2$

## Metallization Mask Layout

