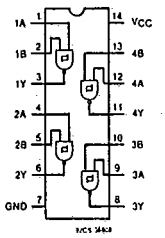
File Number **1649**

CD54/74HC132
CD54/74HCT132

High-Speed CMOS Logic

T-51-21-00



FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

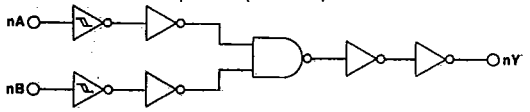
Quad 2-Input NAND Schmitt Trigger

Type Features:

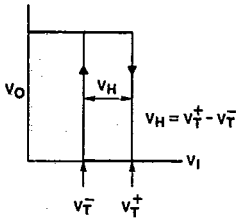
- *Unlimited input rise and fall times*
- *Exceptionally high noise immunity*

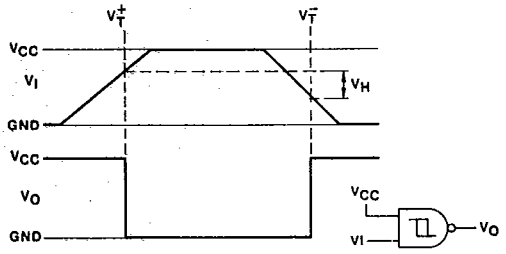
The RCA-CD54/74HC132 and CD54/74HCT132 each contain four 2-input NAND Schmitt Triggers in one package.

The CD54HC132 and CD54HCT132 are supplied in 14-lead ceramic dual-in-line packages (F suffix). The CD74HC132 and CD74HCT132 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both devices are also available in chip form (H suffix).



LOGIC DIAGRAM 92CS-38465RI





Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 37%, N_{IH} = 51% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = High level
L = Low level

92CM-38466

Fig. 1 - Hysteresis definition, characteristic, and test setup.

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CD54/74HC132
CD54/74HCT132

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\ V < V_o < V_{CC} + 0.5V$) ..... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	Unlimited	ns
at 4.5 V	0	Unlimited	ns
at 6 V	0	Unlimited	ns

*Unless otherwise specified, all voltages are referenced to Ground.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC132/CD54HC132 TEST CONDITIONS V_I V	I_O mA	V_{CC} V	74HC/54HC TYPE +25°C Min	Max	74HC TYPE -40/+85°C Min	Max	54HC TYPE -55/+125°C Min	Max	CD74HCT132/CD54HCT132 TEST CONDITIONS V_I V	V_{CC} V	74HCT/54HCT TYPE +25°C Min	Max	74HCT TYPE -40/+85°C Min	Max	54HCT TYPE -55/+125°C Min	Max	UNITS
Input Switch Points V_T^+			2	0.7	1.5	0.7	1.5	0.7	1.5			—	—	—	—	—	—	
			4.5	1.7	3.15	1.7	3.15	1.7	3.15		4.5	1.2	1.9	1.2	1.9	1.2	1.9	V
			6	2.1	4.2	2.1	4.2	2.1	4.2		5.5	1.4	2.1	1.4	2.1	1.4	2.1	
V_T^-			2	0.3	1	0.3	1	0.3	1			—	—	—	—	—	—	
			4.5	0.9	2.2	0.9	2.2	0.9	2.2		4.5	0.5	1.2	0.5	1.2	0.5	1.2	V
			6	1.2	3	1.2	3	1.2	3		5.5	0.6	1.4	0.6	1.4	0.6	1.4	
V_H			2	0.2	1	0.2	1	0.2	1			—	—	—	—	—	—	
			4.5	0.4	1.4	0.4	1.4	0.4	1.4		4.5	0.4	1.4	0.4	1.4	0.4	1.4	V
			6	0.6	1.6	0.6	1.6	0.6	1.6		5.5	0.4	1.5	0.4	1.5	0.4	1.5	
High-Level Output Voltage V_{OH} CMOS Loads	V_T^- or V_T^+	-0.02	2	1.9	—	1.9	—	1.9	—	V_T^- or V_T^+		—	—	—	—	—	—	
			4.5	4.4	—	4.4	—	4.4	—		4.5	4.4	—	4.4	—	4.4	—	V
			6	5.9	—	5.9	—	5.9	—			—	—	—	—	—	—	
TTL Loads	V_T^- or V_T^+		—	—	—	—	—	—	—	V_T^- or V_T^+		—	—	—	—	—	—	
		-4	4.5	3.98	—	3.84	—	3.7	—		4.5	3.98	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	5.34	—	5.2	—			—	—	—	—	—	—	
Low-Level Output Voltage V_{OL} CMOS Loads	V_T^- or V_T^+	0.02	2	—	0.1	—	0.1	—	0.1	V_T^- or V_T^+		—	—	—	—	—	—	
			4.5	—	0.1	—	0.1	—	0.1		4.5	—	0.1	—	0.1	—	0.1	V
			6	—	0.1	—	0.1	—	0.1			—	—	—	—	—	—	
TTL Loads	V_T^- or V_T^+			—	—	—	—	—	—	V_T^- or V_T^+		—	—	—	—	—	—	
		4	4.5	—	0.26	—	0.33	—	0.4		4.5	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	0.26	—	0.33	—	0.4			—	—	—	—	—	—	
Input Leakage Current I_I	V_{CC} or Gnd		6	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	2	—	20	—	40	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*										V_{CC}-2.1	4.5 to 5.5	Min —	Typ 100	Max 360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*
nA, nB	0.6

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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CD54/74HCT132

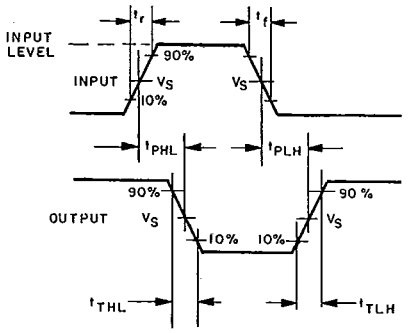
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay A, B to Y	t_{PLH}, t_{PHL}	15	10	13	ns
Power Dissipation Capacitance	C_{PD}*	—	30	30	pF

*C_{PD} is used to determine the dynamic power consumption, per gate.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where:
f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r,t_f = 6 ns)

CHARACTERISTIC		TEST CONDITIONS V_{CC} (V)	+25°C HC Min.	+25°C HC Max.	+25°C HCT Min.	+25°C HCT Max.	-40°C to +85°C 74HC Min.	-40°C to +85°C 74HC Max.	-40°C to +85°C 74HCT Min.	-40°C to +85°C 74HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Propagation Delay A, B to Y	t_{PLH}	2	—	125	—	—	—	156	—	—	—	188	—	—	
	t_{PHL}	4.5	—	25	—	33	—	31	—	41	—	38	—	50	ns
		6	—	21	—	—	—	27	—	—	—	32	—	—	
Output Transition Time	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50% V_{CC}	1.3V

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Fig. 2 - Transition times and propagation delay times.