



# FEMTOCLOCKS™ CRYSTAL-TO-LVPECL 375MHZ, FREQUENCY MARGINING SYNTHESIZER

**ICS843201-375**

## GENERAL DESCRIPTION

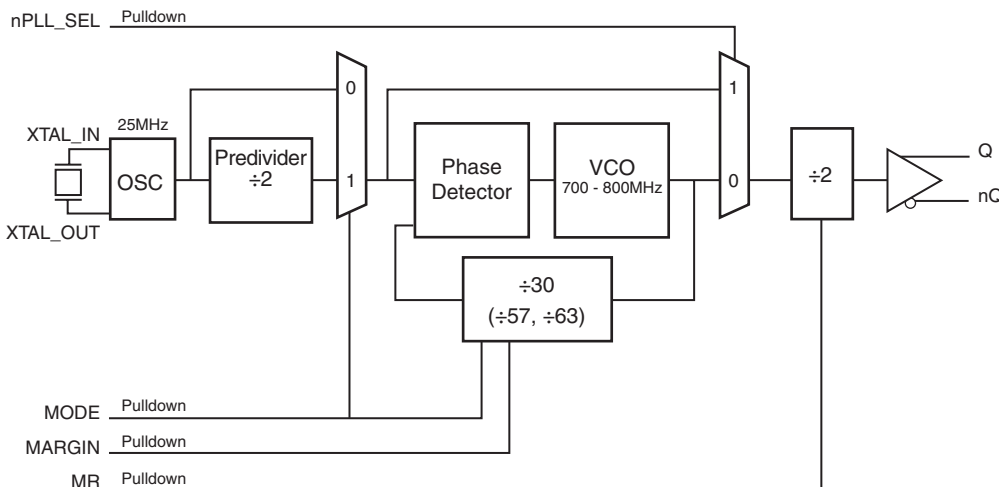


The ICS843201-375 is a low phase-noise frequency margining synthesizer and is a member of the HiPerClockS™ family of high performance clock solutions from IDT. In the default mode, the device nominally generates a 375MHz LVPECL output clock signal from a 25MHz crystal input. There is also a frequency margining mode available where the device can be configured, using control pins, to vary the output frequency up or down from nominal by 5%. The ICS843201-375 is provided in a 16-pin TSSOP package.

## FEATURES

- One 375MHz nominal LVPECL output
- Crystal oscillator interface designed for 25MHz, 18pF parallel resonant crystal
- Output frequency can be varied  $\pm 5\%$  from nominal
- VCO range: 700MHz - 800MHz
- RMS phase jitter @ 375MHz, using a 25MHz crystal (12kHz - 20MHz): 0.72ps (typical) @ 3.3V
- Output supply modes  
Core/Output  
3.3V/3.3V  
3.3V/2.5V  
2.5V/2.5V
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

## BLOCK DIAGRAM



## PIN ASSIGNMENT

Vcc	1	16	Q
MODE	2	15	nQ
nc	3	14	Vcco
XTAL_IN	4	13	Vcc
XTAL_OUT	5	12	VEE
MARGIN	6	11	MR
VEE	7	10	nPLL_SEL
nc	8	9	nc

### ICS843201-375 16-Lead TSSOP

4.4mm x 5.0mm x 0.92mm  
package body  
**G Package**  
Top View

## FUNCTIONAL DESCRIPTION

The ICS843201-375 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A 25MHz fundamental crystal is used as the input to the on chip oscillator. In regular mode, the 25MHz crystal frequency is applied directly to the phase detector. In frequency margining mode, the 25MHz crystal frequency is divided by 2 and a 12.5MHz reference frequency is applied to the phase detector. The VCO of the PLL operates over a range of 700MHz to 800MHz. The output of the M divider is also applied to the phase detector. The default mode for the ICS843201-375 is a nominal 375MHz output. The nominal output frequency can be changed by placing the device into the margining mode using

the mode pin and using the margin pin to change the M feedback divider. Frequency margining mode operation occurs when the MODE input is HIGH. The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. The output of the VCO is scaled by an output divider prior to being sent to the LVPECL output buffer. The divider provides a 50% output duty cycle. The relationship between the crystal input frequency, the M divider, the VCO frequency and the output frequency is provided in Table 1. When changing back from frequency margining mode to nominal mode, the device will return to the default nominal configuration described above.

**TABLE 1. FREQUENCY MARGIN FUNCTION TABLE**

MODE	MARGIN	XTAL (MHz)	Pre-Divider (P)	Reference Frequency (MHz)	Feedback Divider	VCO (MHz)	% Change
1	0	25	2	12.5	57	712.5	-5.0
0	X	25	none	25	30	750	Nom. Mode
1	1	25	2	12.5	63	787.5	5.0

TABLE 2. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 13	V <sub>CC</sub>	Power		Positive supply pins.
2	MODE	Input	Pulldown	MODE pin. LOW = default mode. HIGH = frequency margining mode. LVCMOS/LVTTL interface levels.
3, 8, 9	nc	Unused		No connect.
4, 5	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
6	Margin	Input	Pulldown	Sets the frequency margin to ±5% in frequency margining mode. See Table 1. LVCMOS/LVTTL interface levels.
7, 12	V <sub>EE</sub>	Power		Negative supply pins.
10	nPLL_SEL	Input	Pulldown	PLL select pin. When HIGH, PLL is bypassed and input is fed directly to the output dividers. When LOW, PLL is enabled. LVCMOS/LVTTL interface levels.
11	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q to go low and the inverted output nQ to go high. When logic LOW, the internal dividers and the output is enabled. LVCMOS/LVTTL interface levels.
14	V <sub>CCO</sub>	Power		Output supply pin.
15, 16	nQ, Q	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 3. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

TABLE 4. MODE CONTROL INPUT FUNCTION TABLE

Input	Condition
MODE	Q, nQ
0	Default Mode
1	Frequency Margining Mode

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	99.9°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 5A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Positive Supply Voltage		3.135	3.3	3.465	V
$V_{CCO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				108	mA
$I_{CC}$	Power Supply Current				96	mA
$I_{CCO}$	Output Supply Current				12	mA

**TABLE 5B. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CCO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Positive Supply Voltage		3.135	3.3	3.465	V
$V_{CCO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current				108	mA
$I_{CC}$	Power Supply Current				96	mA
$I_{CCO}$	Output Supply Current				12	mA

**TABLE 5C. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Positive Supply Voltage		2.375	2.5	2.625	V
$V_{CCO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current				101	mA
$I_{CC}$	Power Supply Current				95	mA
$I_{CCO}$	Output Supply Current				6	mA

TABLE 5D. LVCMOS / LVTTTL DC CHARACTERISTICS,  $T_A = 0^\circ\text{C}$  TO  $70^\circ\text{C}$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{CC} = 3.3\text{V}$	2		$V_{CC} + 0.3$	V
		$V_{CC} = 2.5\text{V}$	1.7		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{CC} = 3.3\text{V}$	-0.3		0.8	V
		$V_{CC} = 2.5\text{V}$	-0.3		0.7	V
$I_{IH}$	Input High Current	MARGIN, MODE, nPLL_SEL, MR $V_{CC} = V_{IN} = 3.465$ or $2.625\text{V}$			150	$\mu\text{A}$
$I_{IL}$	Input Low Current	MARGIN, MODE, nPLL_SEL, MR $V_{CC} = 3.465\text{V}$ or $2.625\text{V}$ , $V_{IN} = 0\text{V}$	-5			$\mu\text{A}$

TABLE 5E. LVPECL DC CHARACTERISTICS,  $T_A = 0^\circ\text{C}$  TO  $70^\circ\text{C}$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO} - 2\text{V}$ .

TABLE 6. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF
Drive Level				300	$\mu\text{W}$

NOTE: Characterized using an 18pF parallel resonant crystal.

**TABLE 7A. AC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  TO  $70^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency			375		MHz
$t_{jit}(\Phi)$	RMS Phase Jitter (Random); NOTE 1	375MHz, Integration Range: 12kHz - 20MHz		0.72		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		550	ps
odc	Output Duty Cycle		49		51	%

NOTE 1: Refer to Phase Noise Plot.

**TABLE 7B. AC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CCO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  TO  $70^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency			375		MHz
$t_{jit}(\Phi)$	RMS Phase Jitter (Random); NOTE 1	375MHz, Integration Range: 12kHz - 20MHz		0.72		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		550	ps
odc	Output Duty Cycle		49		51	%

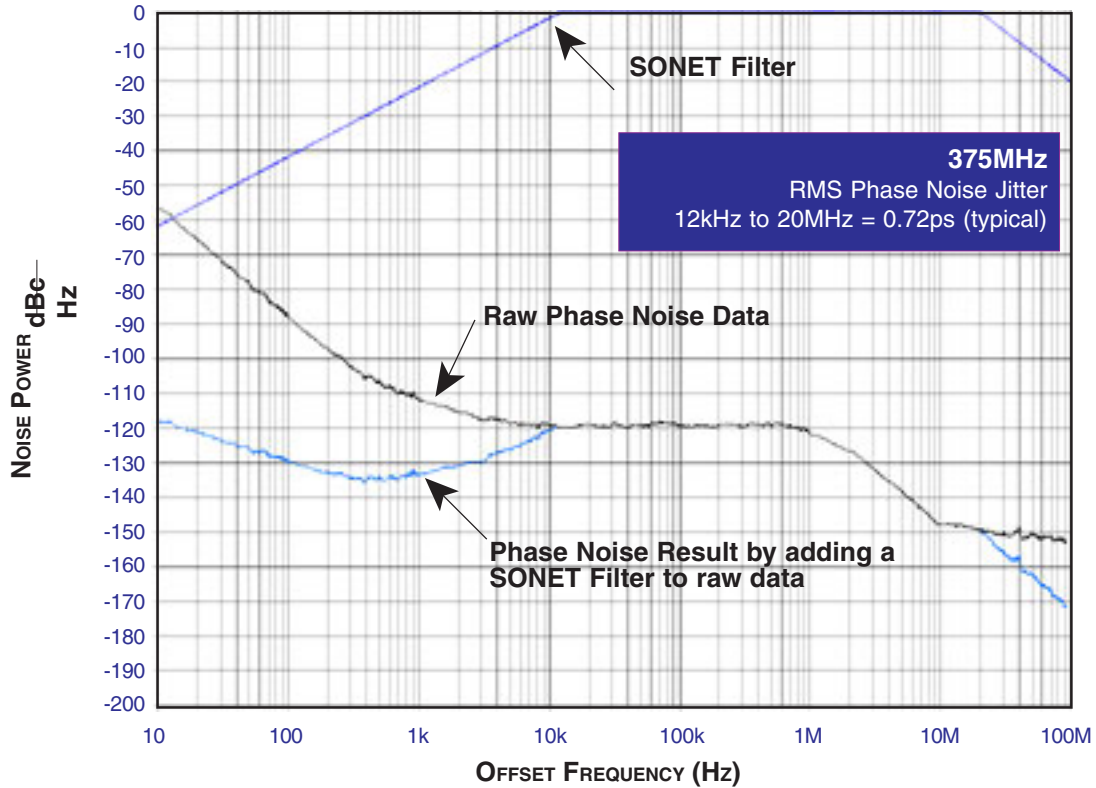
NOTE 1: Refer to Phase Noise Plot.

**TABLE 7C. AC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  TO  $70^\circ\text{C}$** 

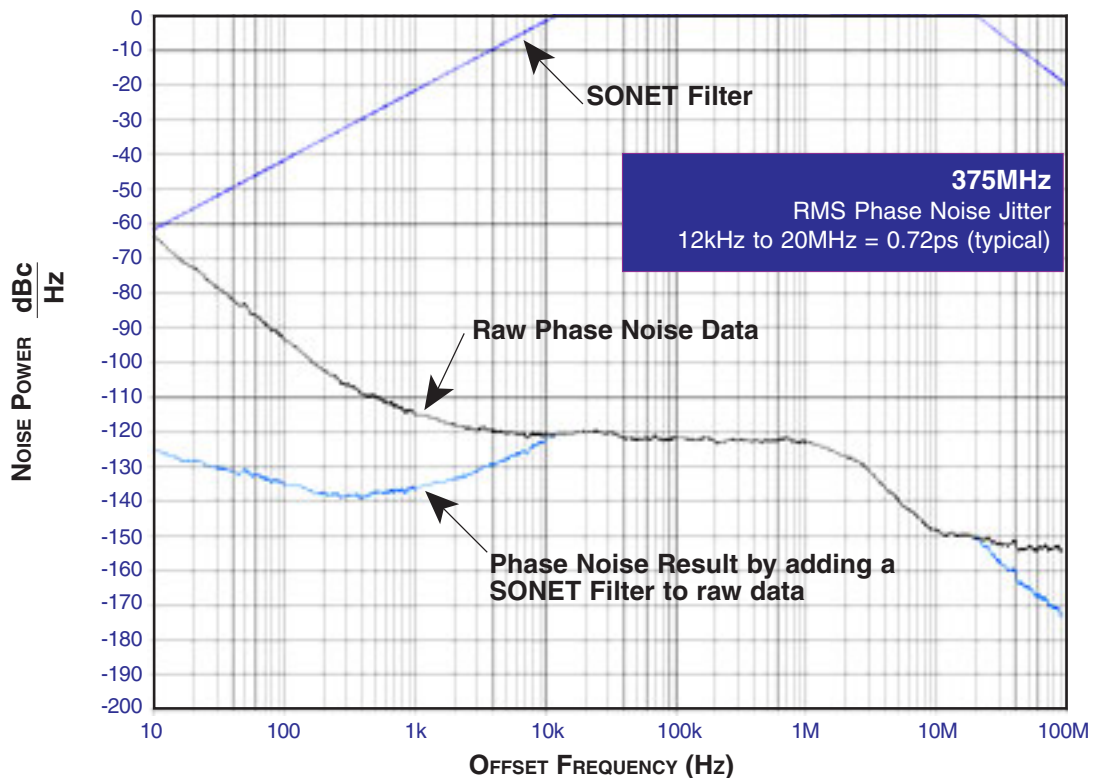
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency			375		MHz
$t_{jit}(\Phi)$	RMS Phase Jitter (Random); NOTE 1	375MHz, Integration Range: 12kHz - 20MHz		0.88		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		550	ps
odc	Output Duty Cycle		49		51	%

NOTE 1: Refer to Phase Noise Plot.

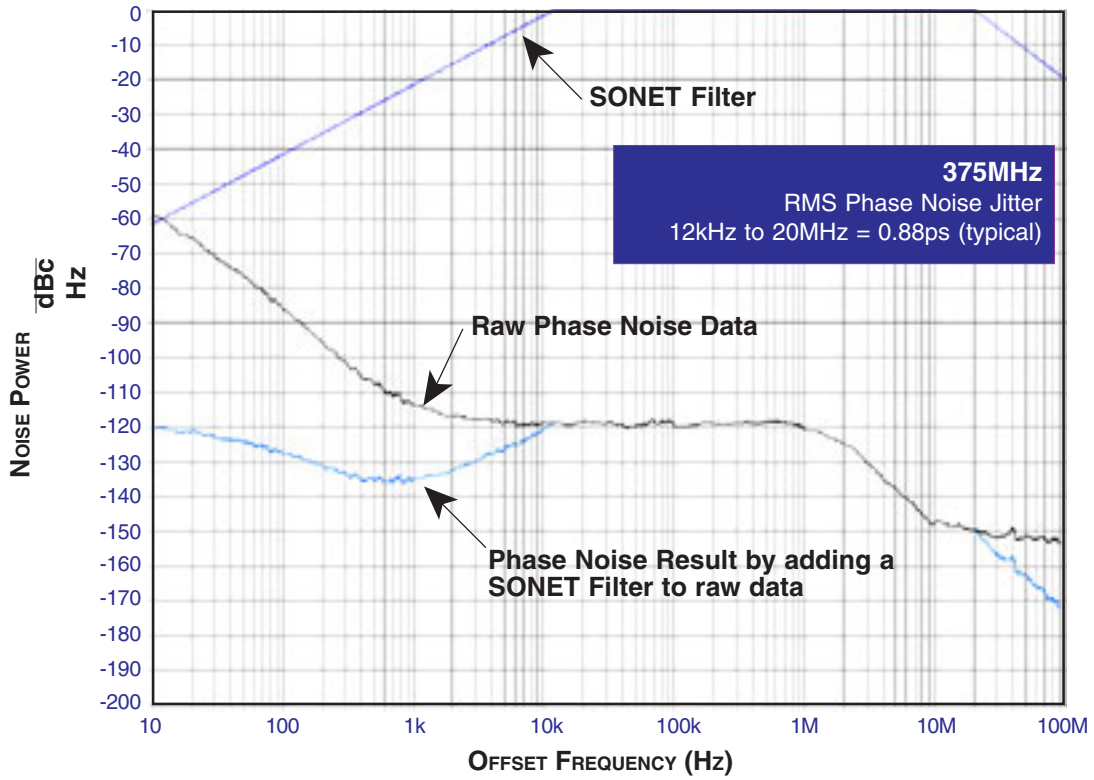
TYPICAL PHASE NOISE AT 375MHz @ 3.3V/3.3V



TYPICAL PHASE NOISE AT 375MHz @ 3.3V/2.5V

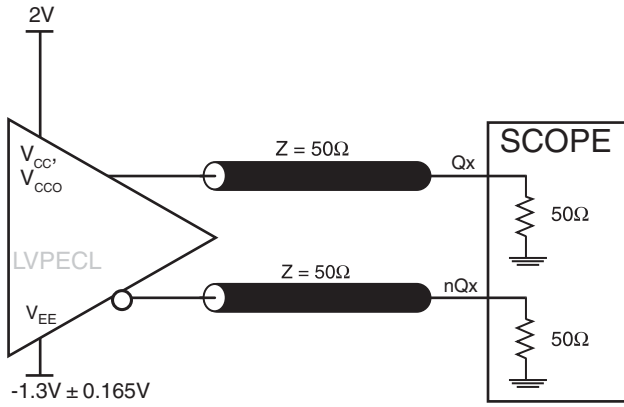


TYPICAL PHASE NOISE AT 375MHZ @ 2.5V/2.5V

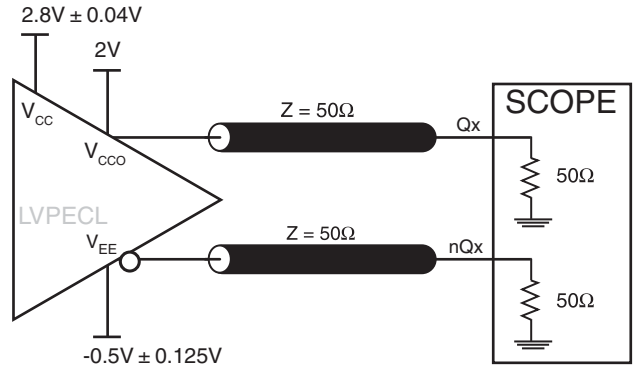




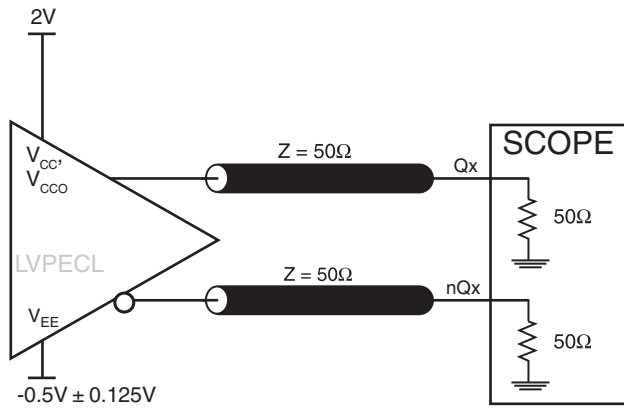
## PARAMETER MEASUREMENT INFORMATION



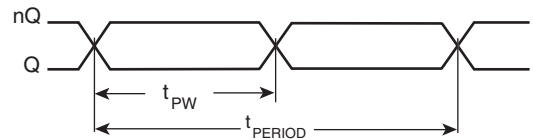
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT

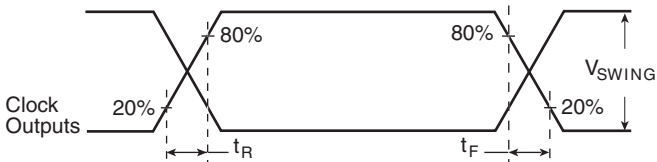


2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

## APPLICATION INFORMATION

### CRYSTAL INPUT INTERFACE

The ICS843201-375 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in

Figure 1 below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

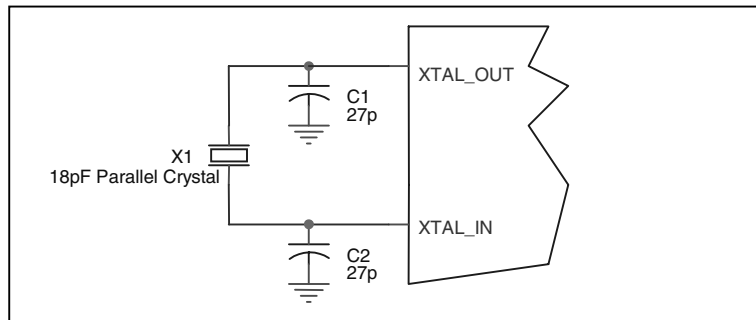


FIGURE 1. CRYSTAL INPUT INTERFACE

### LVCMOS TO XTAL INTERFACE

The XTAL\_IN input can accept a single-ended LVCMOS signal through an AC couple capacitor. A general interface diagram is shown in Figure 2. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and making  $R_2$  50Ω.

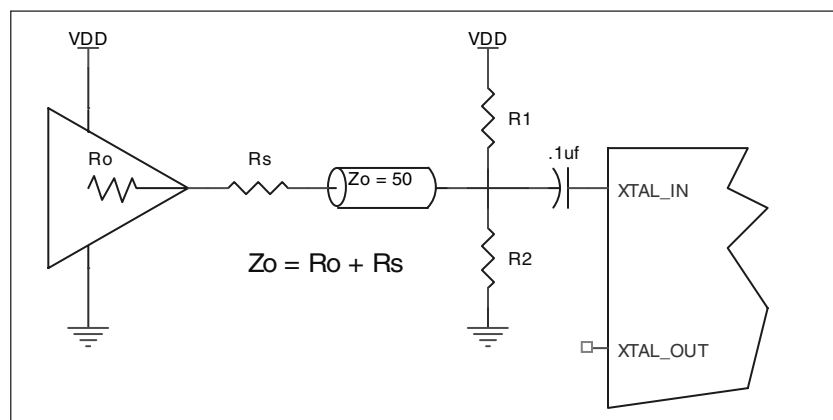


FIGURE 2. General Diagram for LVCMOS Driver to XTAL Input Interface

## RECOMMENDATIONS FOR UNUSED INPUT PINS

### INPUTS:

#### LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

## TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are

designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

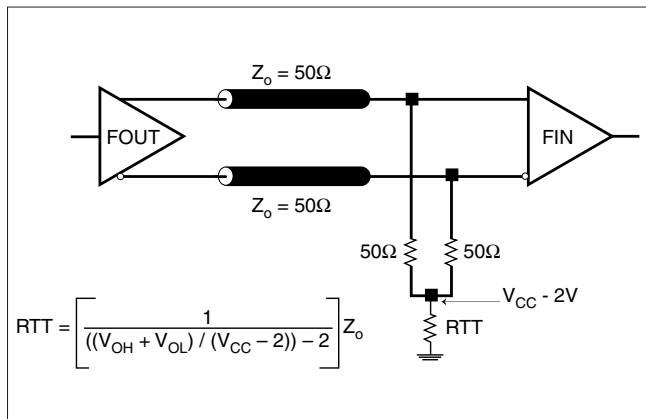


FIGURE 3A. LVPECL OUTPUT TERMINATION

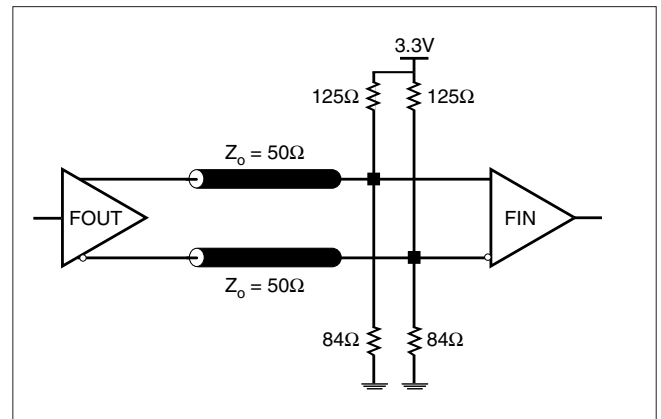
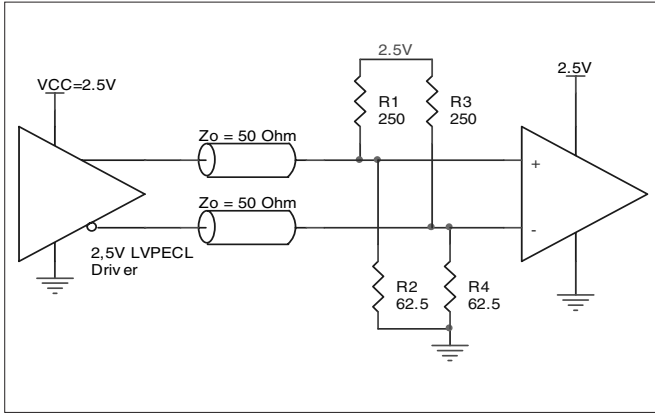


FIGURE 3B. LVPECL OUTPUT TERMINATION

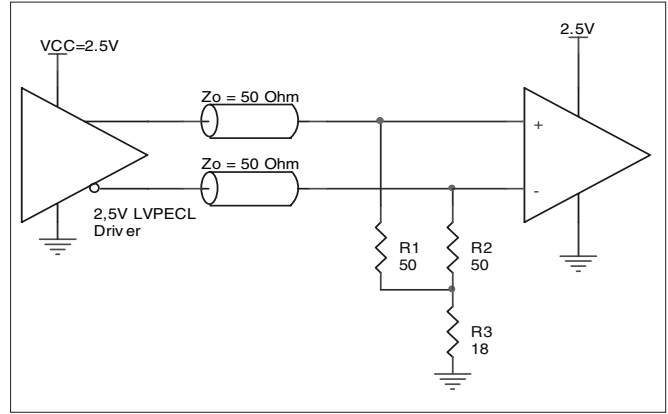
**TERMINATION FOR 2.5V LVPECL OUTPUT**

Figure 4A and Figure 4B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to  $V_{cc} - 2V$ . For  $V_{cc} = 2.5V$ , the  $V_{cc} - 2V$  is

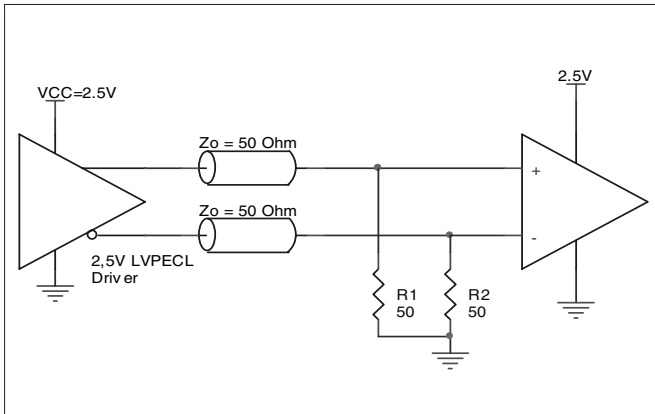
very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in Figure 4C.



**FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE**



**FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE**



**FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE**

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843201-375. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS843201-375 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 108mA = 374.2mW$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**

$$\text{Total Power}_{MAX} (3.465V) = 374.2mW + 30mW = 404.2mW$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming 0 air flow and a multi-layer board, the appropriate value is 99.9°C/W per Table 8 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 0.404W * 99.9^\circ C/W = 110^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

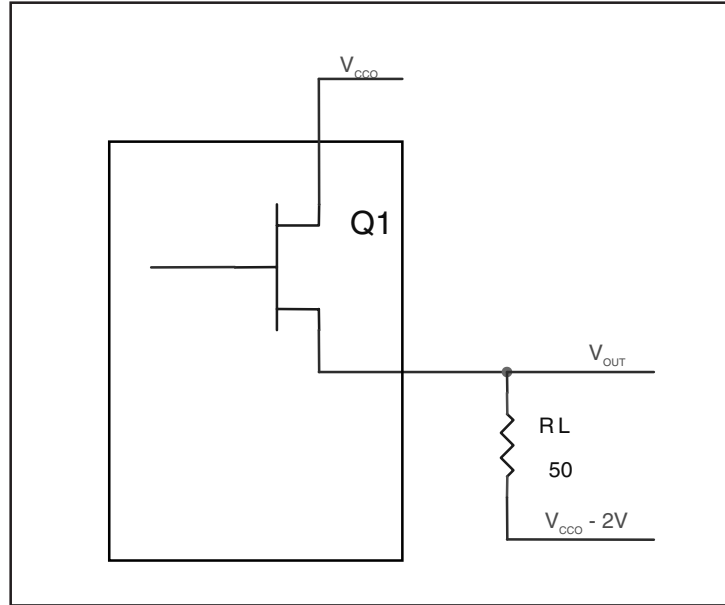
**TABLE 8. THERMAL RESISTANCE  $\theta_{JA}$  FOR 16-PIN TSSOP, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	99.9°C/W	35.6°C/W	93.5°C/W

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5*.



**FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CCO} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 0.9V$

$$(V_{CCO\_MAX} - V_{OH\_MAX}) = 0.9V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.7V$

$$(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.7V$$

Pd<sub>H</sub> is power dissipation when the output drives high.

Pd<sub>L</sub> is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair = Pd<sub>H</sub> + Pd<sub>L</sub> = 30mW

## RELIABILITY INFORMATION

TABLE 9.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	99.9°C/W	35.6°C/W	93.5°C/W

### TRANSISTOR COUNT

The transistor count for ICS843201-375 is: 2433

## PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

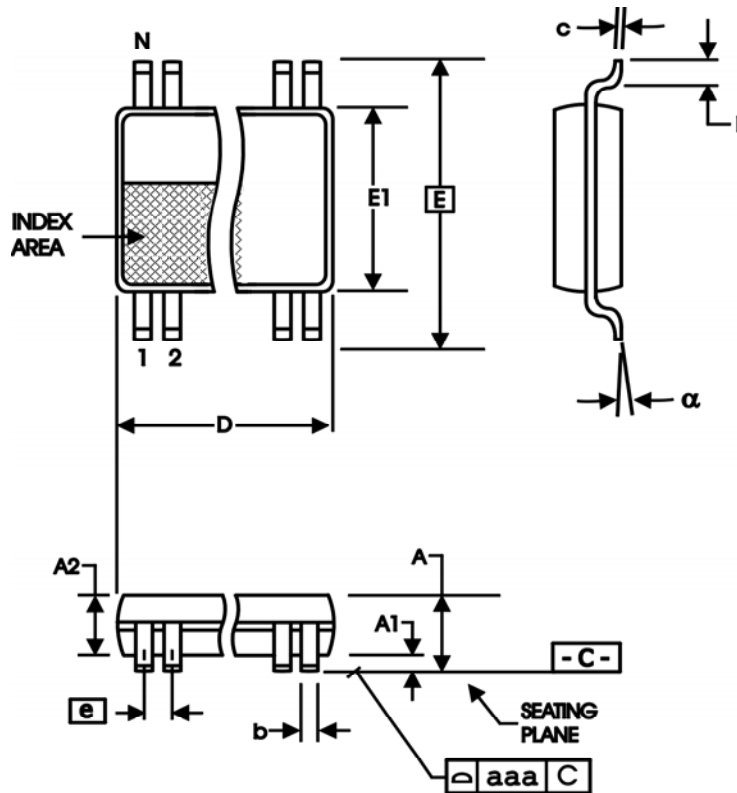


TABLE 10. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
$\alpha$	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153



TABLE 11. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843201AG-375	3201A375	16 Lead TSSOP	tube	0°C to 70°C
ICS843201AG-375T	3201A375	16 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS843201AG-375LF	201A375L	16 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS843201AG-375LFT	201A375L	16 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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