

128 K × 8 Very Low Power CMOS SRAM Rad Tolerant

Introduction

The M65608E is a very low power CMOS static RAM organized as 131072 × 8 bits.

TEMIC brings the solution to applications where fast computing is as mandatory as low consumption, such as aerospace electronics, portable instruments, or embarked systems.

Utilizing an array of six transistors (6T) memory cells, the M65608E combines an extremely low standby

supply current (Typical value = 0.2 μA) with a fast access time at 30 ns over the full military temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

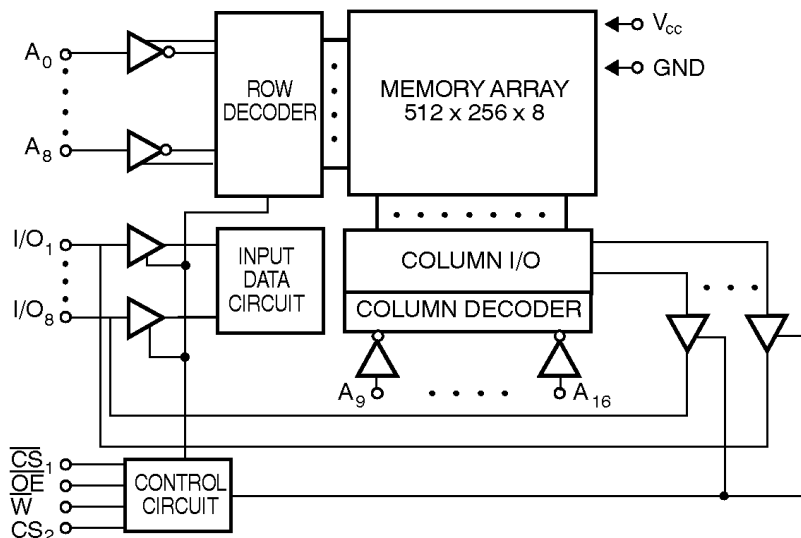
The M65608E is processed according to the methods of the latest revision of the MIL STD 883 (class B or S), ESA SCC 9000 or QML.

Features

- Access time: 30, 45 ns
- Very low power consumption
 - active : 250 mW (Typ)
 - standby : 1 μW (Typ)
 - data retention : 0.5 μW (Typ)
- Wide temperature Range : -55 To +125°C
- 400 Mils width package
- TTL compatible inputs and outputs
- Asynchronous
- Single 5 volt supply
- Equal cycle and access time
- Gated inputs :
 - no pull-up/down
 - resistors are required

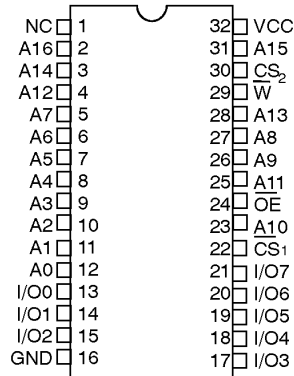
Interface

Block Diagram



Pin Configuration

32 pins DIL side-brazed 400 MILS
 32 pins Flatpack 400 MILS



Pin Names

A0–A16	Address inputs
I/O0–I/O7	Data Input/Output
\overline{CS}_1	Chip select 1
CS ₂	Chip select 2
\overline{W}	Write Enable
\overline{OE}	Output Enable
V _{CC}	Power
GND	Ground

Truth Table

\overline{CS}_1	CS ₂	\overline{W}	\overline{OE}	INPUTS/ OUTPUTS	MODE
H	X	X	X	Z	Deselect/ Power-down
X	L	X	X	Z	Deselect/ Power Down
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	Z	Output Disable

L = low, H = high, X = H or L, Z = high impedance.

Electrical Characteristics

Absolute Maximum Ratings

Supply voltage to GND potential : - 0.5 V + 7.0 V
 DC input voltage : GND - 0,3 V to VCC + 0,3
 DC output voltage high Z state : GND - 0,3 V to VCC + 0,3

Storage temperature : -65 °C to + 150 °C
 Output current into outputs (low) : 20 mA
 Electro statics discharge voltage : > 2 001 V
 (MIL STD 883D method 3015.3)

Operating Range

	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	5 V ± 10 %	- 55 °C to + 125 °C

Recommended DC Operating Conditions

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	GND - 0.3	0.0	0.8	V
VIH	Input high voltage	2.2	-	VCC + 0.3	V

Capacitance

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (1)	Input low voltage	-	-	8	pF
Cout (1)	Output high volt	-	-	8	pF

Note : 1. Guaranteed but not tested.

DC Parameters

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (2)	Input leakage current	- 1	-	1	μA
IOZ (2)	Output leakage current	- 1	-	1	μA
VOL (3)	Output low voltage	-	-	0.4	V
VOH (4)	Output high voltage	2.4	-	-	

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output Disabled.
 3. Vcc min. IOL = 8.0 mA.
 4. Vcc min. IOH = -4.0 mA.

Consumption

SYMBOL	DESCRIPTION	65608 - 30	65608 - 45	UNIT	VALUE
ICCSB (5)	Standby supply current	2	2	mA	max
ICCSB ₁ (6)	Standby supply current	300	300	μA	max
ICCOP (7)	Dynamic operating current	130	100	mA	max

- Notes :
- $\overline{CS}_1 \geq V_{IH}$ or $CS_2 \leq V_{IL}$ and $\overline{CS}_1 \leq V_{IL}$.
 - $\overline{CS}_1 \geq V_{CC} - 0.3$ V or, $CS_2 < Gnd + 0.3$ V and $\overline{CS}_1 \leq 0.2$ V
 - $F = 1/TAVAV$, $I_{out} = 0$ mA, $\overline{W} = \overline{OE} = V_{IH}$, $V_{in} = Gnd/V_{CC}$, V_{CC} max.

AC Parameters

Input pulse levels : Gnd to 3.0 V
 Input rise : 5 ns

Input timing reference levels : 1.5 V
 Output loading IOL/IOH (see figure 1a and 1b) : + 30 pF

AC Test Loads Waveforms

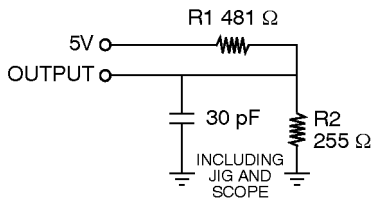


Figure 1a

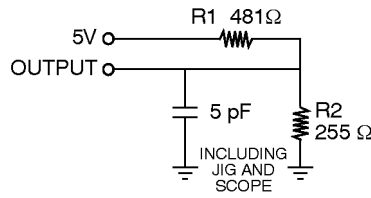


Figure 1b

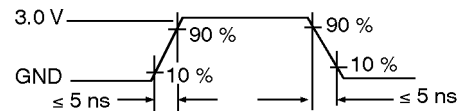
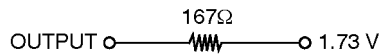


Figure 2

Equivalent to : THEVENIN EQUIVALENT



Data Retention Mode

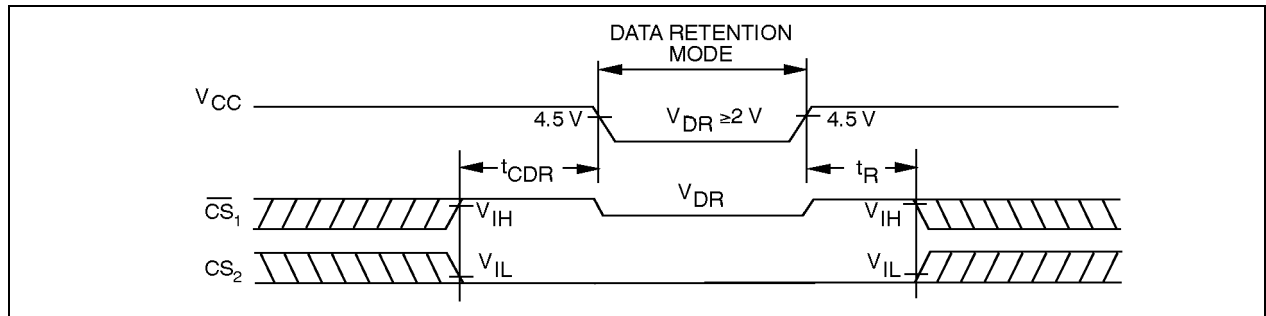
MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

- During data retention chip select \overline{CS}_1 must be held high within V_{CC} to $V_{CC} - 0.2$ V or, chip select CS_2 must be held low within GND to $GND + 0.2$ V.
- Output Enable (\overline{OE}) should be held high to keep the

RAM outputs high impedance, minimizing power dissipation.

- During power up and power down transitions \overline{CS}_1 and \overline{OE} must be kept between $V_{CC} + 0.3$ V and 70 % of V_{CC} , or with CS_2 between GND and $GND - 0.3$ V.
- The RAM can begin operation $> TR$ ns after V_{CC} reaches the minimum operation voltages (4.5 V).

Timing



Data Retention Characteristics

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL T _A = 25 °C	MAXIMUM		UNIT
VCCDR	Vcc for data retention	2.0	–	–		V
TCDR	Chip deselect to data retention time	0.0	–	–		ns
TR	Operation recovery time	TAVAV (9)	–	–		ns
ICCDR1 (10)	Data retention current @ 2.0 V	–	0.1		150	μA
ICCDR2 (10)	Data retention current @ 3.0 V	–	0.2		200	μA

Notes : 9. TAVAV = Read cycle time.

10. $\overline{CS}_1 = V_{CC}$ or $\overline{CS}_2 = \overline{CS}_1 = GND$, $V_{in} = Gnd/V_{CC}$, this parameter is only tested at $V_{CC} = 2 V$.

Write Cycle

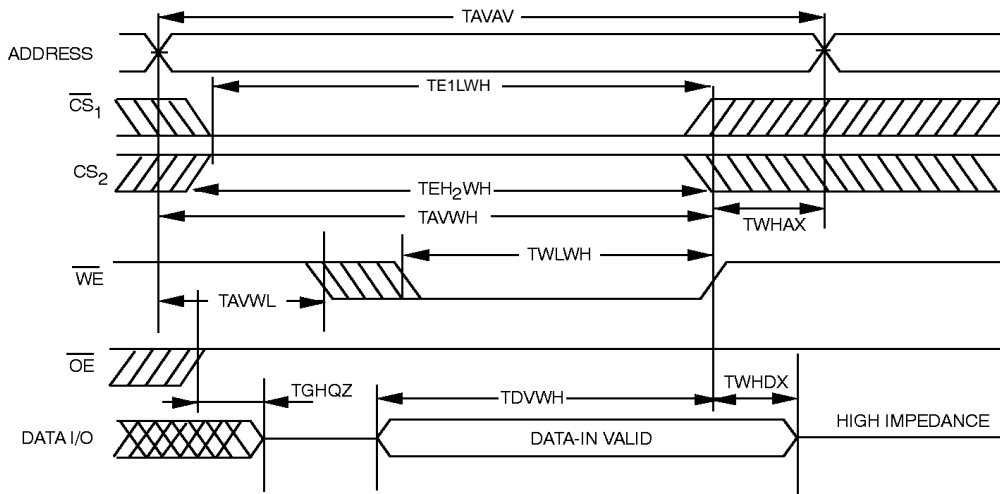
SYMBOL	PARAMETER	65608 – 30	65608 – 45	UNIT	VALUE
TAVAW	Write cycle time	30	45	ns	min
TAVWL	Address set-up time	0	0	ns	min
TAVWH	Address valid to end of write	22	35	ns	min
TDVWH	Data set-up time	18	25	ns	min
TE ₁ LWH	\overline{CS}_1 low to write end	22	35	ns	min
TE ₂ HWH	CS ₂ high to write end	22	35	ns	min
TWLQZ	Write low to high Z (11)	8	15	ns	max
TWLWH	Write pulse width	22	35	ns	min
TWHAX	Address hold from to end of write	0	0	ns	min
TWHDX	Data hold time	0	0	ns	min
TWHQX	Write high to low Z (11)	0	0	ns	min

Read Cycle

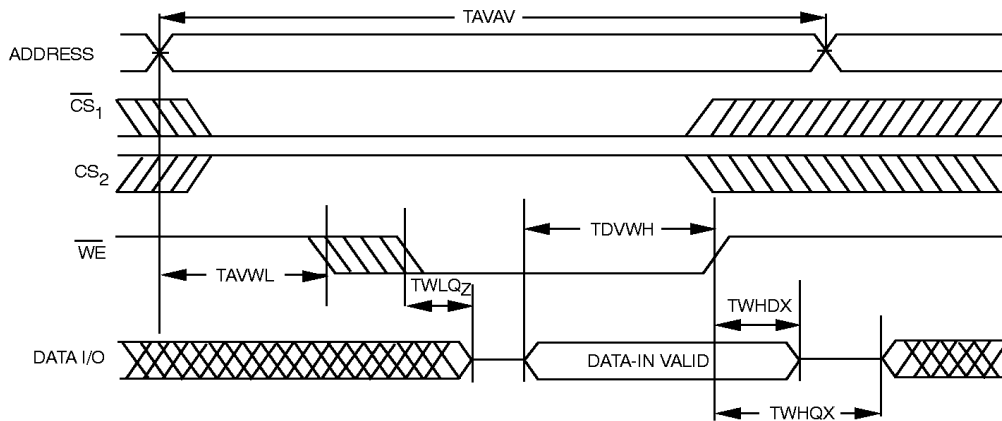
SYMBOL	PARAMETER	65608 – 30	65608 – 45	UNIT	VALUE
TAVAV	Read cycle time	30	45	ns	min
TAVQV	Address access time	30	45	ns	max
TAVQX	Address valid to low Z	5	5	ns	min
TE ₁ LQV	Chip-select ₁ access time	30	45	ns	max
TE ₁ LQX	\overline{CS}_1 low to low Z (11)	3	3	ns	min
TE ₁ HQZ	\overline{CS}_1 high to high Z (11)	18	20	ns	max
TE ₂ HQV	Chip-select ₂ access time	30	45	ns	max
TE ₂ HQX	CS ₂ high to low Z (11)	3	3	ns	min
TE ₂ LQZ	CS ₂ low to high Z (11)	18	20	ns	max
TGLQV	Output Enable access time	12	15	ns	max
TGLQX	\overline{OE} low to low Z (11)	0	0	ns	min
TGHQZ	\overline{OE} high to high Z (11)	8	15	ns	max

Notes : 11. Parameters guaranteed, not tested, with output loading 5 pF. (see fig. 1.b.).

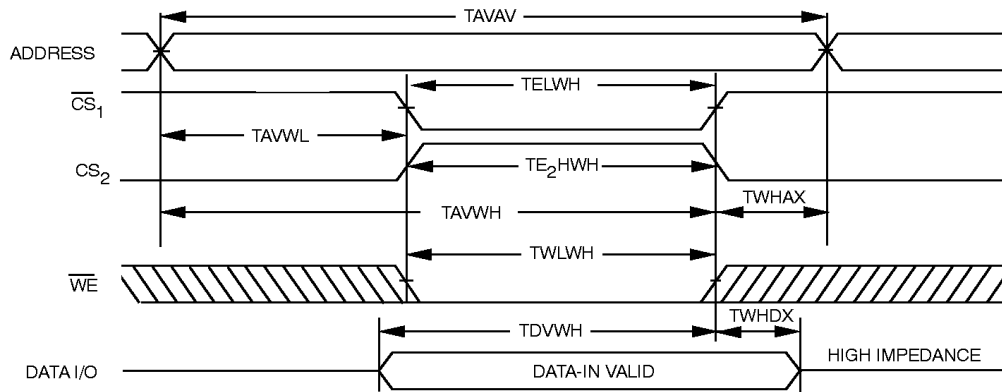
Write Cycle 1. \overline{W} Controlled. \overline{OE} High During Write



Write Cycle 2. \overline{W} Controlled. \overline{OE} Low

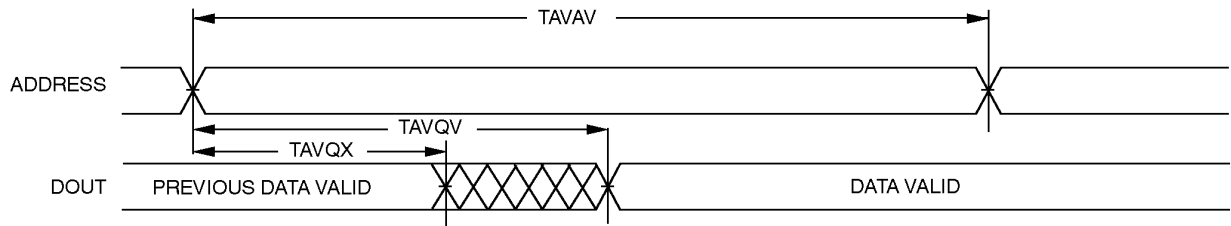


Write Cycle 3. \overline{CS}_1 or \overline{CS}_2 Controlled.

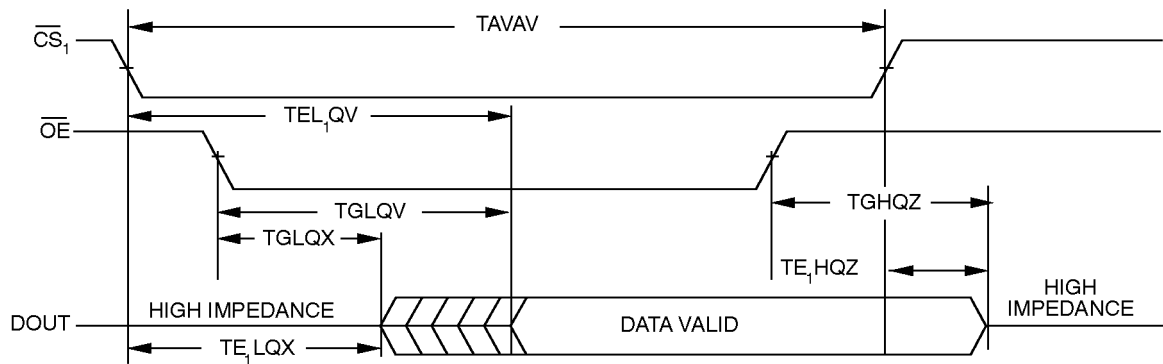


Note : 12. The internal write time of the memory is defined by the overlap of \overline{CS}_1 Low and \overline{CS}_2 HIGH and \overline{WE} LOW. Both signals must be activated to initiate a write and either signal can terminate a write by going in activated. The data input setup and hold timing should be referenced to the activated edge of the signal that terminates the write. Data out is high impedance if $\overline{OE} = \overline{VIH}$.

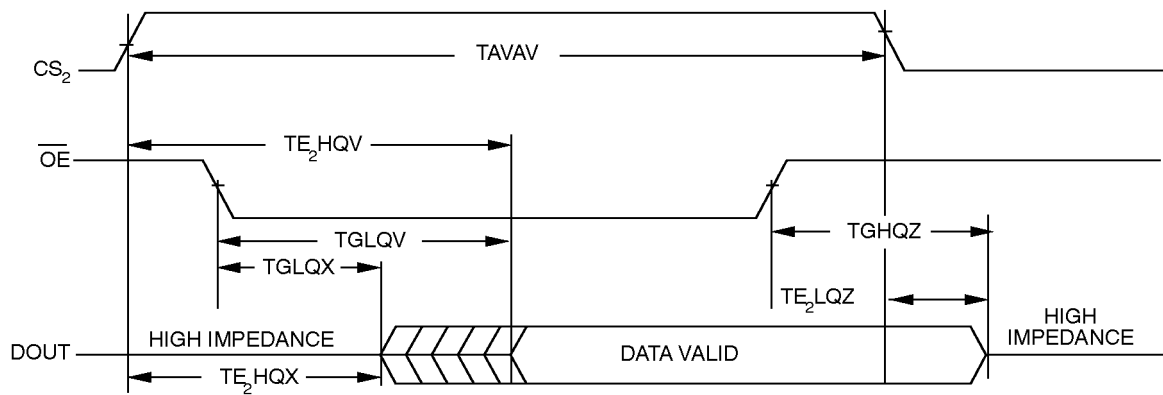
Read Cycle nb 1



Read Cycle nb 2



Read Cycle nb 3



Ordering Information

TEMPERATURE RANGE	PACKAGE	DEVICE	GRADE	SPEED	FLOW*	
M	M	DJ	- 65608E	V	- 45	/883
M = Military S = Space	-55° to +125°C -55° to +125°C			V = Very low power	30 ns 45 ns	
	C9 = Side Brazed 32 pins 400 mils DJ = Flat Package 32 pins 400 mils 0 = die					
		128K × 8 STATIC RAM			blank = MHS standards /883 = MIL-STD 883 Class B or S SB/SC = SCC 9000 level B/C	

* For ordering in QML quality level, use the QML PIN according to SMD n° 5962–89598.

The information contained herein is subject to change without notice. No responsibility is assumed by TEMIC for using this publication and/or circuits described herein : nor for any possible infringements of patents or other rights of third parties which may result from its use.