mosaic

Mosaic Semiconductor Inc.

1 Meg x 1 CMOS SRAM

Issue 1.1 : June 1992

MSM11000-35/45/55

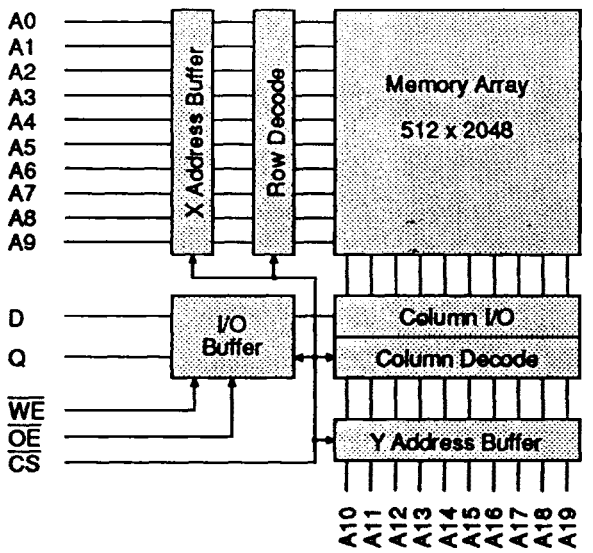
ADVANCE PRODUCT INFORMATION

1,048,576 x 1 CMOS High Speed Static RAM

Features

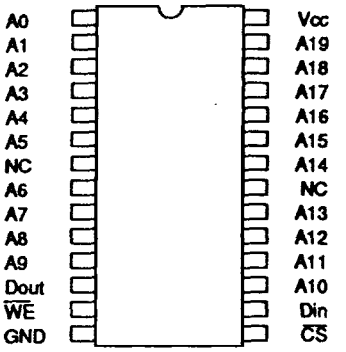
- Fast Access Times of 35,45,55 ns
- JEDEC Standard 28 Pin Footprint
- VIL™ High Density Package Available
- Low Power Standby 500µW (typ.)-L Version
- Low Power Operation 600mW(typ.)
- Completely Static Operation
- Separate Inputs and Outputs
- Equal Access and Cycle Times
- Battery Back-up Version Available
- Directly TTL Compatible
- May be processed to MIL-STD-883, non-compliant

Block Diagram

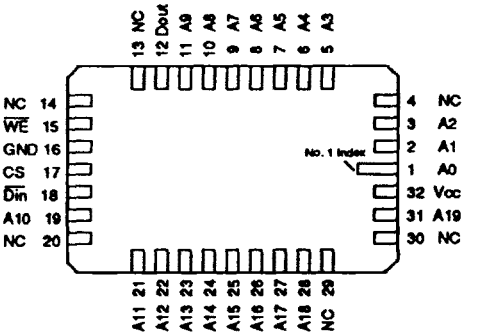


Pin Definition

Package Type: 'K','V','G','W','J'



Package Type: 'WX','JX'



Pin Functions

A0-A19	Address Inputs
Din	Data Input
Dout	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
NC	No Connect
V_{CC}	Power (+5V)
GND	Ground

Package Details Package details and dimensions on page 6,7.

Pin Count	Description	Package Type	Material	Pin Out
28	0.4" Dual-in-Line (DIP)	K	Ceramic	JEDEC
28	0.1" Vertical-in-Line (VIL™)	V	Ceramic	JEDEC
28	Bottom Brazed Flatpack	G	Ceramic	JEDEC
32	Extended Leadless Chip Carrier (LCC)	WX	Ceramic	ASIC
28	Leadless Small Outline Package	W(TBD)	Ceramic	JEDEC
32	'J' Leaded Chip Carrier (JLCC)	JX	Ceramic	ASIC
28	Small Outline 'J' Bend (SOJ)	J(TBD)	Ceramic	JEDEC

Absolute Maximum Ratings

Voltage on any pin relative to V_{ss}	V_t	-0.5* to +7	V
Power Dissipation	P_t	1.0	W
Storage Temperature	T_{stg}	-55 to +150	°C

Note: V_{IL} min. = -2.0V pulse of less than 10ns.

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Operating Temperature	T_a	0	-	70	°C
	T_{ai}	-40	-	85	°C (11000I)
	T_{am}	-55	-	125	°C (11000M, 11000MB)

DC Electrical Characteristics

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI}	V_{IN}=0V to V_{CC}	-	-	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=Gnd to V_{CC}	-	-	2	µA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA, Min. Cycle, Duty=100%	-	-	120	mA
Standby Current	I_{SB}	$\overline{CS}$=V_{IH}, I/P's static	-	-	40	mA
	I_{SBL1}*	$\overline{CS}$≥V_{CC}-0.2V, I/P's<0.2V or ≥Vcc-0.2V	-	-	2	mA
-L Version	I_{SB1}*	CMOS Levels	-	-	100	µA
Output Voltage	V_{OL}	I_{OL}=8.0mA	-	-	0.4	V
	V_{OH}	I_{OH}=-4.0mA	2.4	-	-	V

Typical values are at V_{CC}=5.0V, T_a=25°C and specified loading.
*Vil min =-0.3V

Capacitance (V_{CC}=5V±10%, T_a=25°C)

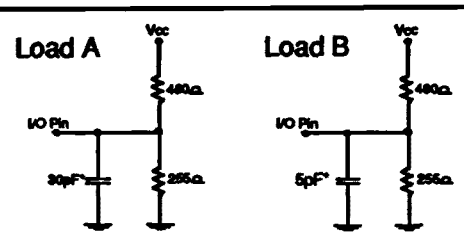
Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance:	C_{IN}	V_{IN}=0V	-	6	pF
I/O Capacitance:	$C_{I/O}$	$V_{I/O}$=0V	-	10	pF

Note: This parameter is guaranteed, not tested.

AC Test Conditions

* Input pulse levels: GND to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* V_{CC}=5V±10%

Output Load Circuit

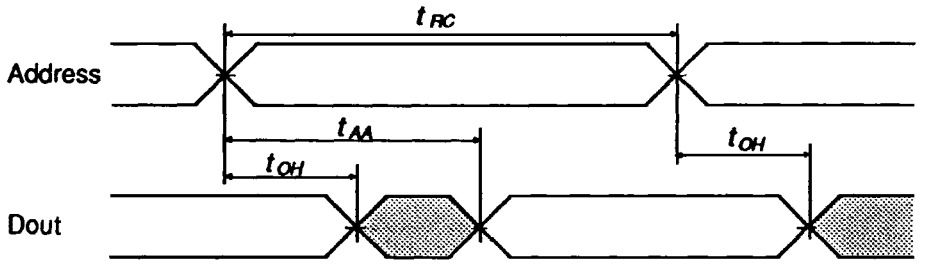


*Including jig and fixture

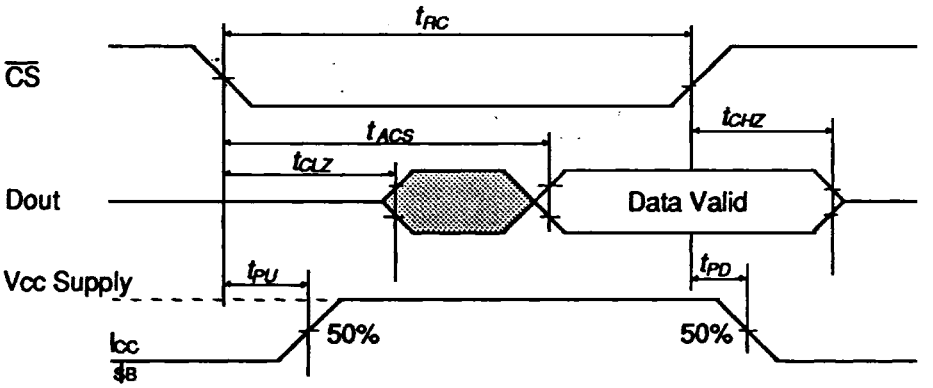
Read Cycle Timing

Parameter	Symbol	-35 min	-35 max	-45 min	-45 max	-55 min	-55 max	Unit	Note
Read Cycle Time	t_{RC}	35	-	45	-	55	-	ns	
Address Access Time	t_{AA}	-	35	-	45	-	55	ns	
Chip Select Access Time	t_{ACS}	-	35	-	45	-	55	ns	
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	ns	
Chip Selection to Output in Low Z	t_{CLZ}	5	-	5	-	5	-	ns	1
Chip Deselection to Output in High Z	t_{CHZ}	0	15	0	20	-	25	ns	1
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	0	-	ns	5
Chip Deselection to Power Down Time	t_{PD}	-	25	-	30	-	35	ns	5

Read Cycle Timing Waveform(1) (1,2)



Read Cycle Timing Waveform (2) (2,4)



Notes:

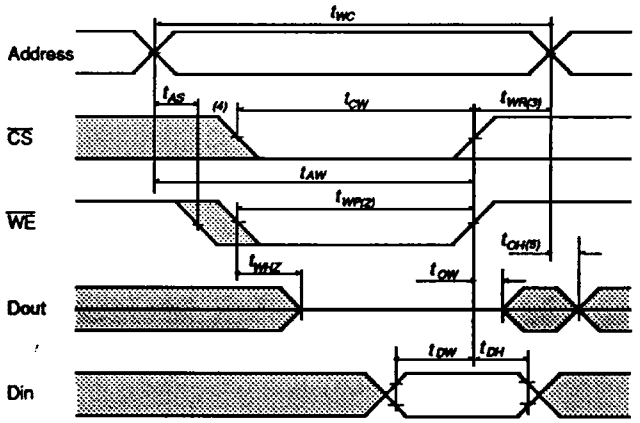
1. Transition is measured +/-200mV from steady voltage with Load B. This parameter is guaranteed and not 100% tested.
2. $\overline{WE}$ is High for Read Cycle.
3. Device is continuously selected, $\overline{CS}$=V_{IL}.
4. Address valid prior to or coincident with $\overline{CS}$ transition Low.
5. These parameters are guaranteed, and not 100% tested.

Write Cycle Timing

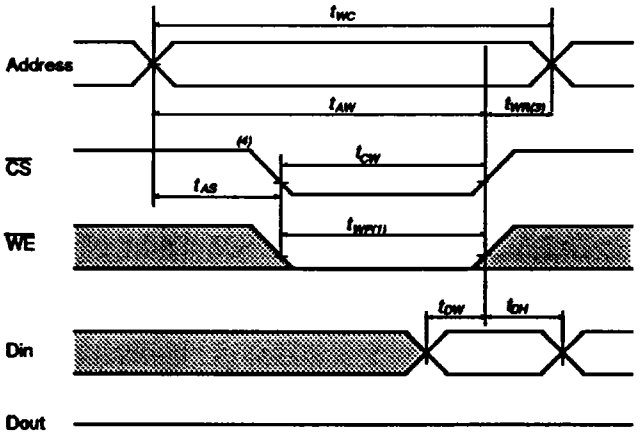
Parameter	Symbol	-35 min	-35 max	-45 min	-45 max	-55 min	-55 max	Unit	Note
Write Cycle Time	t_{WC}	35	-	45	-	55	-	ns	
Chip Selection to End of Write	t_{CW}	25	-	40	-	50	-	ns	
Address Valid to End of Write	t_{AW}	30	-	40	-	50	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns	
Write Pulse Width	t_{WP}	25	-	35	-	45	-	ns	
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns	
Write to Output in High Z	t_{WHZ}	0	20	0	25	0	30	ns	1
Data to Write Time Overlap	t_{DW}	20	-	25	-	30	-	ns	
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns	
Output Active from End of Write	t_{OW}	0	-	0	-	0	-	ns	1

Notes:
1. Transition is measured +/- 200mV from steady state voltage with Load B. This parameter is guaranteed and not 100% tested.

Write Cycle No.1 Timing Waveform (WE Controlled)



Write Cycle No.2 Timing Waveform (CS Controlled)



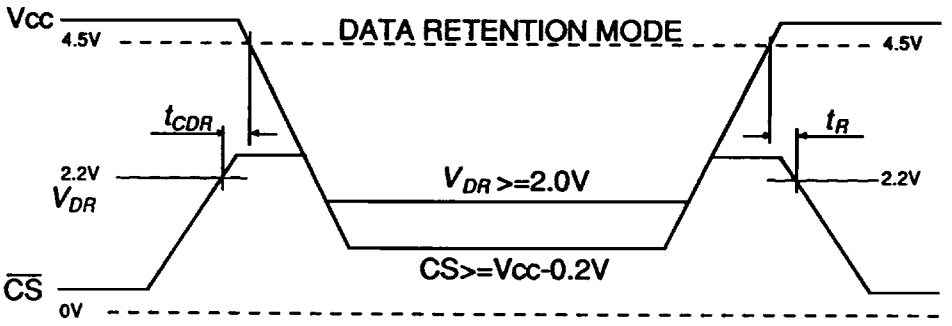
Notes:
1. Transition is measure +/-200mV from high impedance voltage with load B. This parameter is not 100% tested.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
5. Dout is in the same phase as written data of this write cycle.

Low V_{cc} Data Retention Characteristics - L Version Only (T_a = 0 to 70°C)

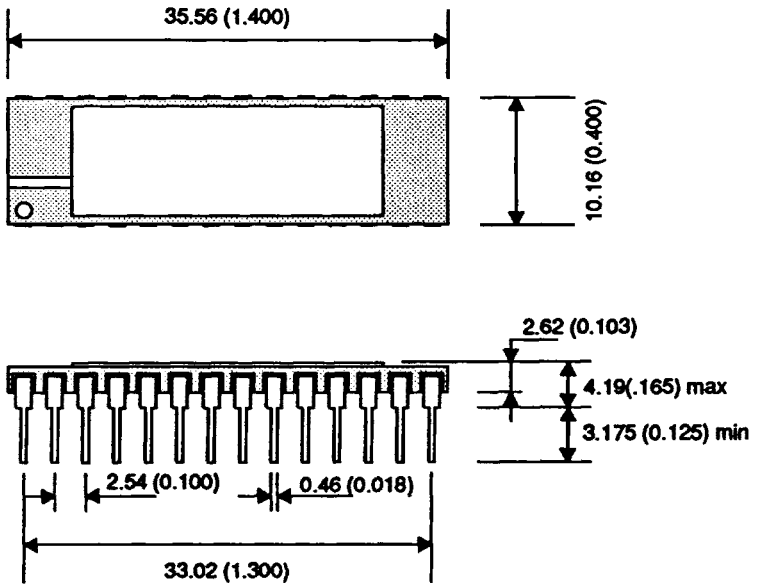
Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Vcc for Data Retention	V_{DR}	$\overline{CS}$>=V_{CC}-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR}	V_{CC}=3.0V, $\overline{CS}$≥V_{CC}-0.2 T_{op}=T_a	-	2	100**	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

Notes: **V_{CC}=3.0V

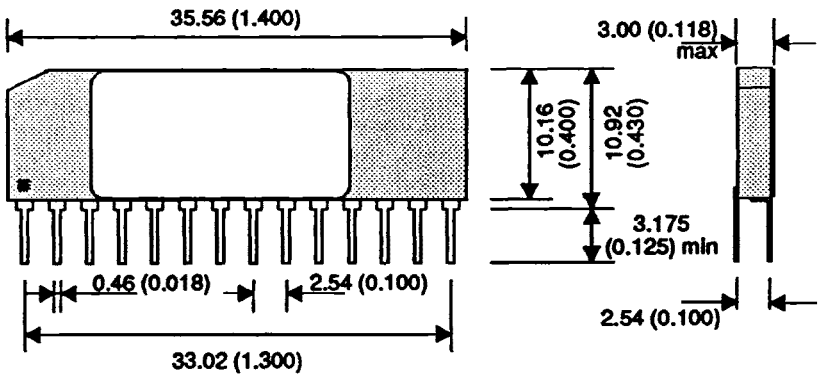
Low V_{CC} Data Retention Timing Waveform



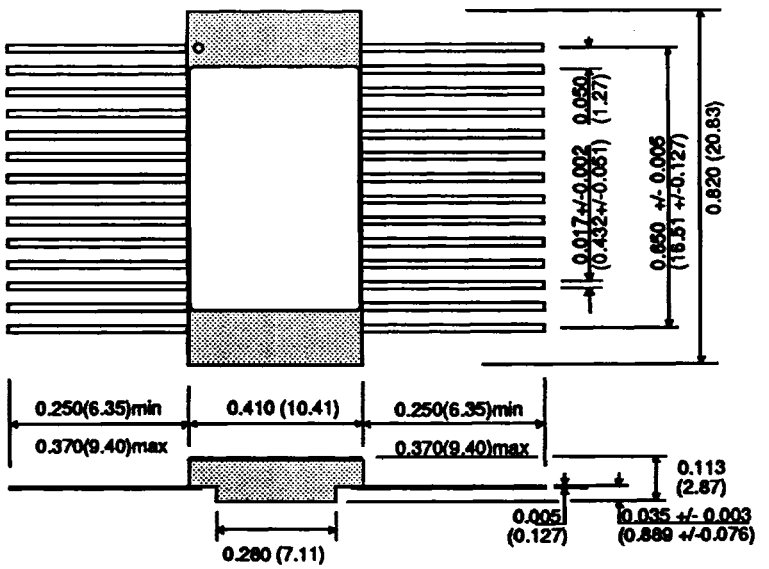
28 Pin 0.4" Dual-In-Line (DIP) - 'K' Package



28 Pin 0.1" Vertical-In-Line (VIL™) - 'V' Package

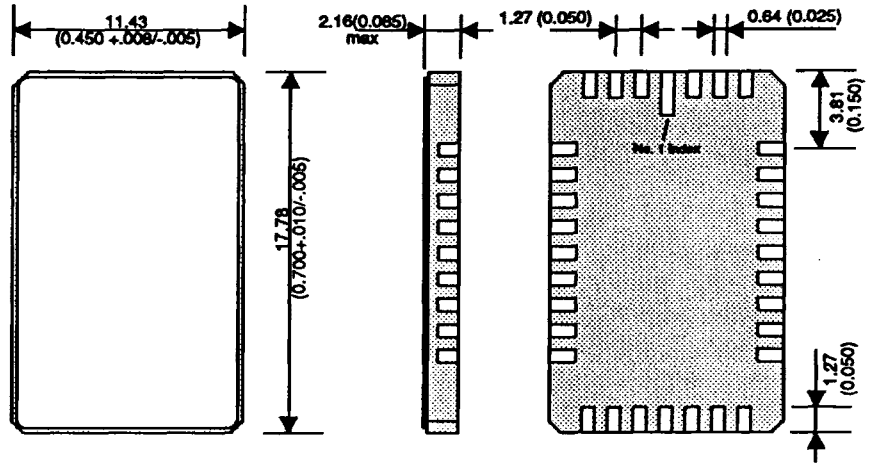


28 Pin Ceramic Flatpack - 'G' Package

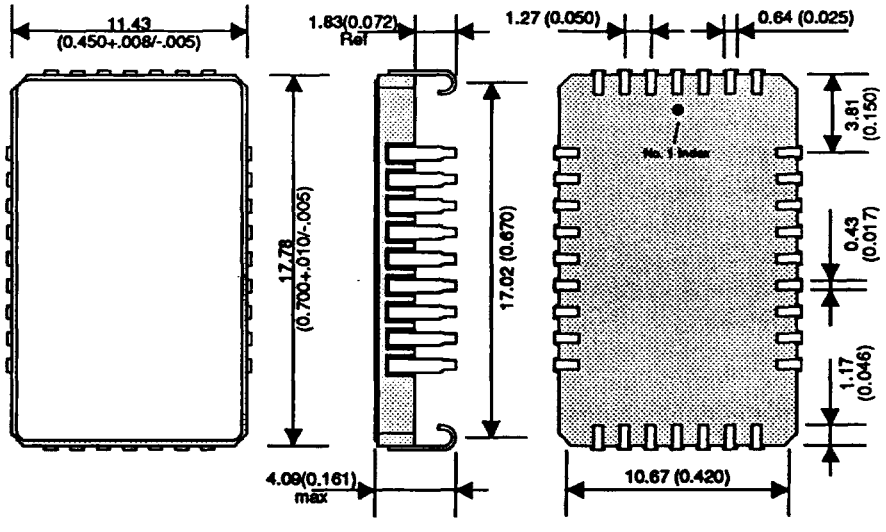


All dimensions imn mm (inches). Tolerance on all dimensions +/-0.254(0.010).

32 Pad Extended Leadless Chip Carrier (LCC) - 'WX' Package



32 Pin Extended 'J'Leaded Chip Carrier (JLCC) - 'JX' Package



Military Screening Procedure

Component Screening Flow for high reliability non-compliant product processed to MIL-STD883 Method 5004 is detailed below:

MB COMPONENT SCREENING FLOW		
SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
High-temperature storage	1008 Condition C (24hrs @ 150 °C)	100%
Temperature Cycle	1010 Condition C (10 Cycles, -65 °C to 150°C)	100%
Constant acceleration	2001 Condition E (Y axis only), (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specification @ Ta+25°C	100%
Final Electrical Tests	Per applicable device specification	
Static (dc)	a) @ Ta=25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ Ta=25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ Ta=25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective Allowable(PDA)	Calculated at post-burn-in @ Ta=25°C	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

MSM11000KLMB -45

Speed	35,45,55 ns	
Temp. Range/Screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military.
	MB	= Processed to MIL-STD 883 Method 5004, non-compliant
Power Consumption	Blank	= Standard Power Part
	L	= Low Power Part
Package	K	= 28 Pin 400 mil DIP
	V	= 28 Pin 100 mil VIL
	G	= 28 Pin Ceramic Flatpack
	WX	= 32 Pad Extended LCC
	W	= 28 Pad Leadless SOJ
	JX	= 32 Pin Extended JLCC
	J	= 28 Pin CSOJ

mosaic
Mosaic Semiconductor Inc.
7420 Carroll Road
San Diego, CA 92121
Tel: (619) 271 4565
FAX: (619) 271 6058