256K x 36, 512K x 18 Smart ZBT™ 3.3V Synchronous SRAMs 3.3V I/O, Burst Counter Pipelined Outputs

Preliminary
IDT71V66603
IDT71V66803

Features

- **256K x 36, 512K x 18 memory configurations**
- **Supports high performance system speed - from 66MHz to 133MHz**
- **ZBT™ Feature - No dead cycles between write and read cycles**
- **Smart ZBT™ Feature - Eases system timing requirements and reduces the likelihood of bus contention**
- **With Smart ZBT™ the output turn-on (t_{CLZ}) is adaptable to the user's system and is a function of the cycle time**
- **Backward compatible with IDT's existing ZBT offerings**
- **User selectable Smart ZBT™ or Original ZBT™ mode pin ($\overline{M}$s)**
- **Internally synchronized output buffer enable eliminates the need to control $\overline{OE}$**
- **Single R/$\overline{W}$ (READ/WRITE) control pin**
- **Positive clock-edge triggered address, data, and control signal registers for fully pipelined applications**
- **4-word burst capability (interleaved or linear)**
- **Individual byte write ($\overline{BW}_1$ - $\overline{BW}_4$) control (May tie active)**
- **Three chip enables for simple depth expansion**
- **3.3V power supply (±5%)**
- **3.3V I/O Supply (V_{DDQ})**
- **Power down controlled by ZZ input**
- **Packaged in a JEDEC standard 100-pin plastic thin quad flatpack (TQFP) and 119 ball grid array (BGA).**

Description

The IDT71V66603/66803 are 3.3V high-speed 9,437,184-bit (9 Megabit) synchronous SRAMs. They are designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus, they have been given the name ZBT™, or Zero Bus Turnaround.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later the associated data cycle occurs, be it read or write.

The IDT71V66603/66803 offer the user a Smart functionality which simplifies system timing requirements when turning the bus around between writes and reads. Traditionally, SRAMs are designed with fast turn-on times (t_{CLZ}) in order to meet the requirements of high-speed applications. This fast turn-on may lead to bus contention at slower speeds, i.e. 133 MHz and slower, since these designs often use less aggressive ASICs/controllers with loose turn-off parameters (t_{CHZ}). Thus at slower speeds, more margin on the RAM's t_{CLZ} may be needed to compensate for the slow turn-off of the ASIC/controller. The IDT71V66603/66803 have the ability to provide this extra margin by allowing t_{CLZ} to adapt to the user's system.

With the Smart ZBT™ feature, the output turn-on time (t_{CLZ}) adapts to the user's system and is solely a function of cycle time (t_{CYC}). Thus with Smart ZBT™, t_{CLZ} is independent of process, voltage, and temperature variations. With this deterministic output turn-on feature, the guesswork of when the SRAM begins to drive the bus is removed, therefore easing system timing requirements. The Smart feature allows the turn-on time of the ZBT™ SRAM output drivers (t_{CLZ}) to adapt to match the requirements of the system.

Pin Description Summary

A_0-A_{18}	Address Inputs	Input	Synchronous
$\overline{CE}_1$, CE_2, $\overline{CE}_2$	Chip Enables	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
R/$\overline{W}$	Read/Write Signal	Input	Synchronous
$\overline{CEN}$	Clock Enable	Input	Synchronous
$\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
ADV/$\overline{LD}$	Advance burst address / Load new address	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	Static
TMS	Test Mode Select	Input	N/A
TDI	Test Data Input	Input	N/A
TCK	Test Clock	Input	N/A
TDO	Test Data Output	Output	N/A
ZZ	Sleep Mode	Input	Asynchronous
I/O_0-I/O_{31}, I/O_{P1}-I/O_{P4}	Data Input / Output	I/O	Synchronous
V_{DD}, V_{DDQ}	Core Power, I/O Power	Supply	Static
V_{SS}	Ground	Supply	Static

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Description (cont.)

The IDT71V66603/66803 contain data I/O, address and control signal registers. Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

A Clock Enable ($\overline{CEN}$) pin allows operation of the IDT71V66603/66803 to be suspended as long as necessary. All synchronous inputs are ignored when $\overline{CEN}$ is high and the internal device registers will hold their previous values.

There are three chip enable pins ($\overline{CE}_1$, CE_2, $\overline{CE}_2$) that allow the user to deselect the device when desired. If any one of these three is not asserted when ADV/$\overline{LD}$ is low, no new memory operation can be initiated. However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state two cycles after the chip is deselected or a write is initiated.

The IDT71V66603/66803 have an on-chip burst counter. In the burst mode, the IDT71V66603/66803 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the $\overline{LBO}$ input pin. The $\overline{LBO}$ pin selects between linear and interleaved burst sequence. The ADV/$\overline{LD}$ signal is used to load a new external address (ADV/$\overline{LD}$ = LOW) or increment the internal burst counter (ADV/$\overline{LD}$ = HIGH).

The IDT71V66603/66803 SRAMs utilize IDT's latest high-performance CMOS process, and are packaged in a JEDEC Standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) as well as a 119 ball grid array (BGA).

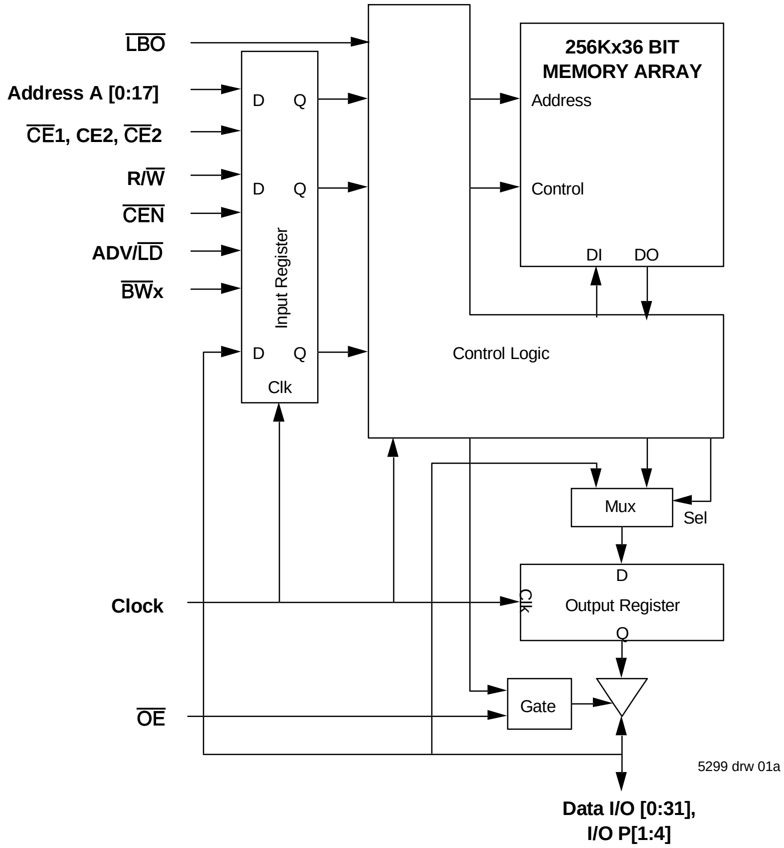
Pin Definitions[(1)]

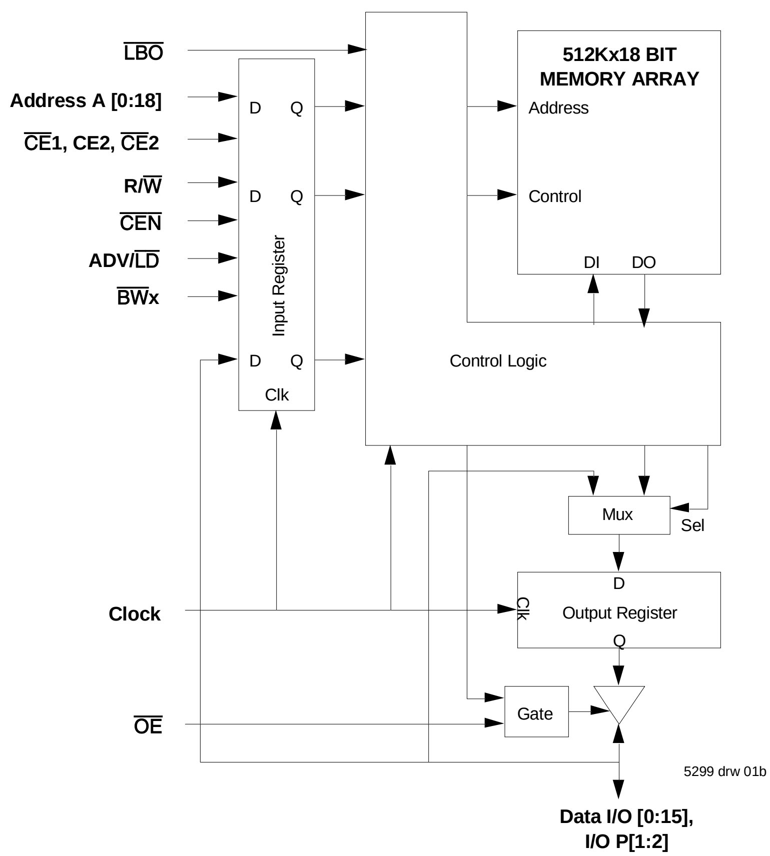
Symbol	Pin Function	I/O	Active	Description
A_0-A_{18}	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, ADV/$\overline{LD}$ low, $\overline{CEN}$ low, and true chip enables.
ADV/$\overline{LD}$	Advance / Load	I	N/A	ADV/$\overline{LD}$ is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/$\overline{LD}$ is low with the chip deselected, any burst in progress is terminated. When ADV/$\overline{LD}$ is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/$\overline{LD}$ is sampled high.
R/$\overline{W}$	Read / Write	I	N/A	R/$\overline{W}$ signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place two clock cycles later.
$\overline{CEN}$	Clock Enable	I	LOW	Synchronous Clock Enable Input. When $\overline{CEN}$ is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of $\overline{CEN}$ sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, $\overline{CEN}$ must be sampled low at rising edge of clock.
$\overline{BW}_1$-$\overline{BW}_4$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. Each 9-bit byte has its own active low byte write enable. On load write cycles (when R/$\overline{W}$ and ADV/$\overline{LD}$ are sampled low) the appropriate byte write signal ($\overline{BW}_1$-$\overline{BW}_4$) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/$\overline{W}$ is sampled high. The appropriate byte(s) of data are written into the device two cycles later. $\overline{BW}_1$-$\overline{BW}_4$ can all be tied low if always doing write to the entire 36-bit word.
$\overline{CE}_1$, $\overline{CE}_2$	Chip Enables	I	LOW	Synchronous active low chip enable. $\overline{CE}_1$ and $\overline{CE}_2$ are used with CE_2 to enable the IDT71V66603/66803 ($\overline{CE}_1$ or $\overline{CE}_2$ sampled high or CE_2 sampled low) and ADV/$\overline{LD}$ low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a two cycle deselect, i.e., the data bus will tri-state two clock cycles after deselect is initiated.
CE_2	Chip Enable	I	HIGH	Synchronous active high chip enable. CE_2 is used with $\overline{CE}_1$ and $\overline{CE}_2$ to enable the chip. CE_2 has inverted polarity but otherwise identical to $\overline{CE}_1$ and $\overline{CE}_2$.
CLK	Clock	I	N/A	This is the clock input to the IDT71V66603/66803. Except for $\overline{OE}$, all timing references for the device are made with respect to the rising edge of CLK.
I/O_0-I/O_{31} I/O_{P1}-I/O_{P4}	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
$\overline{LBO}$	Linear Burst Order	I	LOW	Burst order selection input. When $\overline{LBO}$ is high the Interleaved burst sequence is selected. When $\overline{LBO}$ is low the Linear burst sequence is selected. $\overline{LBO}$ is a static input and it must not change during device operation.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. $\overline{OE}$ must be low to read data from the IDT71V66603/66803. When $\overline{OE}$ is high the I/O pins are in a high-impedance state. $\overline{OE}$ does not need to be actively controlled for read and write cycles. In normal operation, $\overline{OE}$ can be tied low.
TMS	Test Mode Select	I	N/A	Gives input command for TAP controller; sampled on rising edge of TCK.
TDI	Test Data Input	I	N/A	Serial input of registers placed between TDI and TDO. Sampled on rising edge of TCK.
TCK	Test Clock	I	N/A	Clock input of TAP controller. Each TAP event is clocked. Test inputs are captured on rising edge of TCK, while test outputs are driven from falling edge of TCK.
TDO	Test Data Output	O	N/A	Serial output of registers placed between TDI and TDO. This output is active depending on the state of the TAP controller.
ZZ	Sleep Mode	I	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V66603/66803 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.
V_{DD}	Power Supply	N/A	N/A	3.3V core power supply.
V_{DDQ}	Power Supply	N/A	N/A	3.3V I/O Supply.
V_{SS}	Ground	N/A	N/A	Ground.

5299 tbl 02

NOTE:
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Functional Block Diagram





Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V_{DDQ}	I/O Supply Voltage	3.135	3.3	3.465	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage - Inputs	2.0	—	V_{DD}+0.3	V
V_{IH}	Input High Voltage - I/O	2.0	—	V_{DDQ}+0.3	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.8	V

5299 tbl 04

NOTE:
1. V_{IL} (min.) = –1.0V for pulse width less than t_{CYC}/2, once per cycle.

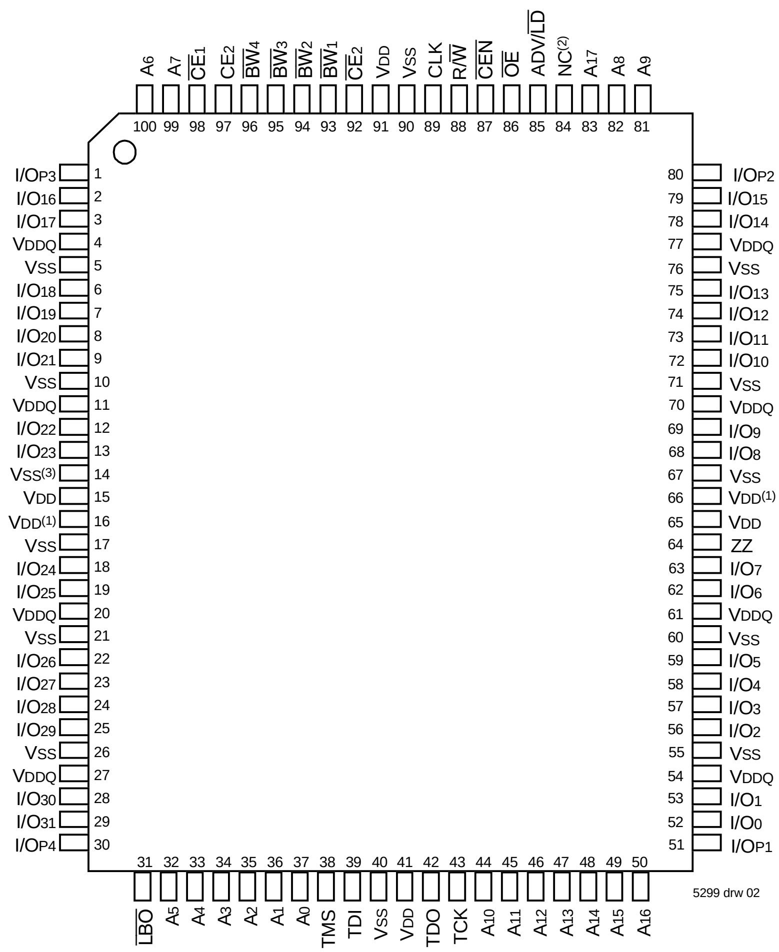
Recommended Operating Temperature and Supply Voltage

Grade	Temperature(1)	Vss	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	0V	3.3V±5%	3.3V±5%

5299 tbl 05

NOTE:
1. T_A is the "instant on" case temperature.

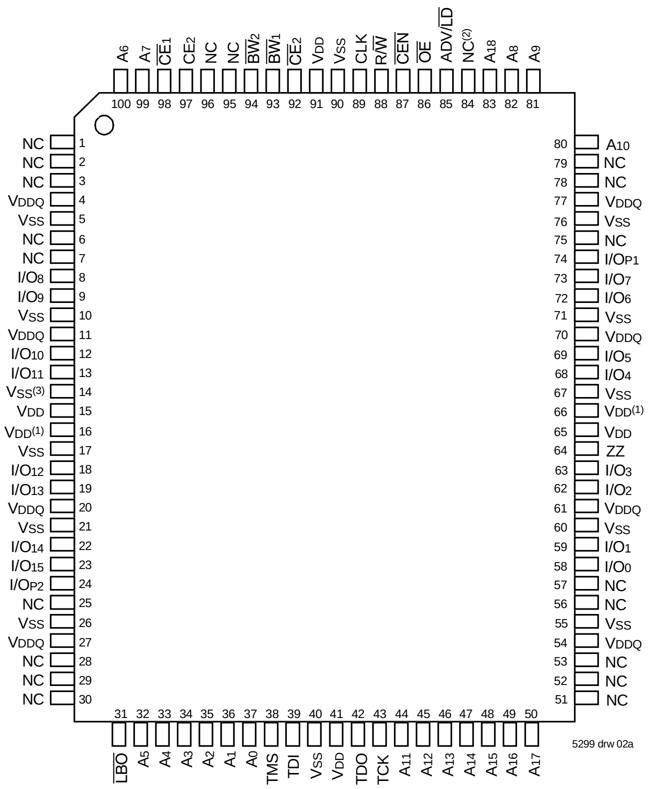
Pin Configuration — 256K x 36



Top View
100 TQFP

NOTES:
1. Pins 16 and 66 do not have to be connected directly to V_{DD} as long as the input voltage is ≥ V_{IH}.
2. Pin 84 is reserved for a future 16M.
3. Pin 14 does not have to be connected directly to Vss as long as the input voltage is $V \leq V_{IL}$.

Pin Configuration — 512K x 18



Top View
100 TQFP

NOTES:
1. Pins 16 and 66 do not have to be connected directly to VDD as long as the input voltage is ≥ VIH.
2. Pin 84 is reserved for a future 16M.
3. Pin 14 does not have to be connected directly to VSS as long as the input voltage is ≤ VIL.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial	Unit
VTERM(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM(3,6)	Terminal Voltage with Respect to GND	-0.5 to VDD	V
VTERM(4,6)	Terminal Voltage with Respect to GND	-0.5 to VDD +0.5	V
VTERM(5,6)	Terminal Voltage with Respect to GND	-0.5 to VDDQ +0.5	V
TA(7)	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
PT	Power Dissipation	2.0	W
IOUT	DC Output Current	50	mA

5299 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VDD terminals only.
3. VDDQ terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed VDDQ during power supply ramp up.
7. TA is the "instant on" case temperature.

100 TQFP Capacitance
(TA = +25°C, f = 1.0MHz, TQFP Package)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	5	pF
CI/O	I/O Capacitance	VOUT = 3dV	7	pF

5299 tbl 07

119 BGA Capacitance
(TA = +25°C, f = 1.0MHz, TQFP Package)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	7	pF
CI/O	I/O Capacitance	VOUT = 3dV	7	pF

5299 tbl 07a

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

Pin Configuration — 256K X 36, 119 BGA(1,2,3)

	1	2	3	4	5	6	7
A	V_{DDQ}	A6	A4	NC(2)	A8	A16	V_{DDQ}
B	NC	CE2	A3	ADV/$\overline{\text{LD}}$	A9	$\overline{\text{CE}}_2$	NC
C	NC	A7	A2	V_{DD}	A12	A15	NC
D	I/O16	I/OP3	V_{SS}	NC	V_{SS}	I/OP2	I/O15
E	I/O17	I/O18	V_{SS}	$\overline{\text{CE}}_1$	V_{SS}	I/O13	I/O14
F	V_{DDQ}	I/O19	V_{SS}	$\overline{\text{OE}}$	V_{SS}	I/O12	V_{DDQ}
G	I/O20	I/O21	$\overline{\text{BW}}_3$	A17	$\overline{\text{BW}}_2$	I/O11	I/O10
H	I/O22	I/O23	V_{SS}	R/$\overline{\text{W}}$	V_{SS}	I/O9	I/O8
J	V_{DDQ}	V_{DD}	V_{DD}(1)	V_{DD}	V_{DD}(1)	V_{DD}	V_{DDQ}
K	I/O24	I/O26	V_{SS}	CLK	V_{SS}	I/O6	I/O7
L	I/O25	I/O27	$\overline{\text{BW}}_4$	NC	$\overline{\text{BW}}_1$	I/O4	I/O5
M	V_{DDQ}	I/O28	V_{SS}	$\overline{\text{CEN}}$	V_{SS}	I/O3	V_{DDQ}
N	I/O29	I/O30	V_{SS}	A1	V_{SS}	I/O2	I/O1
P	I/O31	I/OP4	V_{SS}	A0	V_{SS}	I/O0	I/OP1
R	NC	A5	$\overline{\text{LBO}}$	V_{DD}	V_{SS}(4)	A13	NC
T	NC	NC	A10	A11	A14	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	DNU(3)	V_{DDQ}

5299 drw 13a

Top View

Pin Configuration — 512K X 18, 119 BGA(1,2,3)

	1	2	3	4	5	6	7
A	V_{DDQ}	A6	A4	NC(2)	A8	A16	V_{DDQ}
B	NC	CE2	A3	ADV/$\overline{\text{LD}}$	A9	$\overline{\text{CE}}_2$	NC
C	NC	A7	A2	V_{DD}	A13	A17	NC
D	I/O8	NC	V_{SS}	NC	V_{SS}	I/O7	NC
E	NC	I/O9	V_{SS}	$\overline{\text{CE}}_1$	V_{SS}	NC	I/O6
F	V_{DDQ}	NC	V_{SS}	$\overline{\text{OE}}$	V_{SS}	I/O5	V_{DDQ}
G	NC	I/O10	$\overline{\text{BW}}_2$	A18	V_{SS}	NC	I/O4
H	I/O11	NC	V_{SS}	R/$\overline{\text{W}}$	V_{SS}	I/O3	NC
J	V_{DDQ}	V_{DD}	V_{DD}(1)	V_{DD}	V_{DD}(1)	V_{DD}	V_{DDQ}
K	NC	I/O12	V_{SS}	CLK	V_{SS}	NC	I/O2
L	I/O13	NC	V_{SS}	NC	$\overline{\text{BW}}_1$	I/O1	NC
M	V_{DDQ}	I/O14	V_{SS}	$\overline{\text{CEN}}$	V_{SS}	NC	V_{DDQ}
N	I/O15	NC	V_{SS}	A1	V_{SS}	I/O0	NC
P	NC	I/OP2	V_{SS}	A0	V_{SS}	NC	I/OP1
R	NC	A5	$\overline{\text{LBO}}$	V_{DD}	V_{SS}(4)	A12	NC
T	NC	A10	A15	NC	A14	A11	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	DNU(3)	V_{DDQ}

5299 drw 13b

Top View

NOTES:

1. J3 and J5 do not have to be directly connected to V_{DD} as long as the input voltage is ≥ V_{IH}.
2. A4 is reserved for future 16M.
3. DNU = Do not use; Pin U6 is reserved for asynchronous JTAG reset $\overline{\text{TRST}}$ on future revisions.
4. R5 does not have to be connected directly to V_{SS} as long as the input voltage is ≤ V_{IL}.

Synchronous Truth Table(1)

$\overline{CEN}$	R/$\overline{W}$	Chip(5) Enable	ADV/$\overline{LD}$	$\overline{BW}$x	ADDRESS USED	PREVIOUS CYCLE	CURRENT CYCLE	I/O (2 cycles later)
L	L	Select	L	Valid	External	X	LOAD WRITE	D(7)
L	H	Select	L	X	External	X	LOAD READ	Q(7)
L	X	X	H	Valid	Internal	LOAD WRITE / BURST WRITE	BURST WRITE (Advance burst counter)(2)	D(7)
L	X	X	H	X	Internal	LOAD READ / BURST READ	BURST READ (Advance burst counter)(2)	Q(7)
L	X	Deselect	L	X	X	X	DESELECT or STOP(3)	HiZ
L	X	X	H	X	X	DESELECT / NOOP	NOOP	HiZ
H	X	X	X	X	X	X	SUSPEND(4)	Previous Value

5299 tbl 08

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. When ADV/$\overline{LD}$ signal is sampled high, the internal burst counter is incremented. The R/$\overline{W}$ signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/$\overline{W}$ signal when the first address is loaded at the beginning of the burst cycle.
3. Deselect cycle is initiated when either ($\overline{CE}_1$, or $\overline{CE}_2$ is sampled high or CE_2 is sampled low) and ADV/$\overline{LD}$ is sampled low at rising edge of clock. The data bus will tri-state two cycles after deselect is initiated.
4. When $\overline{CEN}$ is sampled high at the rising edge of clock, that clock edge is blocked from propogating through the part. The state of all the internal registers and the I/Os remains unchanged.
5. To select the chip requires $\overline{CE}_1$ = L, $\overline{CE}_2$ = L, CE_2 = H on these chip enables. Chip is deselected if any one of the chip enables is false.
6. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.
7. Q - Data read from the device, D - data written to the device.

Partial Truth Table for Writes(1)

OPERATION	R/$\overline{W}$	$\overline{BW}_1$	$\overline{BW}_2$	$\overline{BW}_3$(3)	$\overline{BW}_4$(3)
READ	H	X	X	X	X
WRITE ALL BYTES	L	L	L	L	L
WRITE BYTE 1 (I/O[0:7], I/OP1)(2)	L	L	H	H	H
WRITE BYTE 2 (I/O[8:15], I/OP2)(2)	L	H	L	H	H
WRITE BYTE 3 (I/O[16:23], I/OP3)(2,3)	L	H	H	L	H
WRITE BYTE 4 (I/O[24:31], I/OP4)(2,3)	L	H	H	H	L
NO WRITE	L	H	H	H	H

5299 tbl 09

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Multiple bytes may be selected during the same cycle.
3. N/A for X18 configuration.

Interleaved Burst Sequence Table ($\overline{LBO}$=VDD)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	1	0	0	1	0	0

5299 tbl 10

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

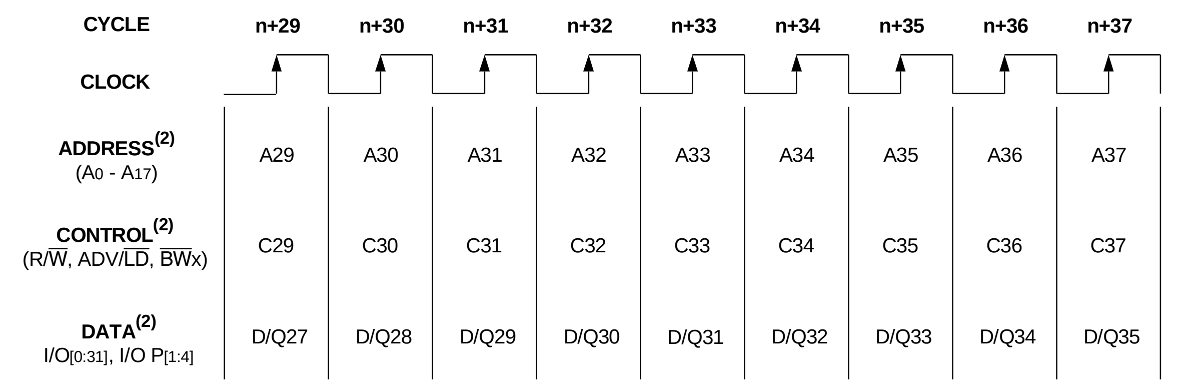
Linear Burst Sequence Table ($\overline{LBO}$=Vss)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	0	0	0	1	1	0

5299 tbl 11

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Functional Timing Diagram(1)



5299 drw 03

NOTES:
1. This assumes $\overline{CEN}$, $\overline{CE}_1$, CE_2, $\overline{CE}_2$ are all true.
2. All Address, Control and Data_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data_Out is valid after a clock-to-data delay from the rising edge of clock.

Device Operation - Showing Mixed Load, Burst, Deselect and NOOP Cycles(2)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(1)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Load read
n+1	X	X	H	X	L	X	X	X	Burst read
n+2	A_1	H	L	L	L	X	L	Q_0	Load read
n+3	X	X	L	H	L	X	L	Q_{0+1}	Deselect or STOP
n+4	X	X	H	X	L	X	L	Q_1	NOOP
n+5	A_2	H	L	L	L	X	X	Z	Load read
n+6	X	X	H	X	L	X	X	Z	Burst read
n+7	X	X	L	H	L	X	L	Q_2	Deselect or STOP
n+8	A_3	L	L	L	L	L	L	Q_{2+1}	Load write
n+9	X	X	H	X	L	L	X	Z	Burst write
n+10	A_4	L	L	L	L	L	X	D_3	Load write
n+11	X	X	L	H	L	X	X	D_{3+1}	Deselect or STOP
n+12	X	X	H	X	L	X	X	D_4	NOOP
n+13	A_5	L	L	L	L	L	X	Z	Load write
n+14	A_6	H	L	L	L	X	X	Z	Load read
n+15	A_7	L	L	L	L	L	X	D_5	Load write
n+16	X	X	H	X	L	L	L	Q_6	Burst write
n+17	A_8	H	L	L	L	X	X	D_7	Load read
n+18	X	X	H	X	L	X	X	D_{7+1}	Burst read
n+19	A_9	L	L	L	L	L	L	Q_8	Load write

5299 tbl 12

NOTES:
1. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.
2. H = High; L = Low; X = Don't Care; Z = High Impedance.

Read Operation(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	X	X	L	Q_0	Contents of Address A_0 Read Out

5299 tbl 13

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Burst Read Operation(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}x$	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	H	X	L	X	X	X	Clock Setup Valid, Advance Counter
n+2	X	X	H	X	L	X	L	Q_0	Address A_0 Read Out, Inc. Count
n+3	X	X	H	X	L	X	L	Q_{0+1}	Address A_{0+1} Read Out, Inc. Count
n+4	X	X	H	X	L	X	L	Q_{0+2}	Address A_{0+2} Read Out, Inc. Count
n+5	A_1	H	L	L	L	X	L	Q_{0+3}	Address A_{0+3} Read Out, Load A_1
n+6	X	X	H	X	L	X	L	Q_0	Address A_0 Read Out, Inc. Count
n+7	X	X	H	X	L	X	L	Q_1	Address A_1 Read Out, Inc. Count
n+8	A_2	H	L	L	L	X	L	Q_{1+1}	Address A_{1+1} Read Out, Load A_2

5299 tbl 14

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE_1}$ = L, $\overline{CE_2}$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE_1}$ = H, $\overline{CE_2}$ = H or CE_2 = L.

Write Operation(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}x$	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	L	X	X	D_0	Write to Address A_0

5299 tbl 15

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE_1}$ = L, $\overline{CE_2}$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE_1}$ = H, $\overline{CE_2}$ = H or CE_2 = L.

Burst Write Operation(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}x$	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	H	X	L	L	X	X	Clock Setup Valid, Inc. Count
n+2	X	X	H	X	L	L	X	D_0	Address A_0 Write, Inc. Count
n+3	X	X	H	X	L	L	X	D_{0+1}	Address A_{0+1} Write, Inc. Count
n+4	X	X	H	X	L	L	X	D_{0+2}	Address A_{0+2} Write, Inc. Count
n+5	A_1	L	L	L	L	L	X	D_{0+3}	Address A_{0+3} Write, Load A_1
n+6	X	X	H	X	L	L	X	D_0	Address A_0 Write, Inc. Count
n+7	X	X	H	X	L	L	X	D_1	Address A_1 Write, Inc. Count
n+8	A_2	L	L	L	L	L	X	D_{1+1}	Address A_{1+1} Write, Load A_2

5299 tbl 16

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE_1}$ = L, $\overline{CE_2}$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE_1}$ = H, $\overline{CE_2}$ = H or CE_2 = L.

Read Operation with Clock Enable Used[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$[2]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A_1	H	L	L	L	X	X	X	Clock Valid
n+3	X	X	X	X	H	X	L	Q_0	Clock Ignored, Data Q_0 is on the bus.
n+4	X	X	X	X	H	X	L	Q_0	Clock Ignored, Data Q_0 is on the bus.
n+5	A_2	H	L	L	L	X	L	Q_0	Address A_0 Read out (bus trans.)
n+6	A_3	H	L	L	L	X	L	Q_1	Address A_1 Read out (bus trans.)
n+7	A_4	H	L	L	L	X	L	Q_2	Address A2 Read out (bus trans.)

5299 tbl 17

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Write Operation with Clock Enable Used[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$[2]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup.
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored.
n+2	A_1	L	L	L	L	L	X	X	Clock Valid.
n+3	X	X	X	X	H	X	X	X	Clock Ignored.
n+4	X	X	X	X	H	X	X	X	Clock Ignored.
n+5	A_2	L	L	L	L	L	X	D_0	Write Data D_0
n+6	A_3	L	L	L	L	L	X	D_1	Write Data D_1
n+7	A_4	L	L	L	L	L	X	D_2	Write Data D_2

5299 tbl 18

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Read Operation with Chip Enable Used(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O(3)	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	?	Deselected.
n+2	A_0	H	L	L	L	X	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+4	A_1	H	L	L	L	X	L	Q_0	Address A_0 Read out. Load A_1.
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+6	X	X	L	H	L	X	L	Q_1	Address A_1 Read out. Deselected.
n+7	A_2	H	L	L	L	X	X	Z	Address and control meet setup.
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+9	X	X	L	H	L	X	L	Q_2	Address A_2 Read out. Deselected.

5299 tbl 19

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.
3. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.

Write Operation with Chip Enable Used(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	?	Deselected.
n+2	A_0	L	L	L	L	L	X	Z	Address and Control meet setup.
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+4	A_1	L	L	L	L	L	X	D_0	Address D_0 Write in. Load A_1.
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+6	X	X	L	H	L	X	X	D_1	Address D_1 Write in. Deselected.
n+7	A_2	L	L	L	L	L	X	Z	Address and control meet setup.
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+9	X	X	L	H	L	X	X	D_2	Address D_2 Write in. Deselected.

5299 tbl 20

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V±5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LI}\|$	$\overline{LBO}$ Input Leakage Current(1)	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{DDQ}, Device Deselected	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +8mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -8mA, V_{DD} = Min.	2.4	—	V

5299 tbl 21

NOTE:
1. The $\overline{LBO}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ pin will be internally pulled to V_{SS} if not actively driven..

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1) (V_{DD} = 3.3V±%)

Symbol	Parameter	Test Conditions	133MHz	100MHz	Unit
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, ADV/$\overline{LD}$ = X, V_{DD} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}(2)	300	250	mA
I_{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0(2,3)	40	40	mA
I_{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX}(2,3)	110	100	mA
I_{SB3}	Idle Power Supply Current	Device Selected, Outputs Open, $\overline{CEN} \geq V_{IH}$, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX}(2,3)	40	40	mA

5299 tbl 22

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of $1/t_{CYC}$; f=0 means no input lines are changing.
3. For I/Os V_{HD} = V_{DDQ} – 0.2V, V_{LD} = 0.2V. For other inputs V_{HD} = V_{DD} – 0.2V, V_{LD} = 0.2V.

AC Test Load

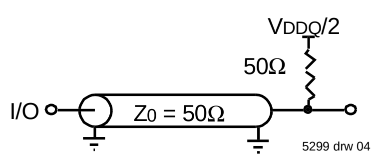


Figure 1. AC Test Load

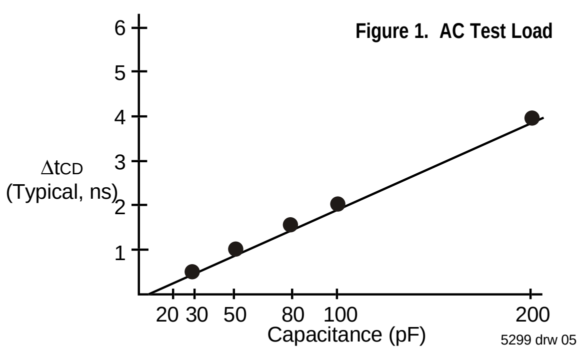


Figure 2. Lumped Capacitive Load, Typical Derating

AC Test Conditions (V_{DDQ} = 3.3V/2.5V)

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figure 1

5299 tbl 23

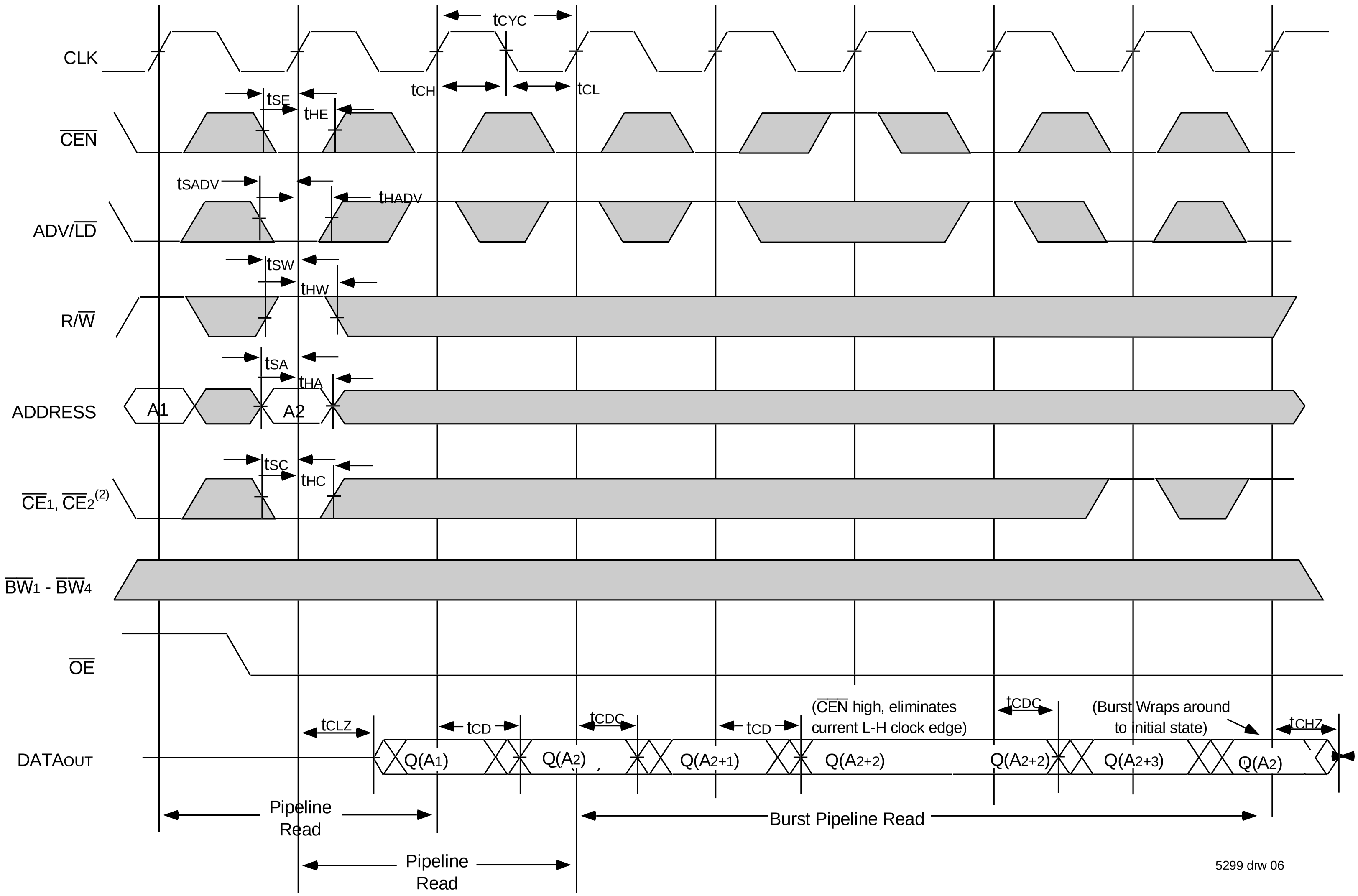
AC Electrical Characteristics
(V_{DD} = 3.3V±5%, T_A = 0 to 70°C)

Symbol	Parameter	133MHz		100MHz		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	7.5	—	10	—	ns
t_F(1)	Clock Frequence	—	133	—	100	MHz
t_{CH}(2)	Clock High Pulse Width	2.2	—	3.2	—	ns
t_{CL}(2)	Clock Low Pulse Width	2.2	—	3.2	—	ns
Output Parameters						
t_{CD}	Clock High to Valid Data	—	(t_{CYC} / 3) + 2.0(5)	—	(t_{CYC} / 3) + 2.0(5)	ns
t_{CDC}	Clock High to Data Change	(t_{CYC} / 3) - 0.2(5)	—	(t_{CYC} / 3) - 0.2(5)	—	ns
t_{CLZ}(3,4)	Clock High to Output Active	(t_{CYC} / 3) - 0.2(5)	—	(t_{CYC} / 3) - 0.2(5)	—	ns
t_{CHZ}(3,4)	Clock High to Data High-Z	1.5	3	1.5	3.3	ns
t_{OE}	Output Enable Access Time	—	4.2	—	5	ns
t_{OLZ}(3,4)	Output Enable Low to Data Active	0	—	0	—	ns
t_{OHZ}(3,4)	Output Enable High to Data High-Z	—	4.2	—	5	ns
Set Up Times						
t_{SE}	Clock Enable Setup Time	1.7	—	2.0	—	ns
t_{SA}	Address Setup Time	1.7	—	2.0	—	ns
t_{SD}	Data In Setup Time	1.7	—	2.0	—	ns
t_{SW}	Read/Write (R/$\overline{W}$) Setup Time	1.7	—	2.0	—	ns
t_{SADV}	Advance/Load (ADV/$\overline{LD}$) Setup Time	1.7	—	2.0	—	ns
t_{SC}	Chip Enable/Select Setup Time	1.7	—	2.0	—	ns
t_{SB}	Byte Write Enable ($\overline{BW}$x) Setup Time	1.7	—	2.0	—	ns
Hold Times						
t_{HE}	Clock Enable Hold Time	0.5	—	0.5	—	ns
t_{HA}	Address Hold Time	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.5	—	0.5	—	ns
t_{HW}	Read/Write (R/$\overline{W}$) Hold Time	0.5	—	0.5	—	ns
t_{HADV}	Advance/Load (ADV/$\overline{LD}$) Hold Time	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	ns
t_{HB}	Byte Write Enable ($\overline{BW}$x) Hold Time	0.5	—	0.5	—	ns

5299 tbl 23a

NOTES:
1. $t_F = 1/t_{CYC}$.
2. Measured as HIGH above $0.6V_{DDQ}$ and LOW below $0.4V_{DDQ}$.
3. Transition is measured ±200mV from steady-state.
4. These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
5. Smart ZBT™ functionality only guaranteed at 66 MHz ≤ f ≤ 133MHz.

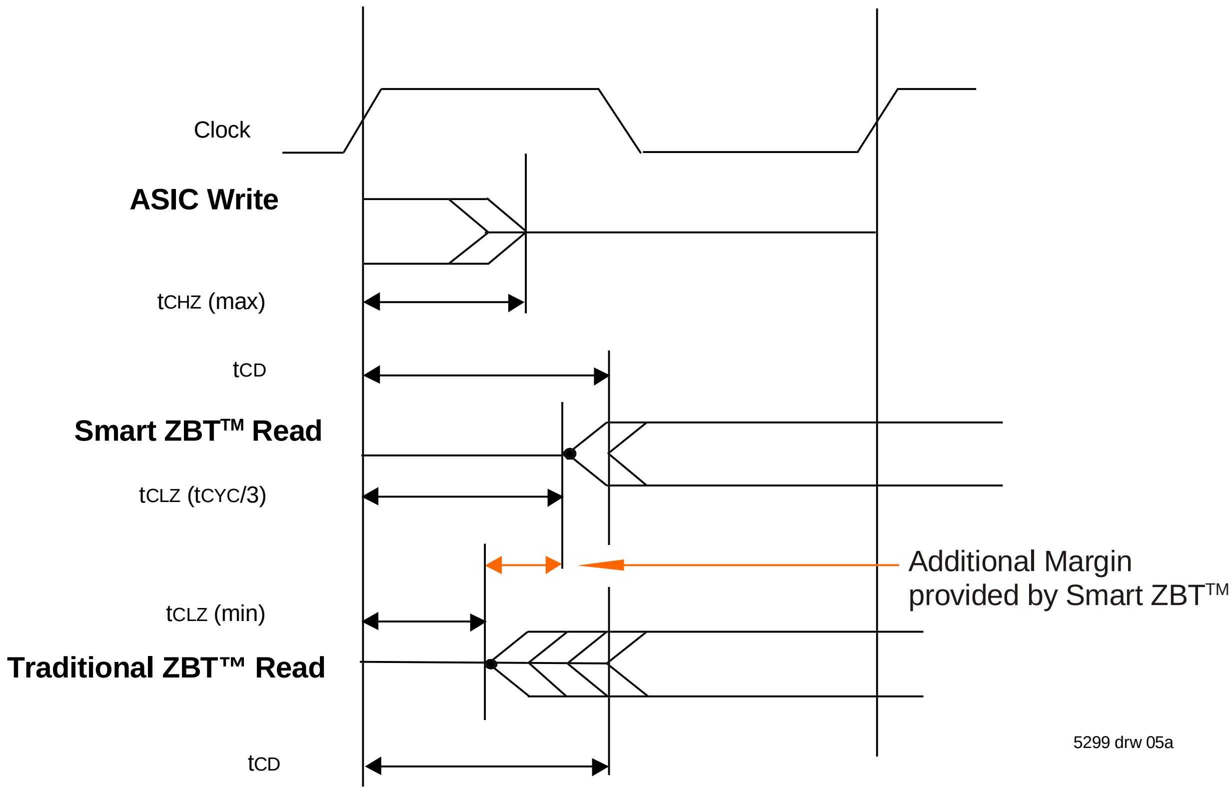
Timing Waveform of Read Cycle(1,2,3,4)



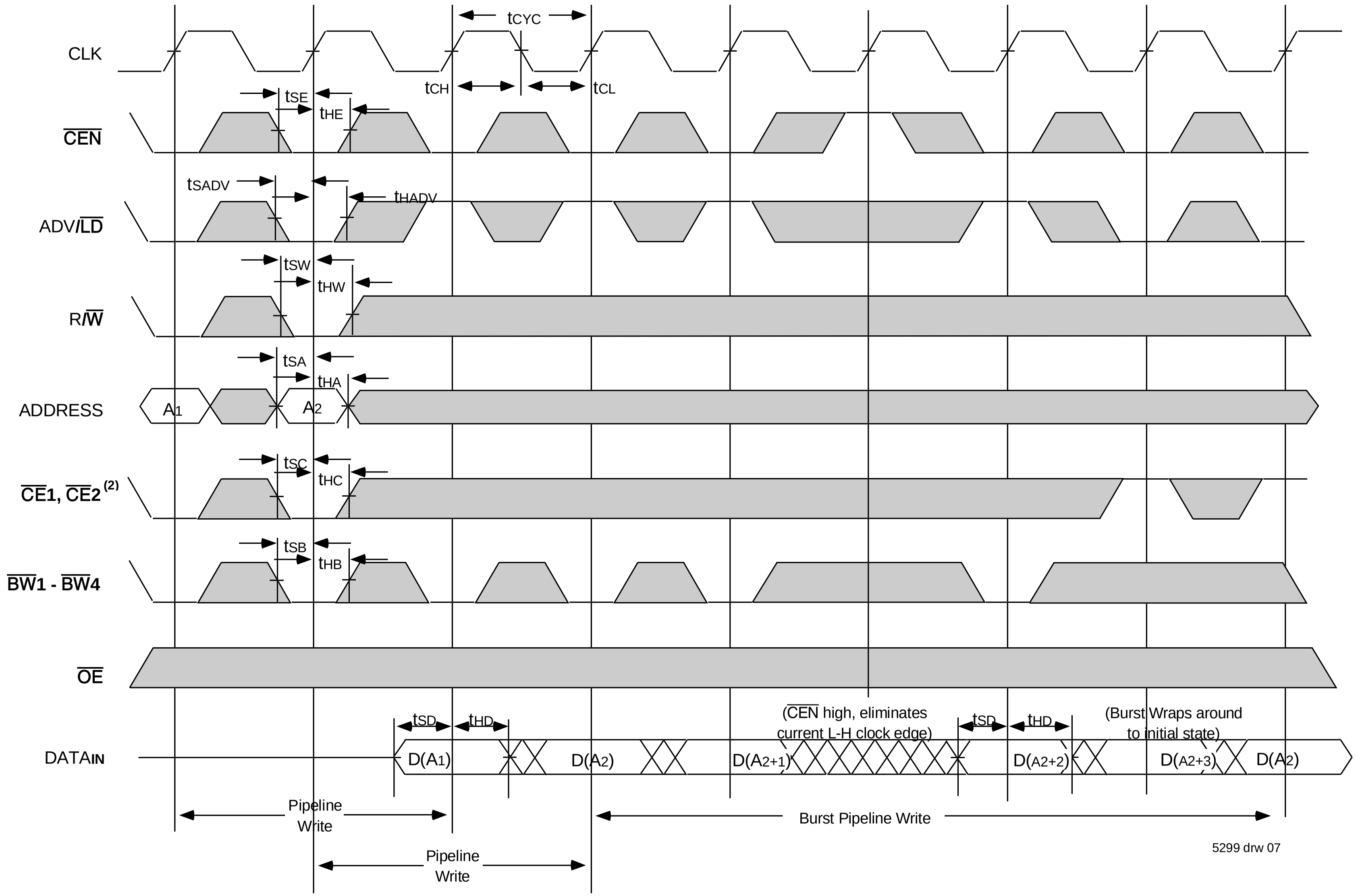
NOTES:

1. Q (A_1) represents the first output from the external address A_1. Q (A_2) represents the first output from the external address A_2; Q (A_{2+1}) represents the next output data in the burst sequence of the base address A_2, etc. where address bits A_0 and A_1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. CE_2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE_2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/$\overline{LD}$ LOW.
4. R/$\overline{W}$ is don't care when the SRAM is bursting (ADV/$\overline{LD}$ sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/$\overline{W}$ signal when new address and control are loaded into the SRAM.

Smart ZBT™ Timing



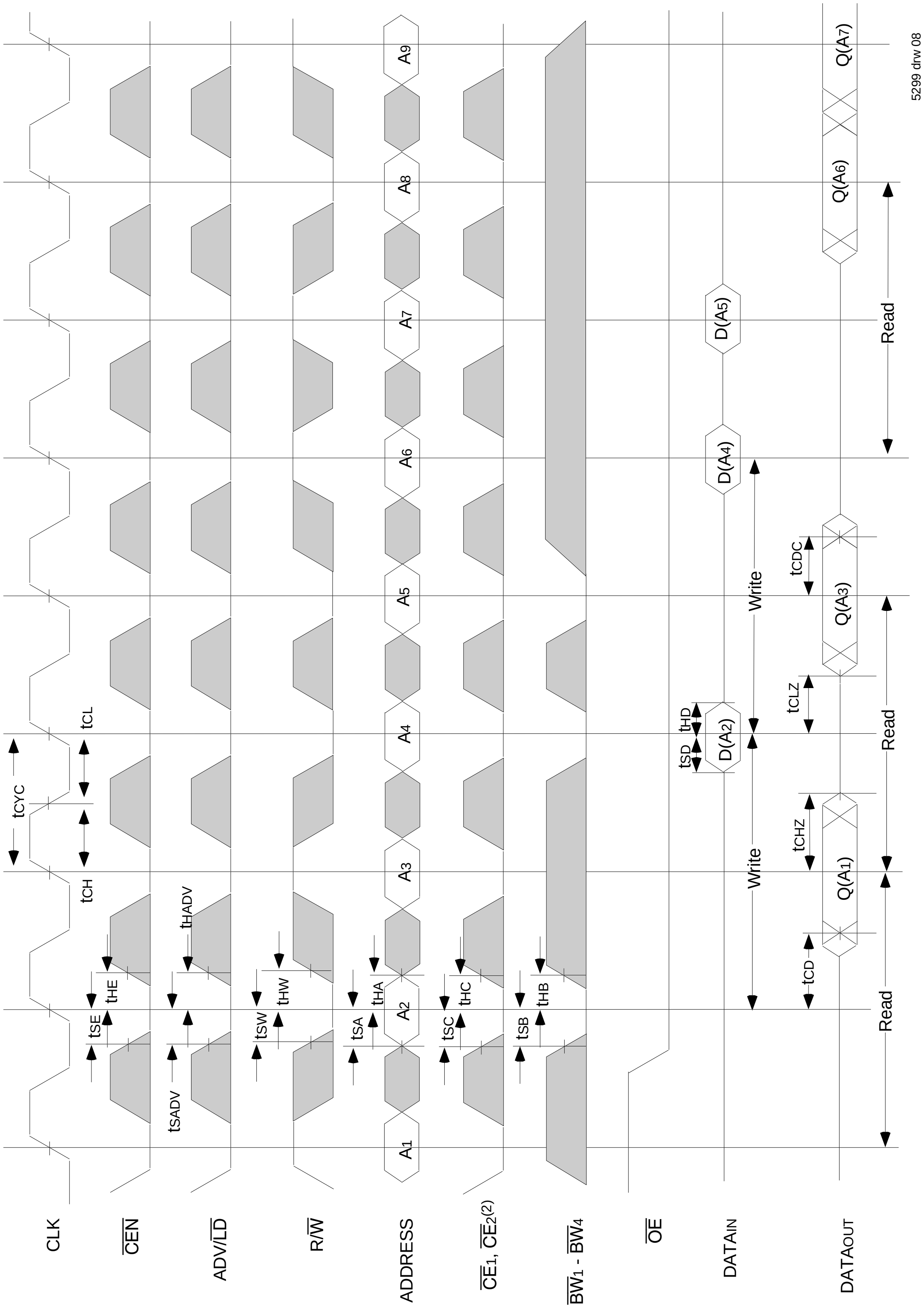
Timing Waveform of Write Cycles(1,2,3,4,5)



NOTES:

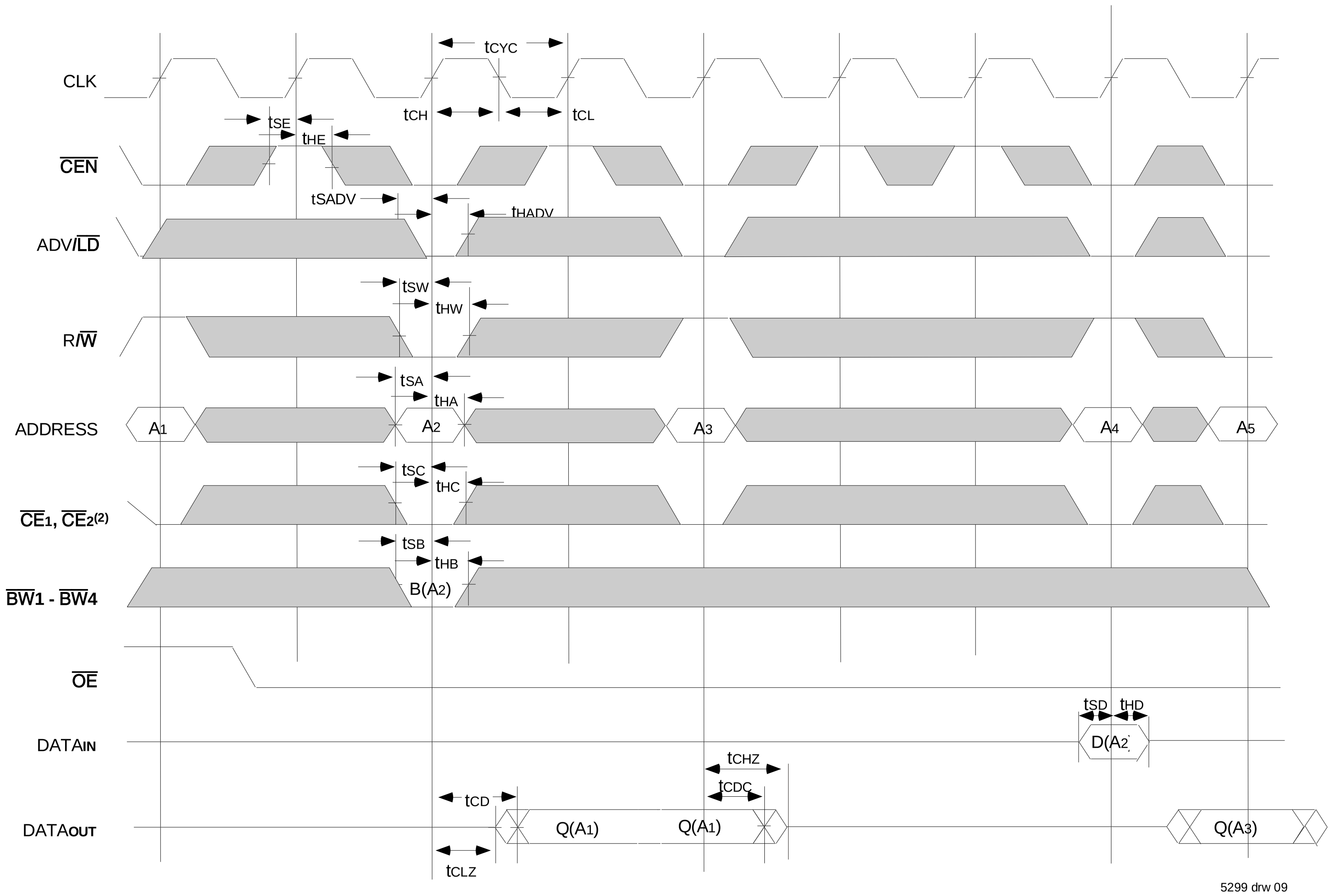
1. D (A_1) represents the first input to the external address A_1. D (A_2) represents the first input to the external address A_2; D (A_{2+1}) represents the next input data in the burst sequence of the base address A_2, etc. where address bits A_0 and A_1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. CE_2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/$\overline{LD}$ LOW.
4. R/$\overline{W}$ is don't care when the SRAM is bursting (ADV/$\overline{LD}$ sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/$\overline{W}$ signal when new address and control are loaded into the SRAM.
5. Individual Byte Write signals ($\overline{BW}$x) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of Combined Read and Write Cycles(1,2,3)



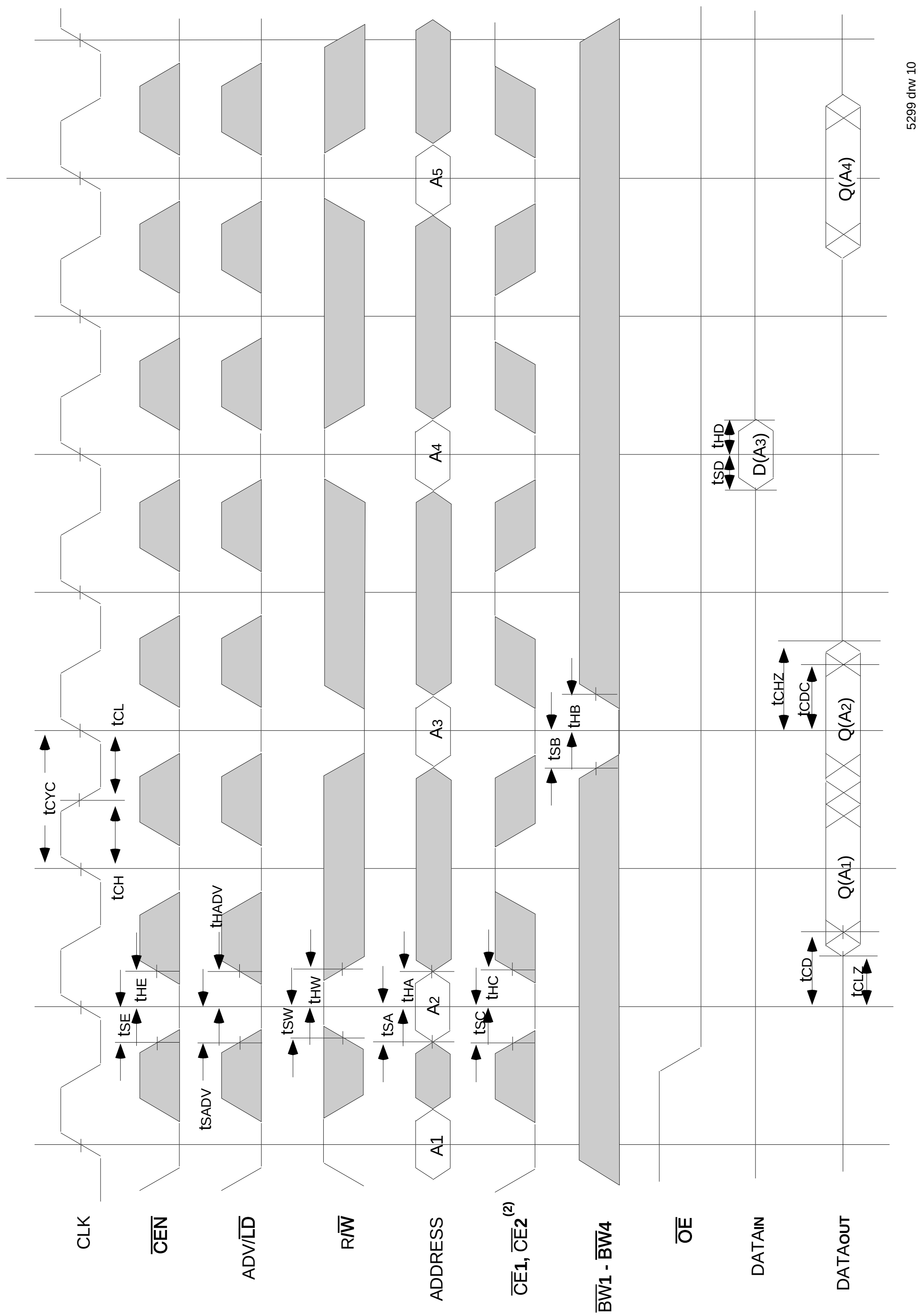
NOTES:
1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. CE2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE2 is HIGH.
3. Individual Byte Write signals ($\overline{BW}$x) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of $\overline{CEN}$ Operation(1,2,3,4)



NOTES:
1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. CE2 timing transitions are identical but inverted to the $\overline{CE_1}$ and $\overline{CE_2}$ signals. For example, when $\overline{CE_1}$ and $\overline{CE_2}$ are LOW on this waveform, CE2 is HIGH.
3. $\overline{CEN}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propogating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($\overline{BW}$x) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

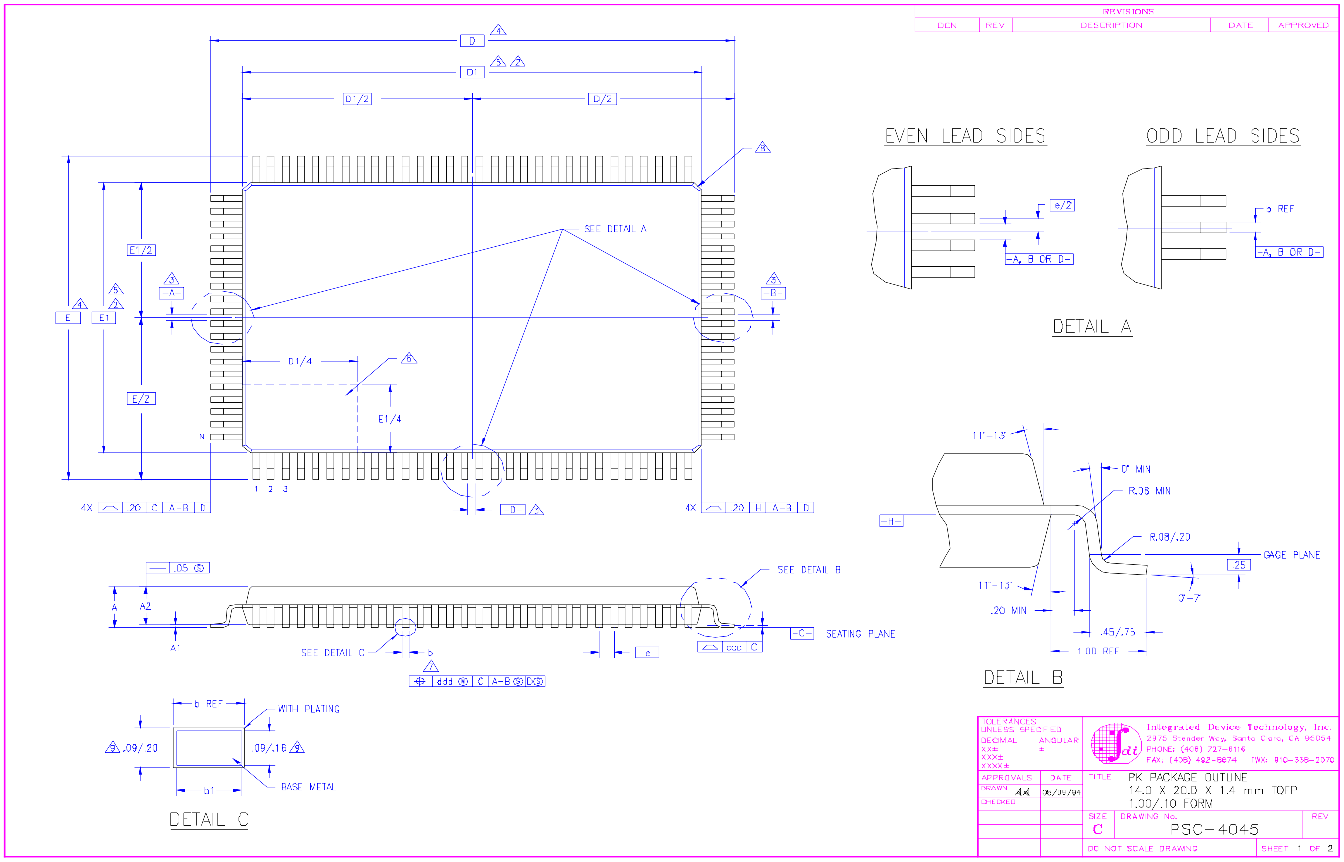
Timing Waveform of $\overline{CS}$ Operation(1,2,3,4)



NOTES:

1. Q (A_1) represents the first output from the external address A_1. D (A_3) represents the input data to the SRAM corresponding to address A_3.
2. CE_2 timing transitions are identical but inverted to the $\overline{CE_1}$ and $\overline{CE_2}$ signals. For example, when $\overline{CE_1}$ and $\overline{CE_2}$ are LOW on this waveform, CE_2 is HIGH.
3. $\overline{CEN}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propogating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($\overline{BWx}$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

100-Pin Plastic Thin Quad Flatpack (TQFP) Package Diagram Outline



REVISIONS

DCN	REV	DESCRIPTION	DATE	APPROVED

SYMBOL	JEDEC VARIATION DJ MIN	NOM	MAX	NOTE
A	–	–	1.60	
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D		22.00 BSC		4
D1		20.00 BSC		5,2
E		16.00 BSC		4
E1		14.00 BSC		5,2
N		100		
ND		30		
NE		20		
e		.65 BSC		
b	.22	.32	.38	7
b1	.22	.30	.33	
ccc	–	–	.10	
ddd	–	–	.13	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3 DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]

5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6 DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

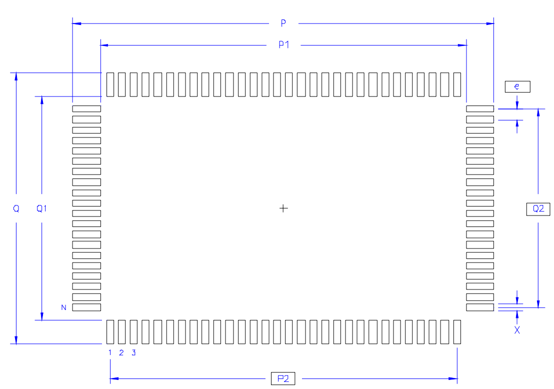
8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION DJ AND BX

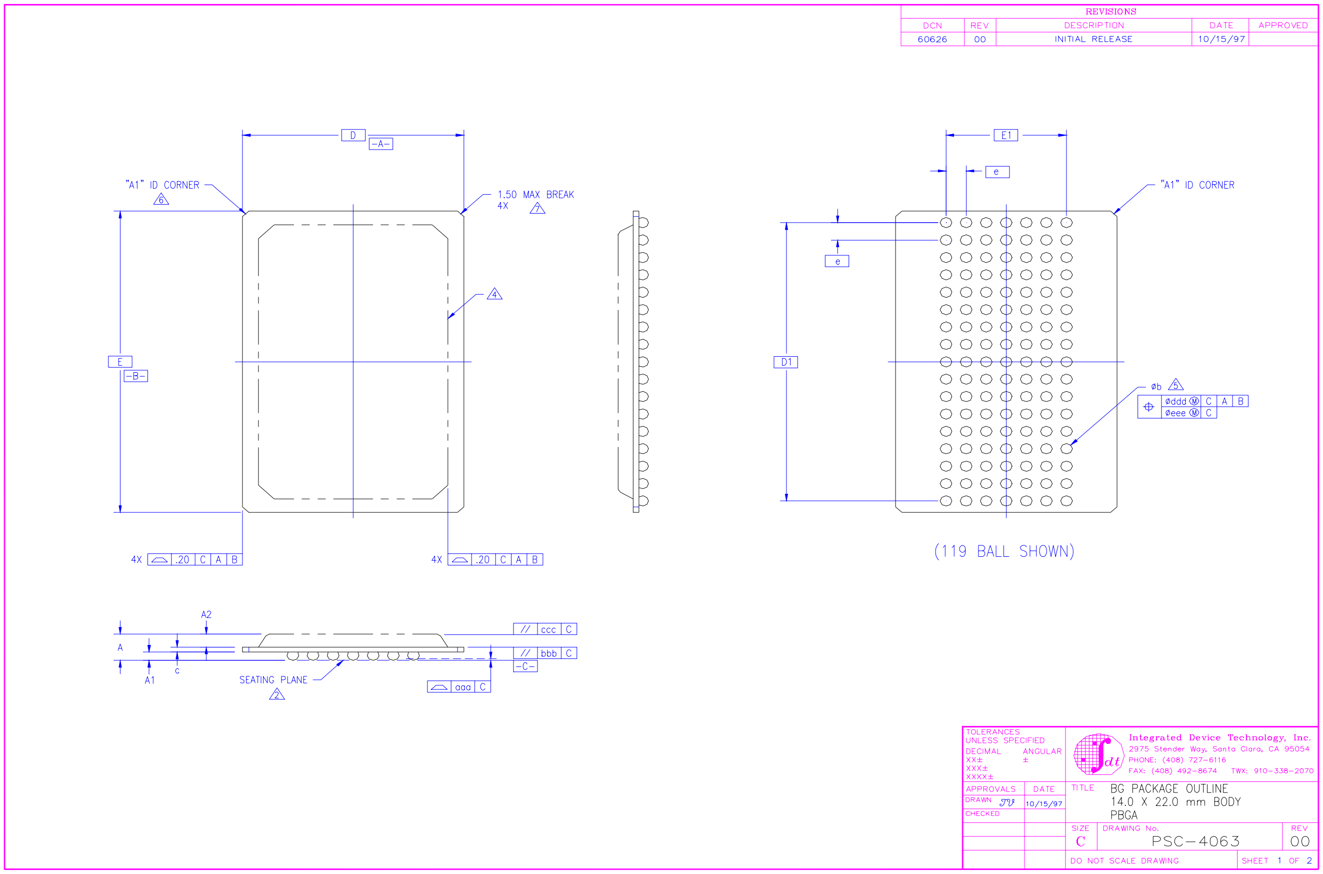
LAND PATTERN DIMENSIONS



	MIN	MAX
P	22.80	23.00
P1	19.80	20.00
P2	18.85 BSC	
Q	16.80	17.00
Q1	13.80	14.00
Q2	12.35 BSC	
X	.30	.50
e	.65 BSC	
N	100	

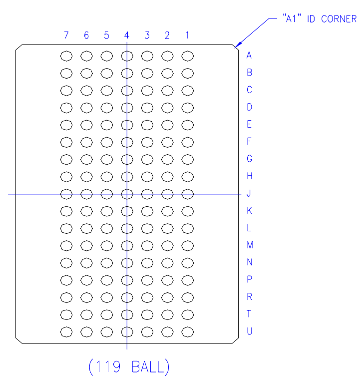
TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070
APPROVALS DATE
DRAWN 08/09/94
CHECKED
TITLE PK PACKAGE OUTLINE
14.0 X 20.0 X 1.4 mm TQFP
1.00/.10 FORM
SIZE C DRAWING No. PSC-4045 REV
DO NOT SCALE DRAWING SHEET 2 OF 2

119 Ball Grid Array (BGA) Package Diagram Outline



REVISIONS

DCN	REV	DESCRIPTION	DATE	APPROVED
60626	00	INITIAL RELEASE	10/15/97	



NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

3 "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION
"ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION
"N" IS THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS

4 PACKAGE MAY EXTEND TO EDGE PERIPHERY AND MAY CONSIST OF MOLDING COMPOUND, EPOXY, METAL, CERAMIC OR OTHER MATERIAL

5 DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-

6 "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY. MARK MUST BE VISIBLE FROM TOP SURFACE

7 ACTUAL SHAPE OF THIS FEATURE IS OPTIONAL

8 ALL DIMENSIONS ARE IN MILLIMETERS

9 THIS DRAWING CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-028, VARIATION AA

SYMBOL	JEDEC VARIATION AA MIN	NOM	MAX	NOTE
A	–	2.15	3.50	
A1	.50	.60	.70	
A2	–	–	2.50	
D		22.00 BSC		
D1		20.32 BSC		
E		14.00 BSC		
E1		7.62 BSC		
MD		17		3
ME		7		3
N		119		3
e		1.27 BSC		
b	.60	.75	.90	5
c	.10	–	2.50	
aaa	–	–	.20	
bbb	–	–	.25	
ccc	–	–	.35	
ddd	–	–	.30	
eee	–	–	.15	

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX± ANGULAR ±
APPROVALS | DATE
DRAWN | 10/15/97
CHECKED

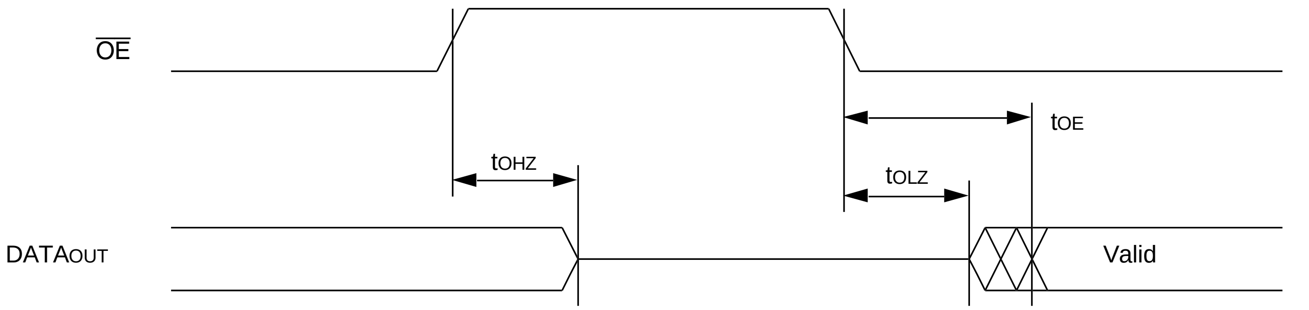
Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

TITLE BG PACKAGE OUTLINE
14.0 X 22.0 mm BODY
PBGA

SIZE C | DRAWING No. PSC-4063 | REV 00

DO NOT SCALE DRAWING | SHEET 2 OF 2

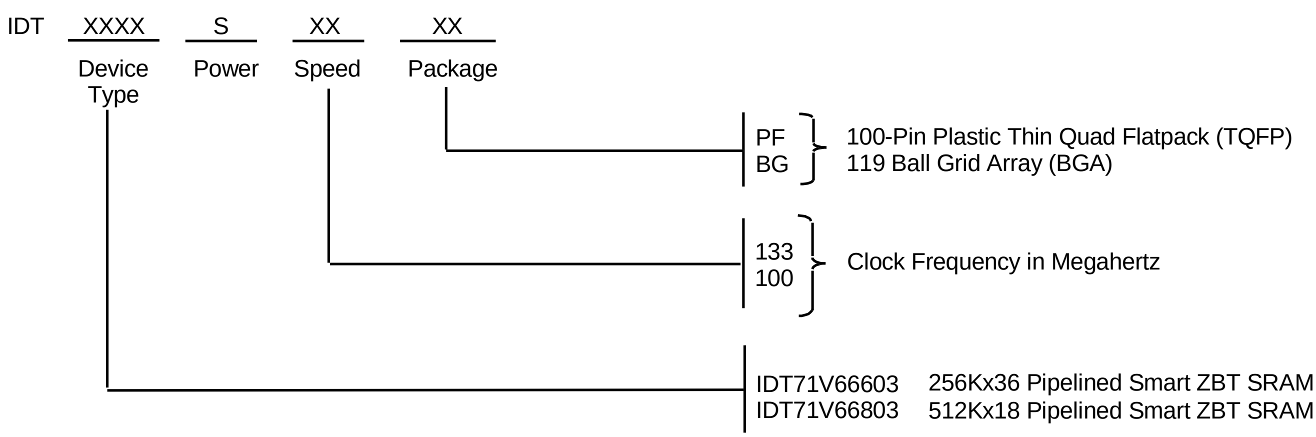
Timing Waveform of $\overline{OE}$ Operation(1)



5299 drw 11

NOTE:
1. A read operation is assumed to be in progress.

Ordering Information



5299 drw 12

Datasheet Document History

12/31/99		Created Smart ZBT datasheet
04/20/00	Pg. 4, 5	Added JTAG reset pins to TQFP pin configuration; removed footnote
		Inserted clarification note to Recommended Operating Temperature and Absolute Max Ratings tables
	Pg. 6	Add note to BGA pin configuration; corrected typo in pinout
	Pg. 21	Insert TQFP Package Diagram Outline

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
sramhelp@idt.com
800-544-7726, x4033