

HIGH-CURRENT NPN TRANSISTOR ARRAYS

DESCRIPTION

The SG 3183 series of arrays consists of five, closely-matched, high-current NPN transistors. Although sharing a common monolithic substrate, the transistors are connected such that all terminals are independent, including the substrate bias connector. With current capability to 100mA per transistor, these arrays are ideally suited for all types of driving applications including relays, lamps, and thyristors.

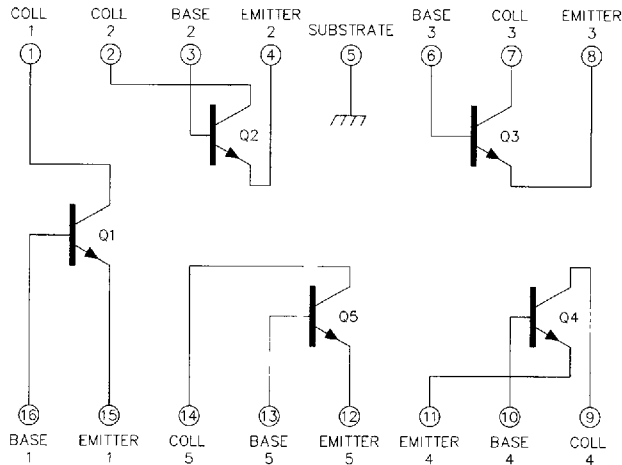
FEATURES

- High voltage capability
- Collector current to 100mA
- Low saturation voltage
- Closely matched parameters

HIGH RELIABILITY FEATURES - SG3183

- ◆ Available to MIL-STD-883
- ◆ SG level "S" processing available

BLOCK DIAGRAM



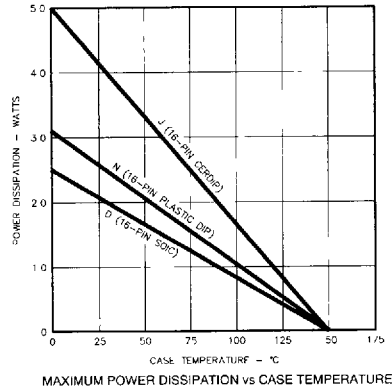
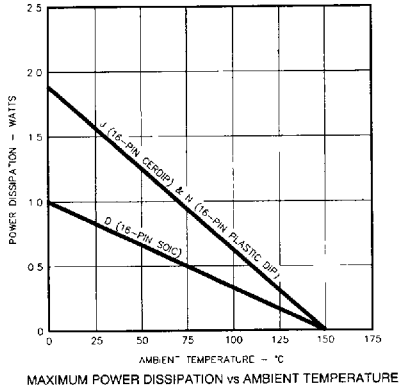
ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Collector Current	100mA
Maximum Base Current	20mA
Power Dissipation	
Any One Transistor	500mW
Total Package	750mW

Operating Junction Temperature	
Hermetic (J-Packages)	150°C
Plastic (N, D-Package)	150°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 Seconds)	300°C

Note 1 Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



RECOMMENDED OPERATING CONDITIONS (Note 2)

Operating Ambient Temperature	
SG3183 (J-Package)	-55°C to 125°C
SG3183 (N, D-Package)	0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures of $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ for the SG3183 (J-package) and $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ for the SG3183 (N & D - packages). Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG3183			Units
		Min.	Typ.	Max.	
Breakdown Voltage					
Collector-Substrate (BV_{CSO})	$I_C = 100\mu\text{A}$	40	70		V
Collector-Base (BV_{CBO})	$I_C = 100\mu\text{A}$	40	70		V
Collector-Emitter (BV_{CEO})	$I_C = 1\text{mA}$	30	40		V
Emitter-Base (BV_{EBO})	$I_E = 100\mu\text{A}$	5.0	6.9		V
Collector Cutoff Current (I_{CEO})	$V_{CE} = 10\text{V}$			10	μA
Collector Cutoff Current (I_{CBO})	$V_{CB} = 10\text{V}$			1	μA
DC Forward Current Transfer Ratio (h_{FE})	$V_{CE} = 3\text{V}, I_C = 10\text{mA}$ $T_A = 25^{\circ}\text{C}$	40			
	$V_{CE} = 3\text{V}, I_C = 10\text{mA}$ $T_A = 25^{\circ}\text{C}$	50	100		
	$V_{CE} = 3\text{V}, I_C = 10\text{mA}$ $T_A = 25^{\circ}\text{C}$	35			
	$V_{CE} = 3\text{V}, I_C = 10\text{mA}$ $T_A = 25^{\circ}\text{C}$	40	75		
Collector-Emitter Saturation Voltage ($V_{CE(SAT)}$)	$I_C = 50\text{mA}, I_B = 5\text{mA}$		1.7	3.0	V
Base-to-Emitter Voltage (V_{BE})	$V_{CE} = 3\text{V}, I_C = 10\text{mA}$ $T_A = 25^{\circ}\text{C}$	0.50		0.95	V
	$V_{CE} = 3\text{V}, I_C = 1\text{mA}$ $T_A = 25^{\circ}\text{C}$	0.65	0.75	0.85	V
For Q_1 and Q_2 Matched Pair:					
Input Offset Voltage (V_{IO})	$T_A = 25^{\circ}\text{C}$			10	mV
	$T_A = 25^{\circ}\text{C}$			5.0	mV
Input Offset Current (I_{IO})	$T_A = 25^{\circ}\text{C}$			5.0	μA
	$T_A = 25^{\circ}\text{C}$			0.7	μA

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG3183J/883B SG3183J	-55°C to 125°C -55°C to 125°C	<pre> C1 [] 1 16 [] B1 C2 [] 2 15 [] E1 B2 [] 3 14 [] C5 E2 [] 4 13 [] B5 SUBSTRATE [] 5 12 [] E5 B3 [] 6 11 [] E4 C3 [] 7 10 [] B4 E3 [] 8 9 [] C4 </pre>
16-PIN PLASTIC DIP N - PACKAGE	SG3183N	0°C to 70°C	
16-PIN SOIC D - PACKAGE	SG3183D	0°C to 70°C	<pre> C1 [] 1 16 [] B1 C2 [] 2 15 [] E1 B2 [] 3 14 [] C5 E2 [] 4 13 [] B5 SUBSTRATE [] 5 12 [] E5 B3 [] 6 11 [] E4 C3 [] 7 10 [] B4 E3 [] 8 9 [] C4 </pre>

Note 1. Contact factory for JAN and DESC product availability.
 2. All packages are viewed from the top.