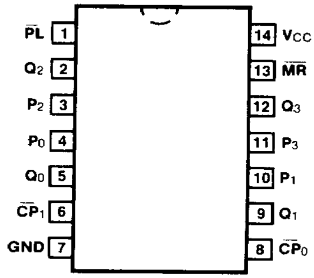
54/74177 610585

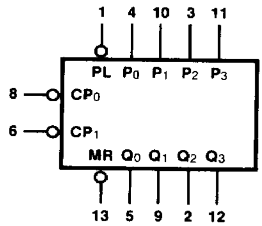
PRESETTABLE BINARY COUNTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '177 is a presettable modulo-16 ripple counter partitioned into divide-by-two and divide-by-eight sections, with a separate clock input for each section. In the counting mode, state changes are initiated by the falling edge of the clock. A LOW signal on the Master Reset ($\overline{MR}$) input overrides all other inputs and forces the outputs LOW. A LOW signal on the Parallel Load ($\overline{PL}$) input overrides the clocks and causes the Q outputs to assume the state of their respective Parallel Data (P_n) inputs. For detail specifications, please refer to the '176 data sheet.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74177PC		9A
Ceramic DIP (D)	A	74177DC	54177DM	6A
Flatpak (F)	A	74177FC	54177FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\overline{CP}_0$	÷2 Section Clock Input (Active Falling Edge)	2.0/3.0
$\overline{CP}_1$	÷8 Section Clock Input (Active Falling Edge)	2.0/2.0
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	2.0/2.0
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0
$Q_0 - Q_3$	Flip-flop Outputs*	20/10

*Q_0 is guaranteed to drive $\overline{CP}_1$ in addition to the full rated load.

FUNCTIONAL DESCRIPTION—The '177 is an asynchronously presettable binary ripple counter partitioned into divide-by-two and divide-by-eight sections. In the counting modes, state changes are initiated by the HIGH-to-LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q_n outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The $\overline{CP}_0$ input serves the Q_0 flip-flop while the $\overline{CP}_1$ input serves the divide-by-eight section. The Q_0 output is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input. With the input frequency connected to $\overline{CP}_0$ and with Q_0 driving $\overline{CP}_1$, the '177 forms a straightforward modulo-16 counter, with Q_0 the least significant output and Q_3 the most significant output.

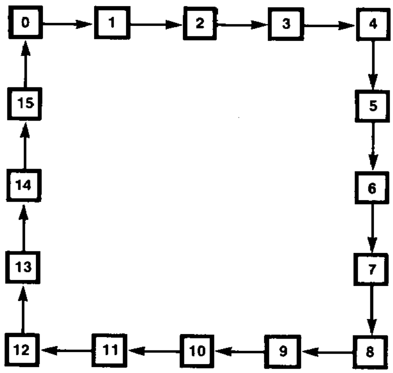
The '177 has an asynchronous active LOW Master Reset input ($\overline{MR}$) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input ($\overline{PL}$) overrides the clock inputs and loads the data from Parallel Data (P_0 — P_3) inputs into the flip-flops. While $\overline{PL}$ is LOW, the counters act as transparent latches and any change in the P_n inputs will be reflected in the outputs.

MODE SELECT TABLE

INPUTS			RESPONSE
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Q_n forced LOW
H	L	X	$P_n \rightarrow Q_n$
H	H	⌝_	Count Up

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

STATE DIAGRAM



LOGIC DIAGRAM