



# Pentium<sup>®</sup> Processor Compatible Clock Synthesizer/Driver

## Features

- Multiple clock outputs to meet requirements of most Pentium<sup>®</sup> motherboards
  - Four pin-selectable CPU clocks @ 66.66 MHz, 60.0 MHz, and 50.0 MHz for support of Intel Triton<sup>™</sup> PCIs set based PC
  - 55.0 MHz pin-selectable CPU clock also available (-2 option only)
  - Six PCI clocks at 1/2 CPU Clock frequency
  - One I/O clock @ 24 MHz
  - One Keyboard Controller clock @ 12 MHz (-1 option) or one Universal Serial Bus clock @ 48 MHz (-2 option)
  - Two Ref. clocks @ 14.318 MHz
  - Ref. 14.318 MHz Xtal oscillator input
- CPU clock jitter  $\leq 200$  ps cycle-to-cycle
- Low skew outputs
  - $\leq 250$  ps between CPU clocks
  - $\leq 250$  ps between PCI clocks
  - $\leq 500$  ps between CPU and PCI clocks (-2 option)
  - CPU clock leads PCI clock by +1 ns min. to +4 ns max. (-1 option)

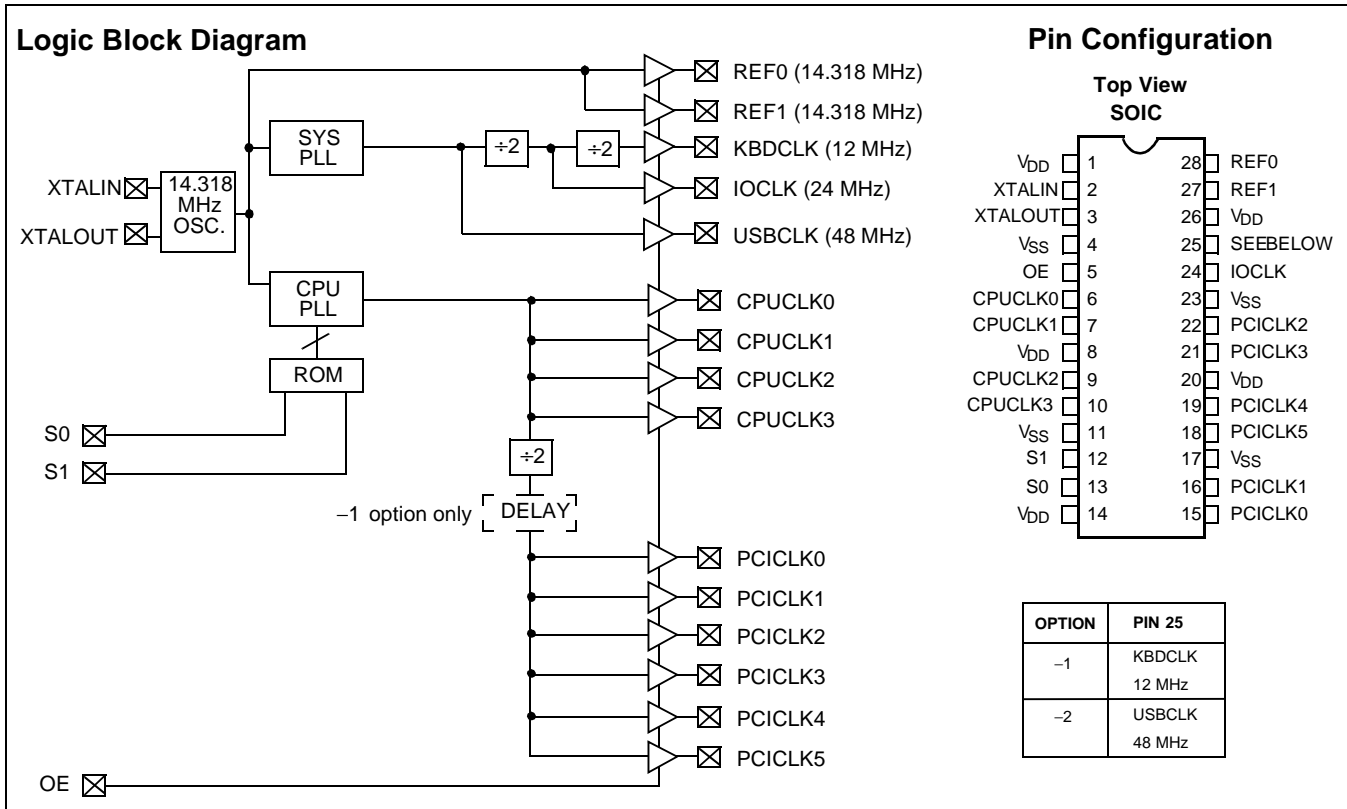
- Freq. stability = 0.01% (max.)
- Output duty cycle 45% min. to 55% max.
- Test mode support (-1 option only)
- 3.3V or 5.0V operation
- Internal pull-up resistors on S0, S1, and OE inputs

## Functional Description

The CY2254A is a Clock Synthesizer/Driver that provides the multiple clocks required for a Pentium-based PC. The CY2254A has low-skew outputs ( $\leq 250$  ps between the CPU Clocks,  $\leq 250$  ps between the PCI Clocks). In addition, the CY2254A CPU clock outputs have less than 200 ps cycle-to-cycle jitter. Finally, both the PCI and CPU clock outputs meet the 1 V/ns slew rate requirement of a Pentium processor-based system.

The CY2254A accepts a 14.318 MHz reference signal as its input. The CY2254A has 2 PLLs, one of which generates the CPU and PCI clocks, and the other generates the I/O and Keyboard Controller or USB clocks. The CY2254A runs off either a 3.3V or 5V supply.

The CY2254A is available in two options. The -1 option supports the Intel Triton PCIs set and provides a 12 MHz keyboard clock on pin 25. The -2 option provides a 48 MHz USB clock on pin 25 and supports the Cyrix<sup>®</sup> M1 processor.



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 Triton is a trademark of Intel Corporation.  
 Cyrix is a registered trademark of Cyrix Corporation.

**Pin Summary**

Name	-1	-2	Description
V <sub>DD</sub>	1	1	Voltage supply
XTALIN <sup>[1]</sup>	2	2	Reference crystal input
XTALOUT <sup>[1]</sup>	3	3	Reference crystal feedback
V <sub>SS</sub>	4	4	Ground
OE	5	5	Output Enable, Active HIGH (internal pull-up resistor to V <sub>DD</sub> )
CPUCLK0	6	6	CPU clock output
CPUCLK1	7	7	CPU clock output
V <sub>DD</sub>	8	8	Voltage supply
CPUCLK2	9	9	CPU clock output
CPUCLK3	10	10	CPU clock output
V <sub>SS</sub>	11	11	Ground
S1	12	12	CPU clock select input, bit 1 (internal pull-up resistor to V <sub>DD</sub> )
S0	13	13	CPU clock select input, bit 0 (internal pull-up resistor to V <sub>DD</sub> )
V <sub>DD</sub>	14	14	Voltage supply
PCICLK0	15	15	PCI clock output
PCICLK1	16	16	PCI clock output
V <sub>SS</sub>	17	17	Ground
PCICLK5	18	18	PCI clock output
PCICLK4	19	19	PCI clock output
V <sub>DD</sub>	20	20	Voltage supply
PCICLK3	21	21	PCI clock output
PCICLK2	22	22	PCI clock output
V <sub>SS</sub>	23	23	Ground
IOCLK	24	24	I/O clock output (24 MHz)
KBDCLK	25		Keyboard controller clock output (12 MHz)
USBCLK		25	Universal Serial Bus clock output (48 MHz)
V <sub>DD</sub>	26	26	Voltage supply
REF1	27	27	Reference clock output (14.318 MHz)
REF0	28	28	Reference clock output (14.318 MHz)

**Function Table**

Option	OE	S0	S1	XTALIN	CPUCLK	PCICLK	Ref. Clock Output	IOCLK	KBDCLK -1 only	USBCLK -2 only
-1,-2	0	X	X	14.318 MHz	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
-1,-2	1	0	0	14.318 MHz	50.0 MHz	25.0 MHz	14.318 MHz	24 MHz	12 MHz	48 MHz
-1,-2	1	0	1	14.318 MHz	60.0 MHz	30.0 MHz	14.318 MHz	24 MHz	12 MHz	48 MHz
-1,-2	1	1	0	14.318 MHz	66.66 MHz	33.33 MHz	14.318 MHz	24 MHz	12 MHz	48 MHz
-1	1	1	1	TCLK <sup>[2]</sup>	TCLK/2	TCLK/4	TCLK	TCLK/4	TCLK/8	
-2	1	1	1	14.318 MHz	55.0 MHz	27.5 MHz	14.318 MHz	24 MHz		48 MHz

**Notes:**

- For best accuracy, use a parallel-resonant crystal, C<sub>LOAD</sub> = 17 pF.
- TCLK is a test clock on XTALIN (pin 2) during test mode.

**PCI Clock Driver Strength Requirements**

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V
- Maximum output impedance: 40Ω measured at 1.5V

**CPU Clock Driver Strength Requirements**

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V
- Maximum output impedance: 40Ω measured at 1.5V

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage.....	-0.5 to +7.0V
Input Voltage .....	-0.5V to $V_{DD} + 0.5$
Storage Temperature (Non-Condensing) ....	-65°C to +150°C
Junction Temperature .....	+150°C
Package Power Dissipation.....	1W
Static Discharge Voltage.....	>2000V (per MIL-STD-883, Method 3015)

**Operating Conditions<sup>[3]</sup>**

Parameter	Description	Min.	Max.	Unit
$V_{DD}$	Supply Voltage 3.3V	3.135	3.6	V
	Supply Voltage 5.0V	4.5	5.5	V
$T_A$	Operating Ambient Temperature	0	70	°C
$C_L$	Max. Capacitive Load on CPUCLK		20	pF
	PCICLK		30	
	IOCLK		20	
	KBDCLK / USBCLK		20	
	REF0		30	
	REF1		15	
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz
$t_{PU}$	Power-up time for all $V_{DD}$ 's to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

**Electrical Characteristics**  $V_{DD} = 3.135V - 3.6V$ , or  $5.0V \pm 10\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ 

Parameter	Description	Test Conditions		Min.	Max.	Unit
$V_{IH}$	High-level Input Voltage	Except Crystal Inputs		2.0		V
$V_{IL}$	Low-level Input Voltage	Except Crystal Inputs			0.8	V
$V_{OH}^{[4]}$	High-level Output Voltage	$V_{DD} = V_{DD} \text{ Min.}$	$I_{OH} = 6 \text{ mA}$ CPUCLK	2.4		V
			$I_{OH} = 12 \text{ mA}$ PCICLK, REF0			
			$I_{OH} = 4 \text{ mA}$ KBDCLK, USBCLK			
			$I_{OH} = 8 \text{ mA}$ REF1			
$V_{OL}^{[4]}$	Low-level Output Voltage	$V_{DD} = V_{DD} \text{ Min.}$	$I_{OL} = 6 \text{ mA}$ CPUCLK		0.4	V
			$I_{OL} = 12 \text{ mA}$ PCICLK, REF0			
			$I_{OL} = 4 \text{ mA}$ KBDCLK, USBCLK			
			$I_{OL} = 8 \text{ mA}$ REF1			
$I_{IH}$	Input High Current	$V_{IH} = V_{DD}$ , $V_{DD} = 3.3V$			5	$\mu A$
		$V_{IH} = V_{DD}$ , $V_{DD} = 5.0V$			10	$\mu A$
$I_{IL}$	Input Low Current	$V_{IL} = 0 \text{ V}$ , $V_{DD} = 3.3V$			100	$\mu A$
		$V_{IL} = 0 \text{ V}$ , $V_{DD} = 5.0V$			250	$\mu A$
$I_{OZ}$	Output Leakage Current	Three-state		-10	+10	$\mu A$
$I_{DD}$	Power Supply Current	$V_{DD} = 3.6V$ , $V_{IN} = 0$ or $V_{DD}$			90	mA
		$V_{DD} = 5.5V$ , $V_{IN} = 0$ or $V_{DD}$			150	

**Electrical Characteristics**  $V_{DD} = 3.135V - 3.6V$ , or  $5.0V \pm 10\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$  (continued)

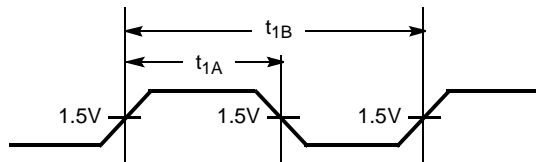
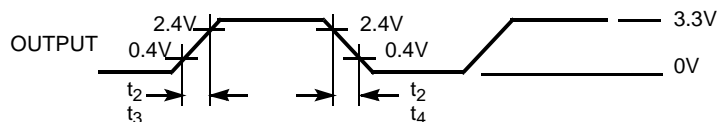
Parameter	Description	Test Conditions	Min.	Max.	Unit
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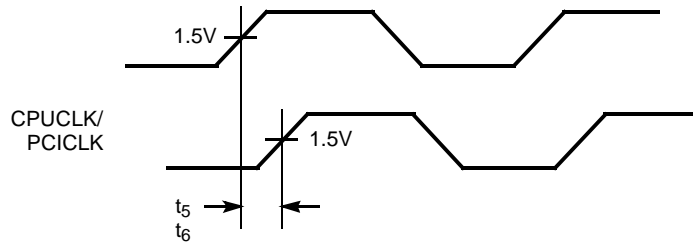
**Notes:**

3. Electrical parameters are guaranteed with these operating conditions.
4. Guaranteed by design, not tested.

**Switching Characteristics<sup>[5]</sup>**

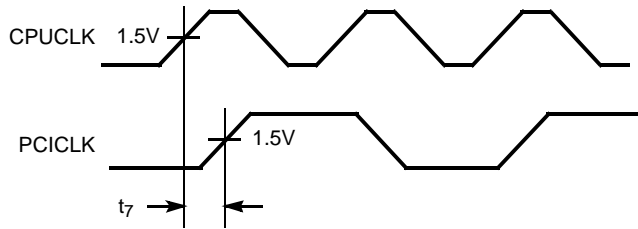
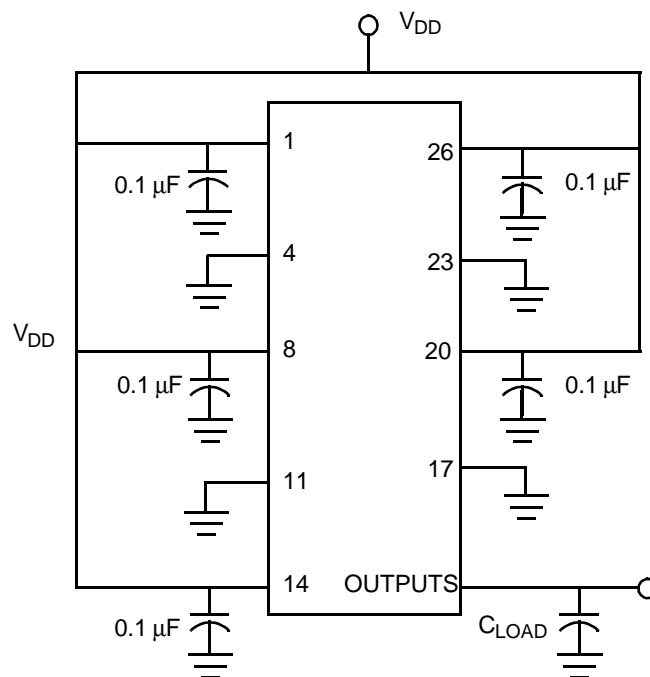
Parameter	Output	Name	Description	Min.	Max.	Unit
$t_1$	All	Output Duty Cycle <sup>[6]</sup>	$t_1 = t_{1A} + t_{1B}$	45%	55%	
$t_2^{[4]}$	CPUCLK, PCICLK	Output Rising and Falling Edge Rate	Measured between 0.4 and 2.4V	1		V/ns
$t_3^{[4]}$	REF, KBDCLK, USBCLK	Rise Time	Measured between 0.4 and 2.4V		4	ns
$t_4^{[4]}$	REF, KBDCLK, USBCLK	Fall Time	Measured between 2.4 and 0.4V		4	ns
$t_5^{[4]}$	CPUCLK	CPU-CPU Clock Skew	Measured at 1.5V		250	ps
$t_6^{[4]}$	PCICLK	PCI-PCI Clock Skew	Measured at 1.5V		250	ps
$t_7^{[4]}$	CPUCLK, PCICLK	CPU-PCI Skew	Measured at 1.5V (-1 option)	1	4	ns
			Measured at 1.5V (-2 option)		500	ps
$t_8^{[4]}$	CPUCLK	Cycle-Cycle Clock Jitter	CPU Clock Jitter		200	ps

**Switching Waveforms**
**Duty Cycle Timing**

**All Outputs Rise/Fall Time**


**Switching Waveforms** (continued)**Clock Skew****Notes:**

5. All parameters specified with outputs fully loaded.
6. Duty cycle is measured at 1.5V.

**Switching Waveforms** (continued)

**CPU-PCI Clock Skew**

**Test Circuit**


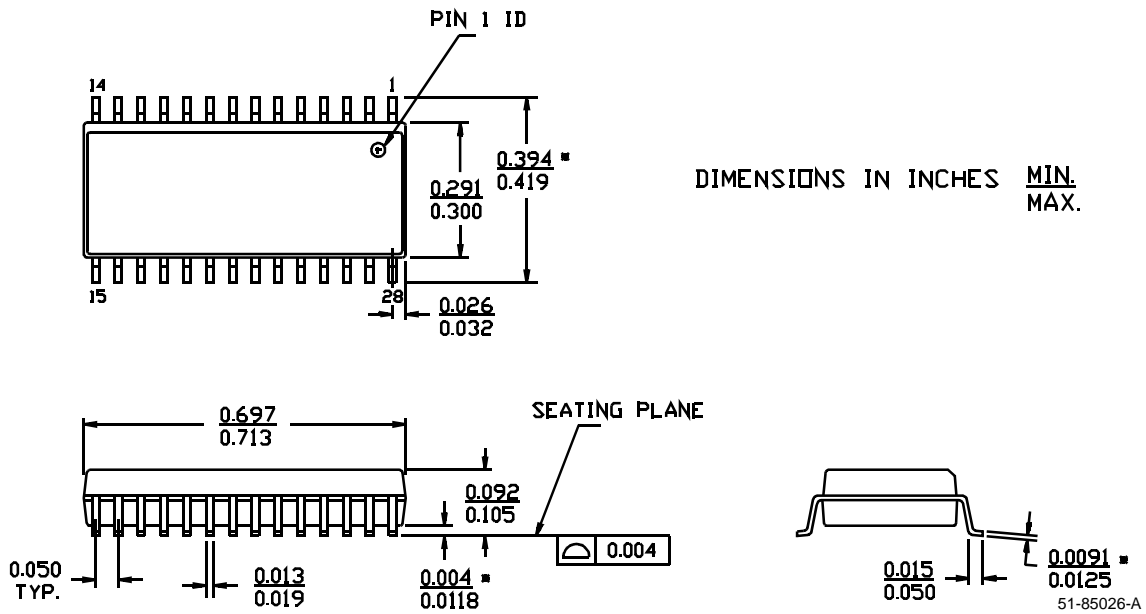
**Note:** All capacitors should be placed as close to each pin as possible.

**Ordering Information**

Ordering Code	Package Name	Package Type	Operating Range
CY2254ASC-1	S21	28-Pin SOIC	Commercial
CY2254ASC-2	S21	28-Pin SOIC	Commercial

Package Diagram

28-Lead (300-Mil) Molded SOIC S21



<b>Document Title: CY2254A Pentium® Processor Compatible Clock Synthesizer/Driver</b>				
<b>Document Number: 38-07203</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	111723	12/15/01	DSG	Change from Spec number: 38-00504 to 38-07203
*A	121838	12/14/02	RBI	Power up requirements added to Operating Conditions Information