

700MHZ, CRYTAL OSCILLATOR-TO-LVDS FREQUENCY SYNTHESIZER

ICS8442I-90

GENERAL DESCRIPTION

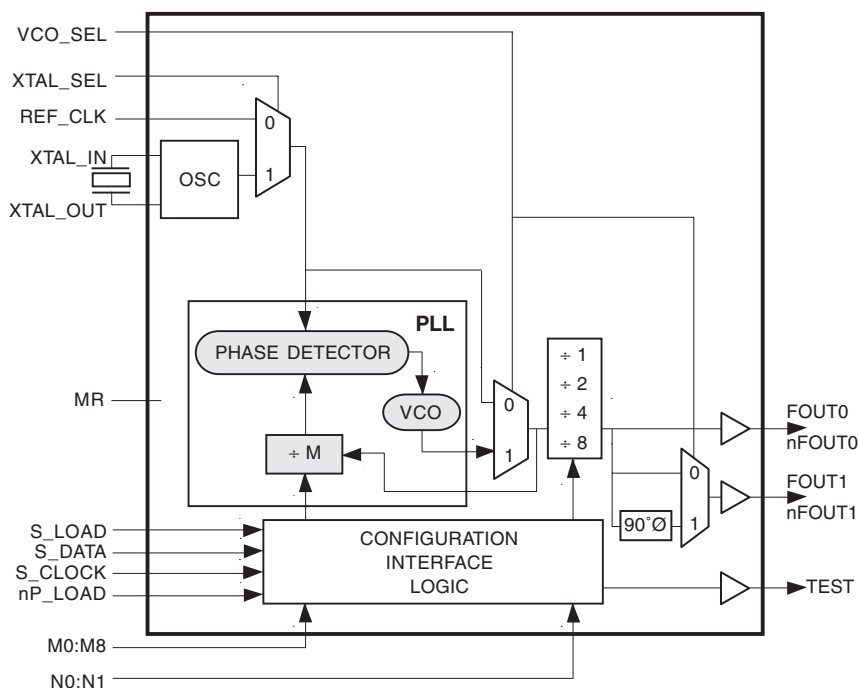


The ICS8442I-90 is a general purpose, dual output Crystal-to-Differential LVDS High Frequency Synthesizer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8442I-90 has a selectable REF_CLK or crystal input. The REF_CLK input accepts LVCMOS or LVTTTL input levels and translates them to LVDS levels. The VCO operates at a frequency range of 250MHz to 700MHz. The VCO frequency is programmed in steps equal to the value of the input reference or crystal frequency. The VCO and output frequency can be programmed using the serial or parallel interface to the configuration logic. The low phase noise characteristics of the ICS8442I-90 makes it an ideal clock source for Gigabit Ethernet and Sonet applications.

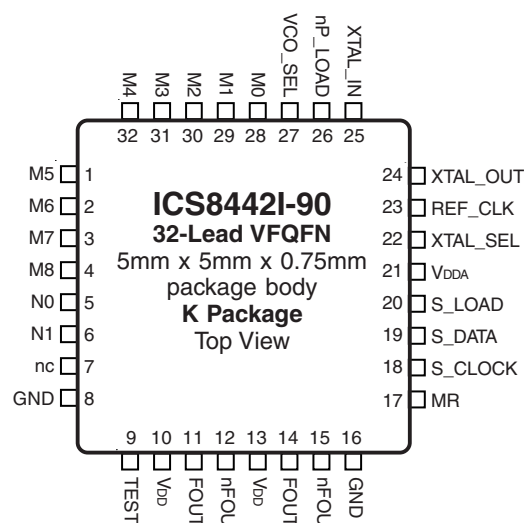
FEATURES

- Dual differential LVDS outputs
FOUT1/nFOUT1 lags FOUT0/nFOUT0 by 90°
- Selectable crystal oscillator interface or LVCMOS/LVTTTL REF_CLK
- Output frequency range: 31.25MHz to 700MHz
- Crystal input frequency range: 10MHz to 25MHz
- VCO range: 250MHz to 700MHz
- Parallel or serial interface for programming counter and output dividers
- RMS period jitter: 3.5ps (typical)
- Cycle-to-cycle jitter: 18ps (typical)
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

BLOCK DIAGRAM



PIN ASSIGNMENT



The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

FUNCTIONAL DESCRIPTION

NOTE: The functional description that follows describes operation using a 25MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1.

The ICS8442I-90 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is fed into the phase detector. A 25MHz crystal provides a 25MHz phase detector reference frequency. The VCO of the PLL operates over a range of 250MHz to 700MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVDS output buffers. The divider provides a 50% output duty cycle.

The programmable features of the ICS8442I-90 support two input modes to program the M divider and N output divider. The two input operational modes are parallel and serial. Figure 1 shows the timing diagram for each mode. In parallel mode, the nP_LOAD input is initially LOW. The data on inputs M0 through M8 and N0 and N1 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. As a result, the M and N bits can be hardwired to set the M divider and N output divider to a spe-

cific default state that will automatically occur during power-up. The TEST output is LOW when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows:

$$f_{VCO} = f_{xtal} \times M$$

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock for a 25MHz reference are defined as $10 \leq M \leq 28$. The frequency output is defined as follows:

$$F_{OUT} = \frac{f_{VCO}}{N} = \frac{f_{xtal} \times M}{N}$$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider and N output divider when S_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider and N output divider on each rising edge of S_CLOCK. The serial mode can be used to program the M and N bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

T1	T0	TEST Output
0	0	LOW
0	1	S_Data, Shift Register Input
1	0	Output of M divider
1	1	CMOS FOUT

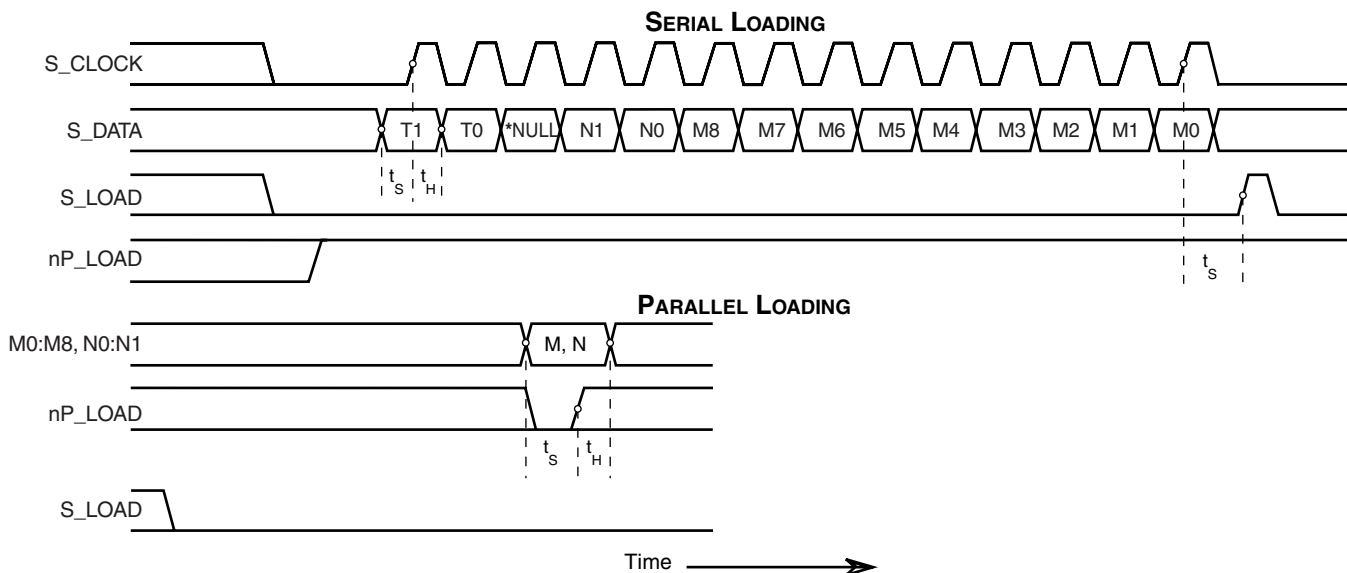


FIGURE 1. PARALLEL & SERIAL LOAD OPERATIONS

*NOTE: The NULL timing slot must be observed.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	M5	Input	Pullup	M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS / LVTTTL interface levels.
2, 3, 4, 28, 29, 30, 31, 32	M6, M7, M8, M0, M1, M2, M3, M4	Input	Pulldown	
5, 6	N0, N1	Input	Pulldown	
7	nc	Unused		No connect.
8, 16	GND	Power		Power supply ground.
9	TEST	Output		Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS / LVTTTL interface levels.
10, 13	V _{DD}	Power		Core supply pins.
11, 12	FOUT1, nFOUT1	Output		Differential output for the synthesizer. Lags FOUT0/nFOUT0 by 90°. LVDS interface levels.
14, 15	FOUT0, nFOUT0	Output		Differential output for the synthesizer. LVDS interface levels.
17	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs FOUTx to go low and the inverted outputs nFOUTx to go high. When logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not effect loaded M, N, and T values. LVCMOS / LVTTTL interface levels.
18	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS / LVTTTL interface levels.
19	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS / LVTTTL interface levels.
20	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the dividers. LVCMOS / LVTTTL interface levels.
21	V _{DDA}	Power		Analog supply pin.
22	XTAL_SEL	Input	Pullup	Selects between crystal oscillator or test inputs as the PLL reference source. Selects XTAL inputs when HIGH. Selects REF_CLK when LOW. LVCMOS / LVTTTL interface levels.
23	REF_CLK	Input	Pullup/ Pulldown	Reference clock input. V _{DD} /2 default when left floating. LVCMOS / LVTTTL interface levels.
24, 25	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
26	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at N1:N0 sets the N output divider value. LVCMOS / LVTTTL interface levels.
27	VCO_SEL	Input	Pullup	Determines whether synthesizer is in PLL or bypass mode. In bypass mode, VCO_SEL = 0, the differential outputs are phase aligned. LVCMOS / LVTTTL interface levels. NOTE 1.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

NOTE 1: In bypass mode, VCO_SEL = 0, the differential outputs are phase aligned.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ
R _{VDD/2}	Pullup/Pulldown Resistors			51		kΩ

TABLE 3A. PARALLEL AND SERIAL MODE FUNCTION TABLE

Inputs							Conditions
MR	nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	
H	X	X	X	X	X	X	Reset. When HIGH, forces the outputs to a differential LOW state (FOUTx = LOW and nFOUTx = HIGH), but does not effect loaded M, N, and T values.
L	L	Data	Data	X	X	X	Data on M and N inputs passed directly to the M divider and N output divider. TEST output forced LOW.
L	↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
L	H	X	X	↓	L	Data	M divider and N output divider values are latched.
L	H	X	X	L	X	X	Parallel or serial input do not affect shift registers.
L	H	X	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

NOTE: L = LOW

H = HIGH

X = Don't care

↑ = Rising edge transition

↓ = Falling edge transition

TABLE 3B. PROGRAMMABLE VCO FREQUENCY FUNCTION TABLE

VCO Frequency (MHz)	M Divide	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
250	10	0	0	0	0	0	1	0	1	0
275	11	0	0	0	0	0	1	0	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
650	26	0	0	0	0	1	1	0	1	0
675	27	0	0	0	0	1	1	0	1	1
700	28	0	0	0	0	1	1	1	0	0

NOTE 1: These M divide values and the resulting frequencies correspond to crystal or TEST_CLK input frequency of 25MHz.

TABLE 3C. PROGRAMMABLE OUTPUT DIVIDER FUNCTION TABLE

Inputs		N Divider Value	Output Frequency (MHz)	
N1	N0		Minimum	Maximum
0	0	1	250	700
0	1	2	125	350
1	0	4	62.5	175
1	1	8	31.25	87.5

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5$ V
Outputs, V_O	-0.5V to $V_{DD} + 0.5$ V
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			165		mA
I_{DDA}	Analog Supply Current			12		mA

TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	M0-M4, M6-M8, N0, N1, MR, nP_LOAD, S_CLOCK, S_DATA, S_LOAD, REF_CLK	$V_{DD} = V_{IN} = 3.465$ V		150	μ A
		M5, XTAL_SEL, VCO_SEL	$V_{DD} = V_{IN} = 3.465$ V		5	μ A
I_{IL}	Input Low Current	M0-M4, M6-M8, N0, N1, MR, nP_LOAD, S_CLOCK, S_DATA, S_LOAD	$V_{DD} = 3.465$ V, $V_{IN} = 0$ V	-5		μ A
		M5, REF_CLK, XTAL_SEL, VCO_SEL	$V_{DD} = 3.465$ V, $V_{IN} = 0$ V	-150		μ A
V_{OH}	Output High Voltage	TEST; NOTE 1	2.6			V
V_{OL}	Output Low Voltage	TEST; NOTE 1			0.5	V

NOTE 1: Outputs terminated with 50 Ω to $V_{DD}/2$. See Parameter Measurement Information section, "3.3V Output Load Test Circuit".

TABLE 4C. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			450		mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage			1.4		V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

TABLE 5. INPUT FREQUENCY CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	REF_CLK; NOTE 1	10		25	MHz
		XTAL_IN, XTAL_OUT; NOTE 1	10		25	MHz
		S_CLOCK			50	MHz

NOTE 1: For the input crystal and REF_CLK frequency range the M value must be set for the VCO to operate within the 250MHz to 700MHz range. Using the minimum input frequency of 10MHz valid values of M are $25 \leq M \leq 70$. Using the maximum frequency of 25MHz valid values of M are $10 \leq M \leq 28$.

TABLE 6. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		25	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 7. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		31.25		700	MHz
$f_{jit}(cc)$	Cycle-to-Cycle Jitter; NOTE 1, 2	N = 1, 2		18		ps
		N = 4		29		ps
$f_{jit}(per)$	Period Jitter, RMS; NOTE 1, 2			3.5		ps
$t_{phase}(\emptyset)$	Output Phase Relationship; NOTE 3			90		$^\circ$
t_R / t_F	Output Rise/Fall Time	20% to 80%	150		750	ps
t_S	Setup Time	M, N to nP_LOAD	5			ns
		S_DATA to S_CLOCK	5			ns
		S_CLOCK to S_LOAD	5			ns
t_H	Hold Time	M, N to nP_LOAD	5			ns
		S_DATA to S_CLOCK	5			ns
		S_CLOCK to S_LOAD	5			ns
odc	Output Duty Cycle; NOTE 4	N > 1		50		%
t_{PW}	Output Pulse Width	N = 1	$t_{Period}/2 - 150$		$t_{Period}/2 + 150$	ps
t_{LOCK}	PLL Lock Time				1	ms

See Parameter Measurement Information section.

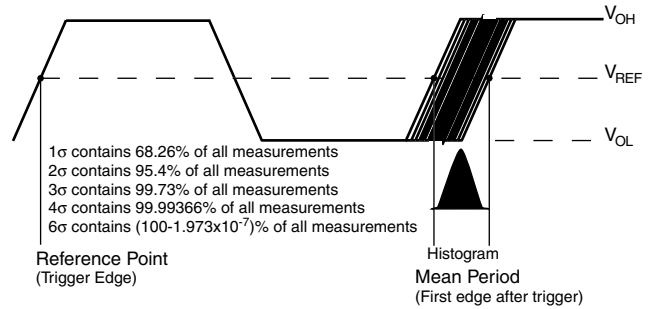
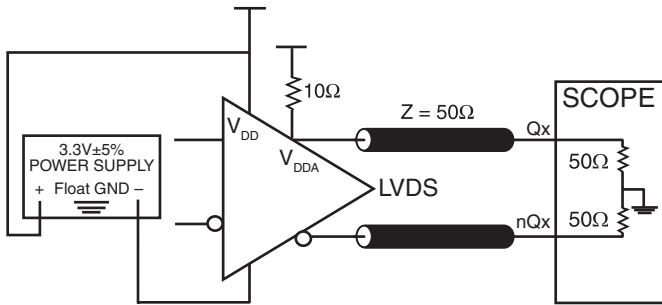
NOTE 1: Jitter performance using XTAL inputs.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Not valid when VCO_SEL = 0.

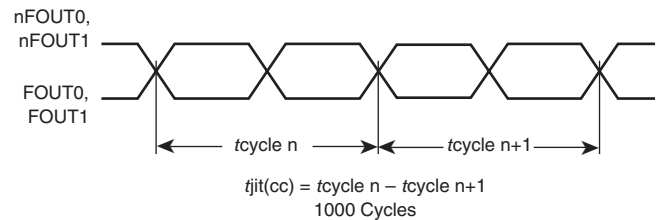
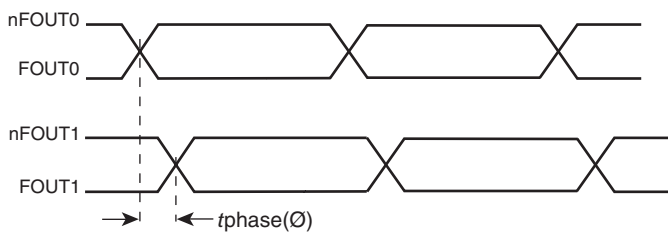
NOTE 4: In the Application Section, please refer to the application note, "Differential Duty Cycle Improvement".

PARAMETER MEASUREMENT INFORMATION



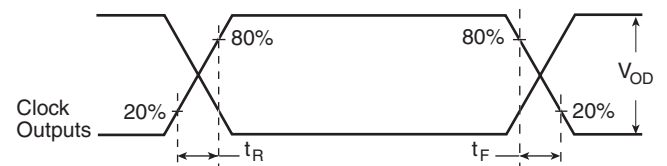
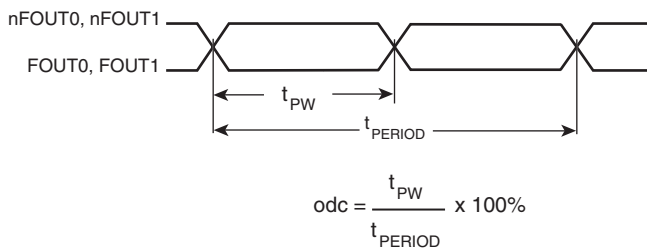
3.3V LVDS OUTPUT LOAD AC TEST CIRCUIT

PERIOD JITTER



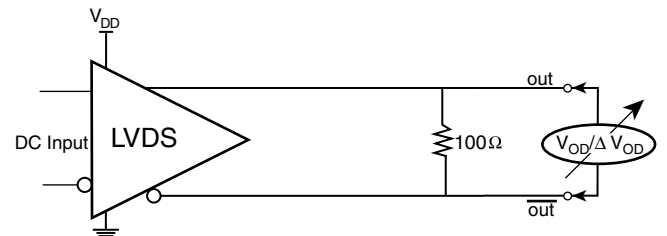
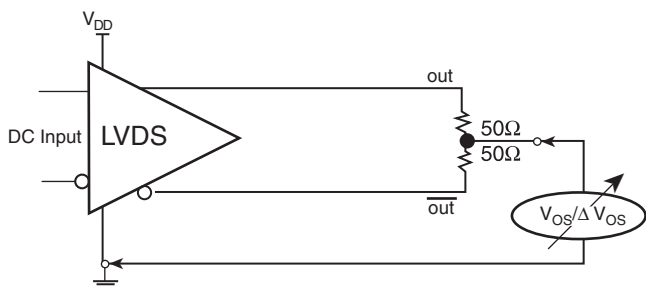
OUTPUT PHASE RELATIONSHIP

CYCLE-TO-CYCLE JITTER



OUTPUT DUTY CYCLE

OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP

DIFFERENTIAL OUTPUT VOLTAGE SETUP

APPLICATION INFORMATION

STORAGE AREA NETWORKS

A variety of technologies are used for interconnection of the elements within a SAN. The tables below lists the common

frequencies used as well as the settings for the ICS8442I-90 to generate the appropriate frequency.

TABLE 8. COMMON SANs APPLICATION FREQUENCIES

Interconnect Technology	Clock Rate	Reference Frequency to SERDES (MHz)	Crystal Frequency (MHz)
Gigabit Ethernet	1.25 GHz	125, 250, 156.25	25, 19.53125
Fibre Channel	FC1 1.0625 GHz FC2 2.1250 GHz	106.25, 53.125, 132.8125	16.6015625, 25
Infiniband	2.5 GHz	125, 250	25

TABLE 9. CONFIGURATION DETAILS FOR SANs APPLICATIONS

Interconnect Technology	Crystal Frequency (MHz)	ICS8442I-90 Output Frequency to SERDES (MHz)	ICS8442I-90 M & N Settings										
			M8	M7	M6	M5	M4	M3	M2	M1	M0	N1	N0
Gigabit Ethernet	25	125	0	0	0	0	1	0	1	0	0	1	0
	25	250	0	0	0	0	1	0	1	0	0	0	1
	25	156.25	0	0	0	0	1	1	0	0	1	1	0
	19.53125	156.25	0	0	0	1	0	0	0	0	0	1	0
Fiber Channel 1	25	53.125	0	0	0	0	1	0	0	0	1	1	1
	25	106.25	0	0	0	0	1	0	0	0	1	1	0
Fiber Channel 2	16.6015625	132.8125	0	0	0	1	0	0	0	0	0	1	0
Infiniband	25	125	0	0	0	0	1	0	1	0	0	1	0
	25	250	0	0	0	0	1	0	1	0	0	0	1

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8442I-90 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. Figure 2 illustrates how a 10Ω resistor along with a 10μF and a .01μF bypass capacitor should be connected to each V_{DDA} .

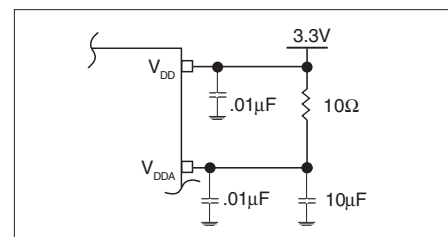


FIGURE 2. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

A crystal can be characterized for either series or parallel mode operation. The ICS8442I-90 has a built-in crystal oscillator circuit. This interface can accept either a series or parallel crystal without additional components and generate

frequencies with accuracy suitable for most applications. Additional accuracy can be achieved by adding two small capacitors C1 and C2 as shown in *Figure 3*. Typical results using parallel 18pF crystals are shown in Table 10.

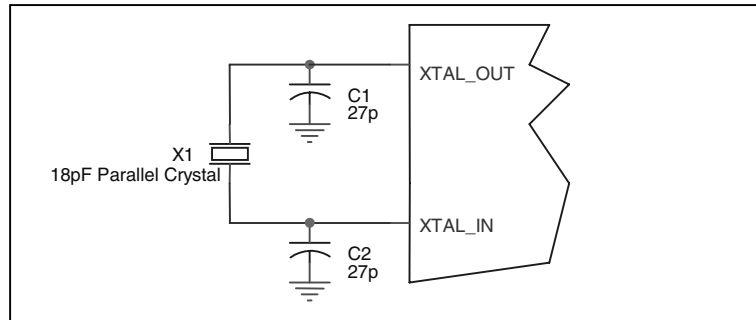


FIGURE 3. CRYSTAL INPUT INTERFACE

LVC MOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4*. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver (R_o) plus the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50 Ω applications, R_1 and R_2 can be 100 Ω . This can also be accomplished by removing R_1 and making R_2 50 Ω .

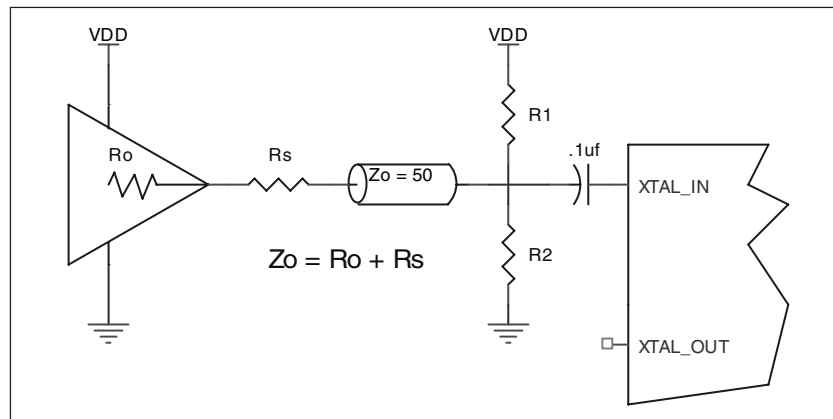


FIGURE 4. GENERAL DIAGRAM FOR LVC MOS DRIVER TO XTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT:

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from the REF_CLK to ground.

LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

OUTPUTS:

LVDS Output

All unused LVDS output pairs can be either left floating or terminated with 100 Ω across. If they are left floating, there should be no trace attached.

DIFFERENTIAL DUTY CYCLE IMPROVEMENT

The schematic below is recommended for applications using the ± 1 output configuration for improving the differential duty cycle.

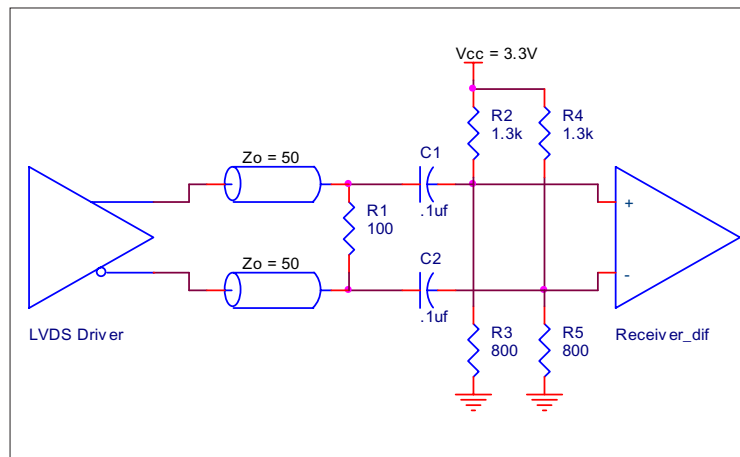


FIGURE 5. DIFFERENTIAL DUTY CYCLE IMPROVEMENT

THERMAL RELEASE PATH

The expose metal pad provides heat transfer from the device to the P.C. board. The expose metal pad is ground pad connected to ground plane through thermal via. The exposed pad on the device to the exposed metal pad on the PCB is contacted through

solder as shown in *Figure 6*. For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

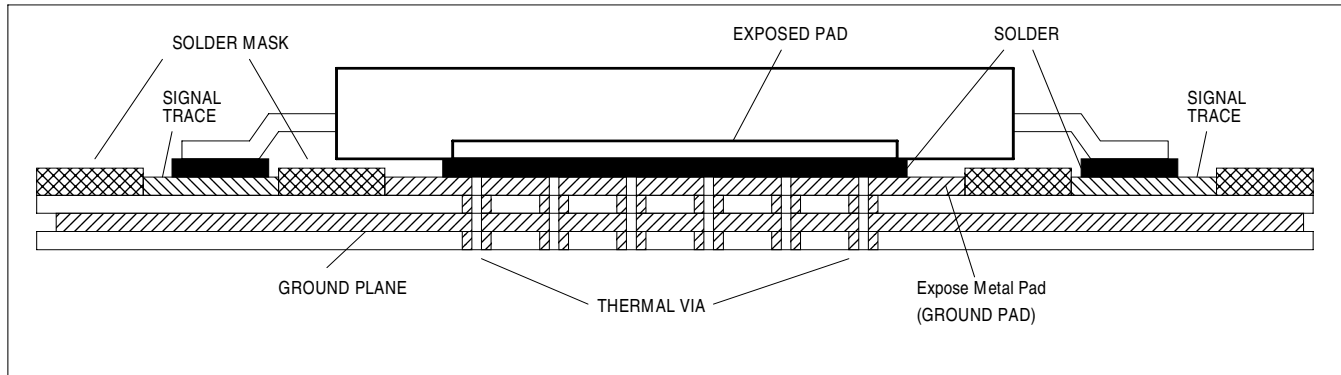


FIGURE 6. P.C. BOARD FOR EXPOSED PAD THERMAL RELEASE PATH EXAMPLE

LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 7*. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver

input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

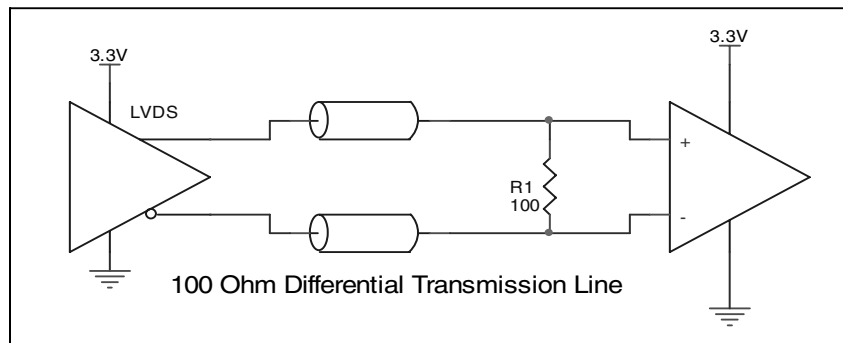


FIGURE 7. TYPICAL LVDS DRIVER TERMINATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8422I-90. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8422I-90 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

- Power (core)_{MAX} = $V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (165mA + 12mA) = 578.65mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 10 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:
 $85°C + 0.579W * 37°C/W = 106.4°C$. This is well below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 10. THERMAL RESISTANCE θ_{JA} FOR 32-LEAD VFQFN, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

RELIABILITY INFORMATION

TABLE 11. θ_{JA} vs. AIR FLOW TABLE FOR 32 LEAD VFQFN

θ_{JA} vs. Air Flow (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

TRANSISTOR COUNT

The transistor count for ICS8442I-90 is: 4358

PACKAGE OUTLINE - K SUFFIX FOR 32 LEAD VFQFN

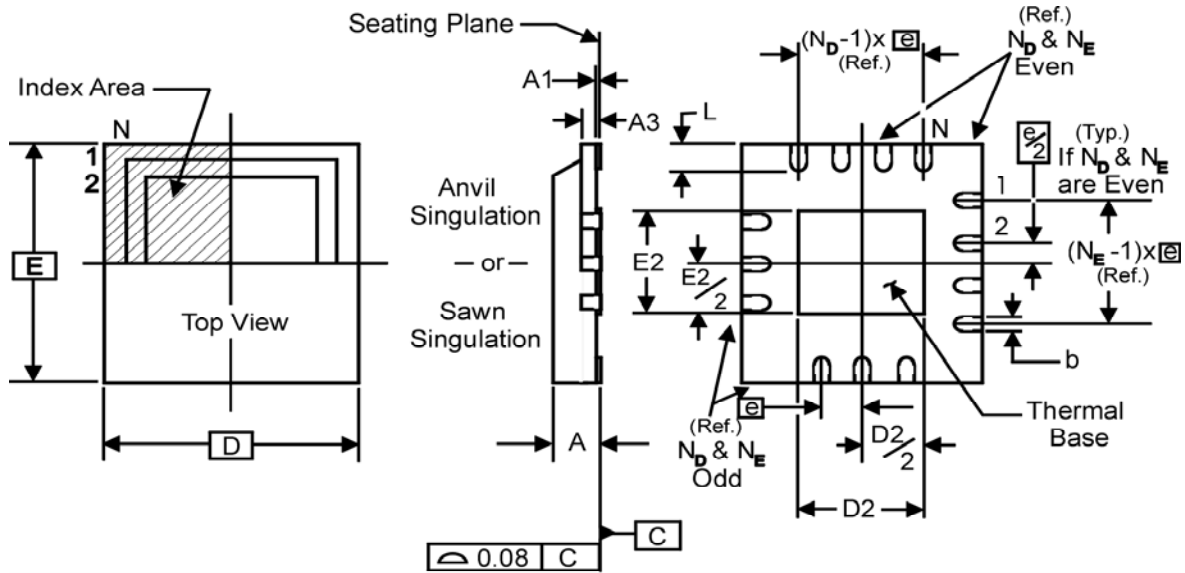


TABLE 12. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	VHHD-2		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	0.80	--	1.00
A1	0	--	0.05
A3	0.25 Ref.		
b	0.18	0.25	0.30
N_D			8
N_E			8
D	5.00 BASIC		
D2	1.25	2.25	3.25
E	5.00 BASIC		
E2	1.25	2.25	3.25
e	0.50 BASIC		
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 13. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8442AKI-90	TBD	32 Lead VFQFN	Tray	-40°C to 85°C
ICS8442AKI-90T	TBD	32 Lead VFQFN	1000 Tape & Reel	-40°C to 85°C
ICS8442AKI-90LF	ICS442AI90L	32 Lead "Lead-Free" VFQFN	Tray	-40°C to 85°C
ICS8442AKI-90LFT	ICS442AI90L	32 Lead "Lead-Free" VFQFN	1000 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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